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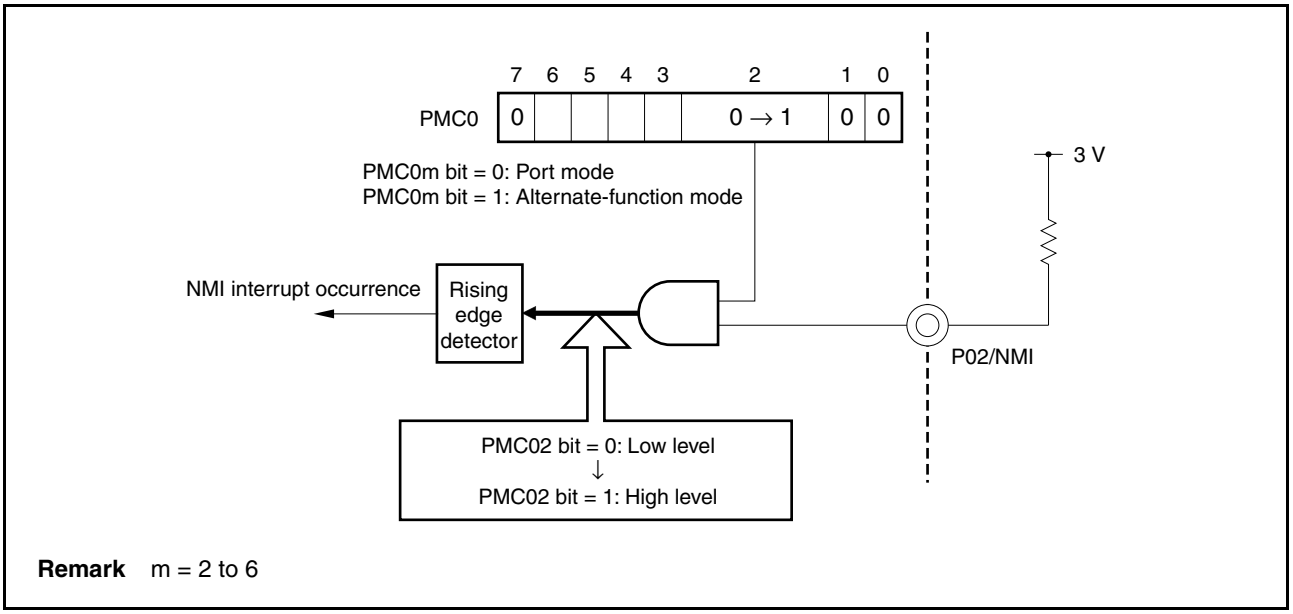
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | V850ES |
| Core Size | 32-Bit Single-Core |
| Speed | 20MHz |
| Connectivity | CSI, EBI/EMI, I²C, UART/USART |
| Peripherals | DMA, LVD, PWM, WDT |
| Number of I/O | 83 |
| Program Memory Size | 768KB (768K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 80K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 12x10b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 121-LBGA |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3841f1-cah-a |

**Figure 4-37. Example of Switching from P02 to NMI (Incorrect)**



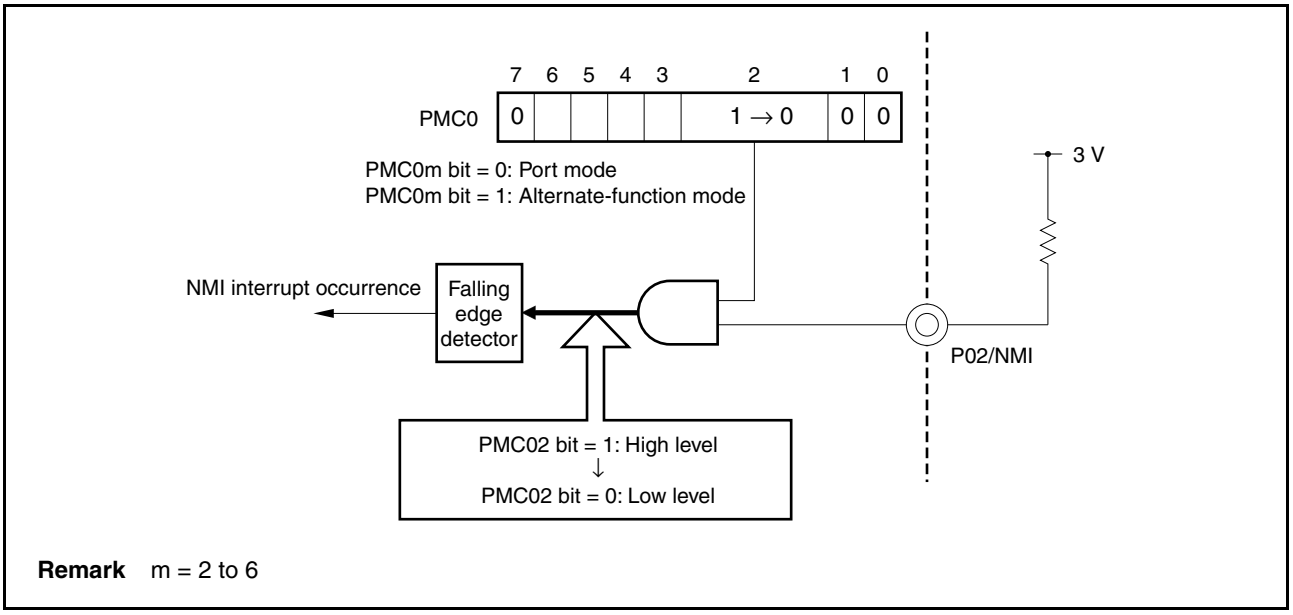

**Remark** m = 2 to 6

[Example 2] Switching from external pin (NMI) to general-purpose port pin (P02)

When the P02/NMI pin is pulled up as shown in Figure 4-38 and the falling edge is specified by the NMI pin edge detection setting, even though a high level is input continuously to the NMI pin when switching from the NMI pin to the P02 pin (PMC02 bit = 1 → 0), this is detected as a falling edge, as if the high level changed to a low level, and an NMI interrupt occurs.

To avoid this, set the NMI pin edge detection as “No edge detected” before switching to the P02 pin.

**Figure 4-38. Example of Switching from NMI to P02 (Incorrect)**




**Remark** m = 2 to 6

(2) In port mode, the PFn.PFnm bit is valid only in the output mode (PMn.PMnm bit = 0). In the input mode (PMnm bit = 1), the value of the PFnm bit is not reflected in the buffer.

**(9) TMPn counter read buffer register (TPnCNT)**

The TPnCNT register is a read buffer register from which the count value of the 16-bit counter can be read.

If this register is read when the TPnCTL0.TPnCE bit = 1, the count value of the 16-bit timer can be read.

This register is read-only, in 16-bit units.

The value of the TPnCNT register is cleared to 0000H when the TPnCE bit = 0. If the TPnCNT register is read at this time, the value of the 16-bit counter (FFFFH) is not read, but 0000H is read.

Because the TPnCE bit is cleared to 0, the value of the TPnCNT register is cleared to 0000H after reset.

**Caution Accessing the TPnCNT register is prohibited in the following statuses. Moreover, if the system is in the wait status, the only way to cancel the wait status is to execute a reset. For details, see 3.4.9 (1) Accessing specific on-chip peripheral I/O registers.**

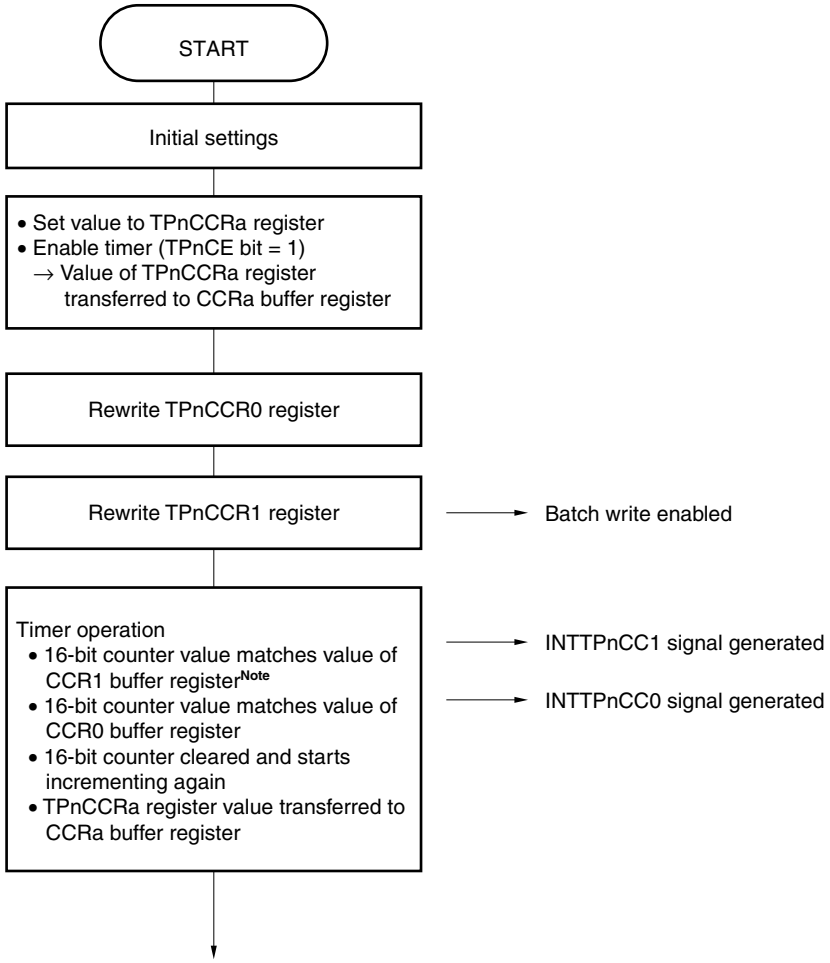
- **When the CPU operates on the subclock and main clock oscillation is stopped**
- **When the CPU operates on the internal oscillator clock**

After reset: 0000H R Address: TP0CNT FFFFF59AH, TP1CNT FFFFF5AAH, TP2CNT FFFFF5BAH, TP3CNT FFFFF5CAH, TP4CNT FFFFF5DAH, TP5CNT FFFFF5EAH

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPnCNT | | | | | | | | | | | | | | | | |

(n = 0 to 5)

**Figure 6-4. Flowchart Showing Basic Batch Write Operation**




**Note** The 16-bit counter is only cleared when its value matches the value of the CCR0 buffer register, not the CCR1 buffer register.

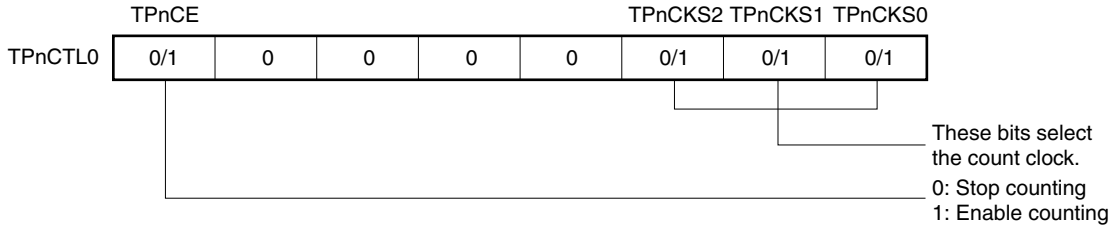
**Caution The process of writing to the TPnCCR1 register includes enabling batch write. It is therefore necessary to rewrite the TPnCCR1 register after rewriting the TPnCCR0 register.**

**Remarks 1.** The flowchart applies to the case when TMPn is being used in the PWM output mode.

**2.** a = 0, 1

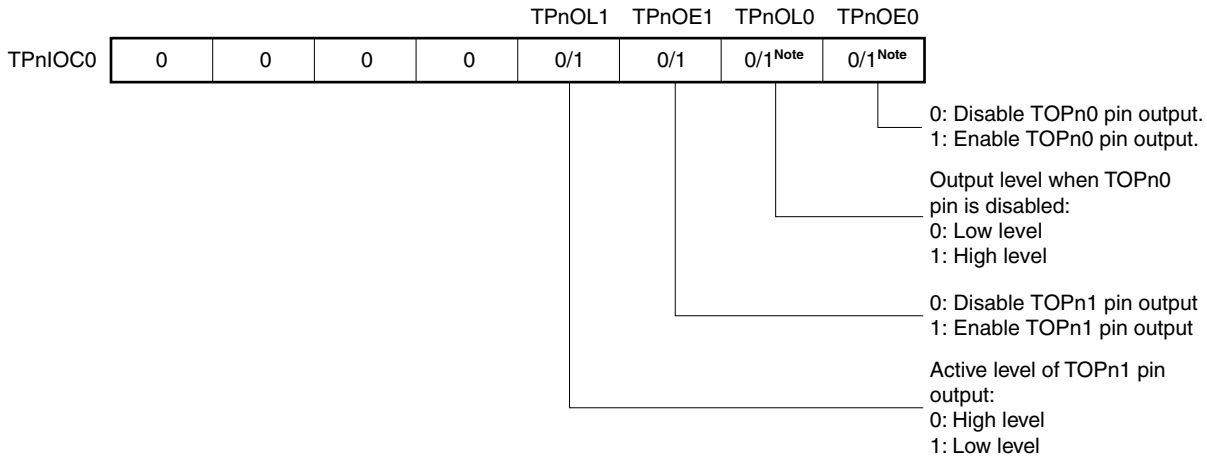
**Figure 6-40. Register Settings in One-Shot Pulse Output Mode (1/2)**

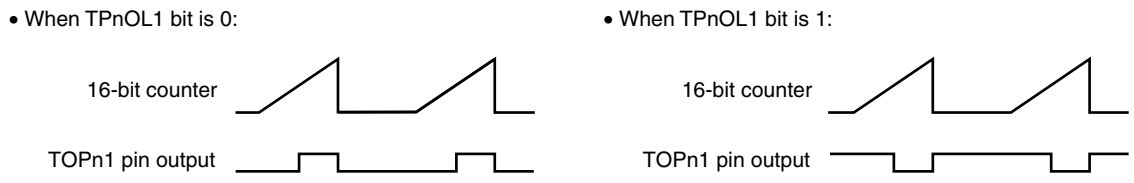
**(a) TMPn control register 0 (TPnCTL0)**




**(b) TMPn control register 1 (TPnCTL1)**


**(c) TMPn I/O control register 0 (TPnIOC0)**




**Note** Set this bit to 0 when not using the TOPn0 pin in the one-shot pulse output mode.

### 7.2.2 Interrupts

The following five types of interrupt signals are used by TMQ0:

(1) INTTQ0CC0

This signal is generated when the value of the 16-bit counter matches the value of the CCR0 buffer register, or when a capture signal is input from the TIQ00 pin.

(2) INTTQ0CC1

This signal is generated when the value of the 16-bit counter matches the value of the CCR1 buffer register, or when a capture signal is input from the TIQ01 pin.

(3) INTTQ0CC2

This signal is generated when the value of the 16-bit counter matches the value of the CCR2 buffer register, or when a capture signal is input from the TIQ02 pin.

(4) INTTQ0CC3

This signal is generated when the value of the 16-bit counter matches the value of the CCR3 buffer register, or when a capture signal is input from the TIQ03 pin.

(5) INTTQ0OV

This signal is generated when the 16-bit counter overflows after incrementing up to FFFFH.

The following table shows the functions of the capture/compare register in each operation mode, and how to write data to the compare register.

**Table 7-4. Function of Capture/Compare Register in Each Mode and How to Write Compare Register**

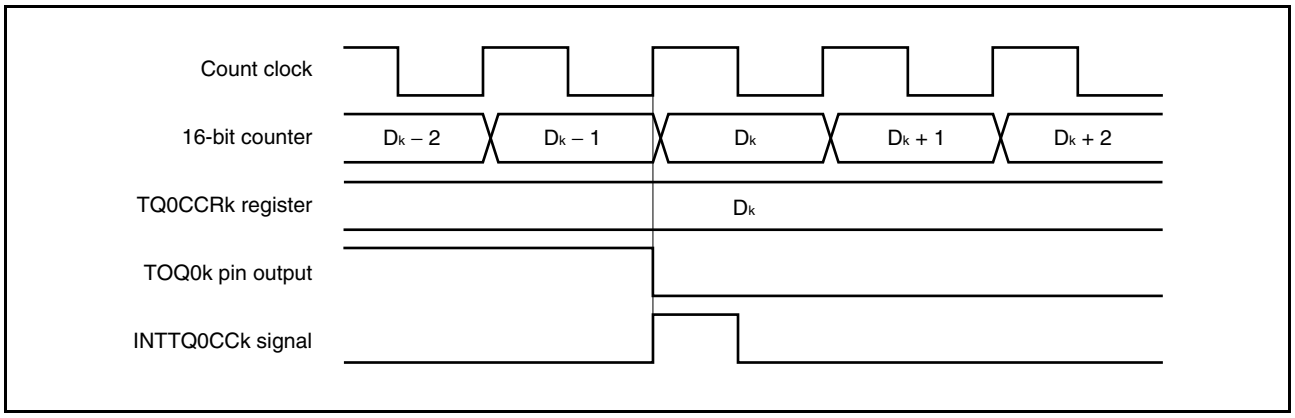
| Operation Mode | Capture/Compare Register | How to Write Compare Register |
|---|---|---|
| Interval timer | Compare register | Anytime write |
| External event counter | Compare register | Anytime write |
| External trigger pulse output | Compare register | Batch write |
| One-shot pulse output | Compare register | Anytime write |
| PWM output | Compare register | Batch write |
| Free-running timer | Capture/compare register | Anytime write |
| Pulse width measurement | Capture register | – |

**Remark** For details about anytime write and batch write, see **7.4 (2) Anytime write and batch write**.

**(b) Timing of generating the compare match interrupt request signal (INTTQ0CCk)**

In the one-shot pulse output mode, the INTTQ0CCk signal is generated when the value of the 16-bit counter matches the value of the TQ0CCRk register.

**Figure 7-43. Timing of Generating Compare Match Interrupt Signal (INTTQ0CCk)**




**Remark** k = 1 to 3

### (1) Operations in interval timer mode

**Figure 8-5. Timing and Processing of Operations in Interval Timer Mode**

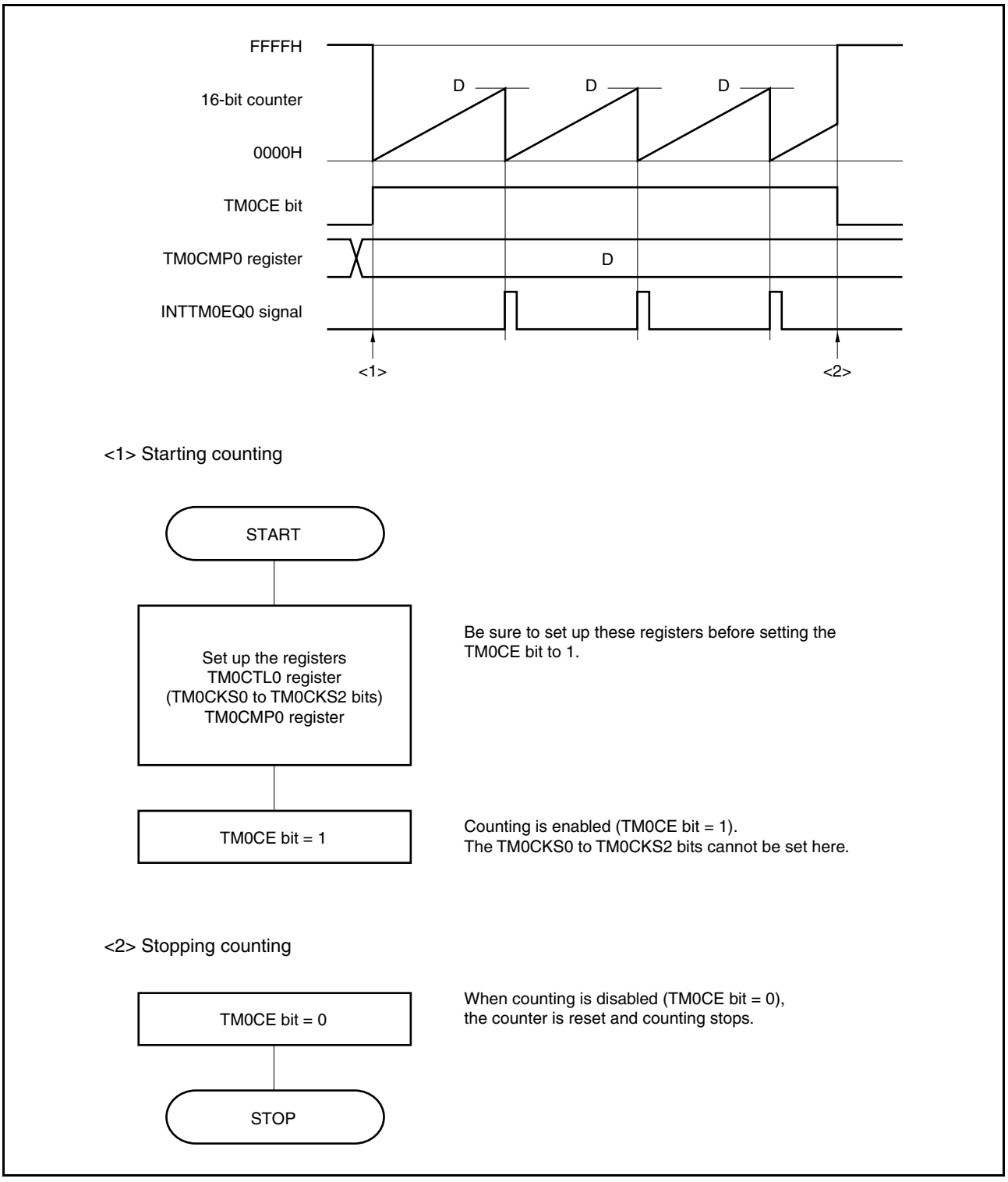
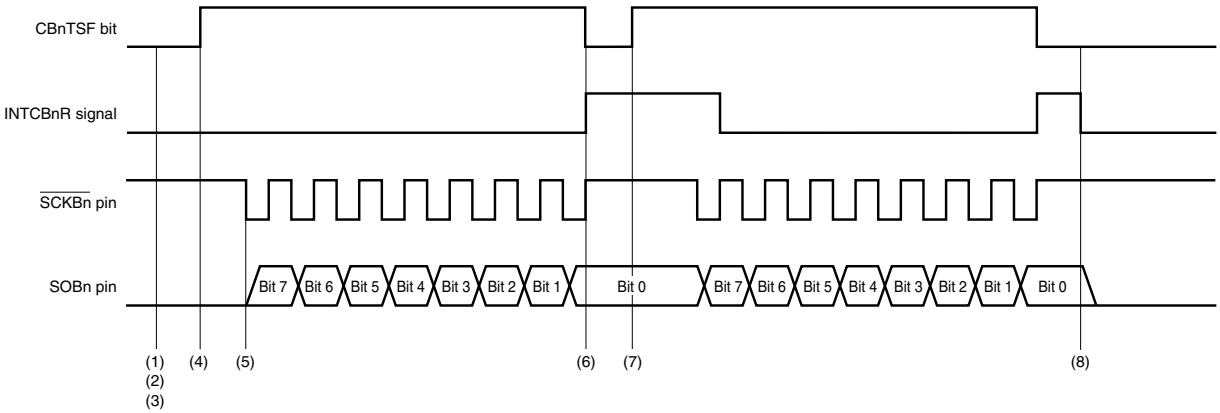


**Figure 16-6. Single Transfer Mode Operation Timing (Master Mode, Transmission Mode)**




(1) Write 00H to the CBnCTL1 register, and select communication type 1, communication clock ($f_{CCLK}$) = $f_{XX}$/2, and master mode.

(2) Write 00H to the CBnCTL2 register, and set the transfer data length to 8 bits.

(3) Write C1H to the CBnCTL0 register, and select the transmission mode and MSB first at the same time as enabling the operation of the communication clock ($f_{CCLK}$).

(4) The CBnSTR.CBnTSF bit is set to 1 by writing the transmit data to the CBnTX register, and transmission is started.

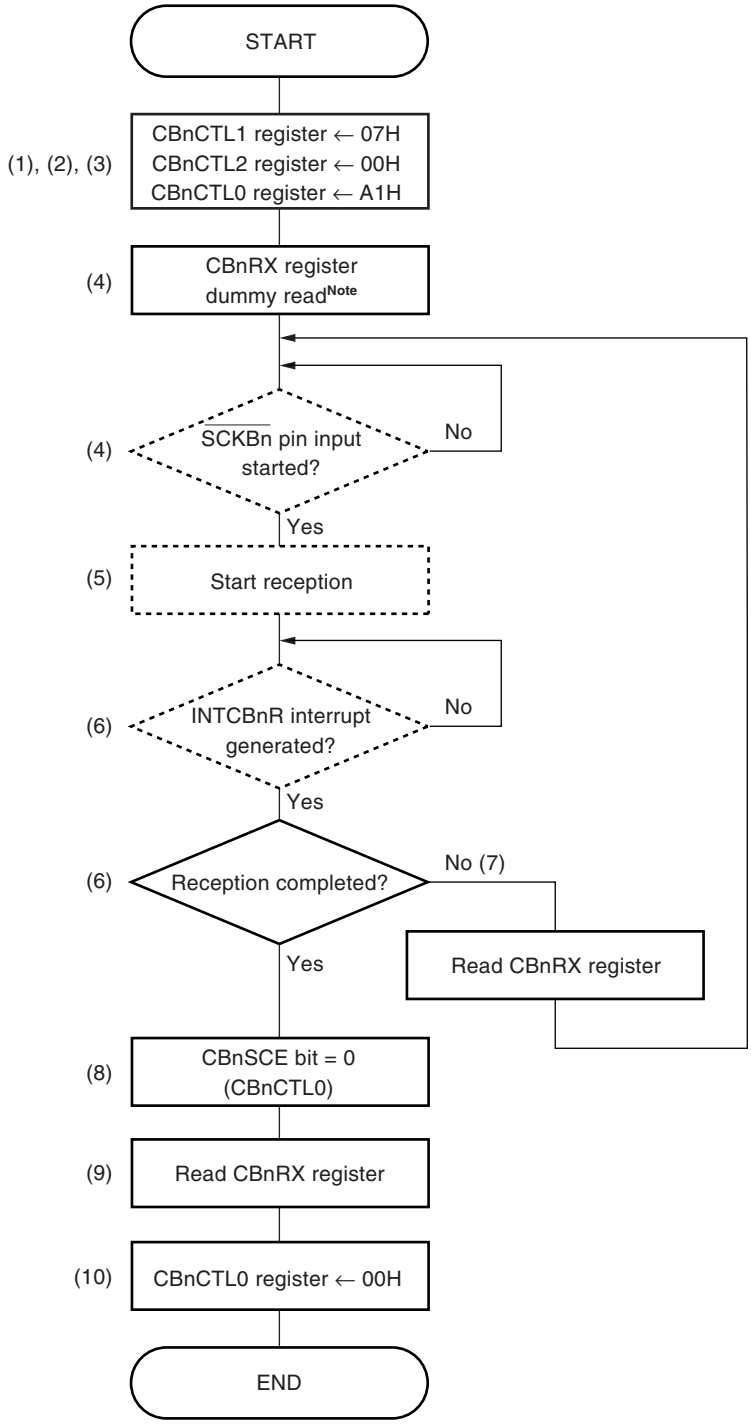
(5) When transmission is started, output the serial clock to the $\overline{\text{SCKBn}}$ pin, and output the transmit data from the SOBn pin in synchronization with the serial clock.

(6) When transmission of data of the transfer data length set by the CBnCTL2 register is completed, stop the serial clock output and transmit data output, generate the reception complete interrupt request signal (INTCBnR) at the last edge of the serial clock cycle, and clear the CBnTSF bit to 0.

(7) To continue transmission, repeat the above steps from (4) after the INTCBnR signal is generated.

(8) To end transmission, clear the CBnCTL0.CBnPWR and CBnCTL0.CBnTXE bits to 0.

**Figure 16-13. Single Transfer Mode Operation (Slave Mode, Reception Mode)**




**Note** If the serial clock is input via the $\overline{\text{SCKBn}}$ pin of the master before a dummy-read of the CBnRX register is executed, data cannot be received normally. In this case, initialize both the master and the slave.

**Remarks 1.** The broken lines indicate the hardware processing.

**2.** The numbers in this figure correspond to the processing numbers in **Figure 16-14**.

## 17.2 Features

I²C0n have the following two modes.

- Operation stopped mode
- I²C (Inter IC) bus mode (multimasters supported)

**(1) Operation stopped mode**

In this mode, serial transfers are not performed, thus enabling a reduction in power consumption.

**(2) I²C bus mode (multimaster support)**

This mode is used for 8-bit data transfers with several devices via two lines: a serial clock pin (SCL0n) and a serial data bus pin (SDA0n).

This mode complies with the I²C bus format and the master device can generate “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition” data to the slave device via the serial data bus. The slave device automatically detects the received statuses and data by hardware. This function can simplify the part of an application program that controls the I²C bus.

Since SCL0n and SDA0n pins are used for N-ch open-drain outputs, I²C0n requires pull-up resistors for the serial clock line and the serial data bus line.

### 19.3.4 Interrupt control register (xxICn)

An xxICn register is assigned to each interrupt request signal (maskable interrupt) and sets the control conditions for each maskable interrupt request.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 47H.

**Cautions 1. To mask interrupts, set up the IMR register or use a bit manipulation instruction. The priority levels must be specified at a time when no interrupt will occur.**

**2. Disable interrupts (DI) before reading the xxICn.xxIFn bit. If the xxIFn bit is read while interrupts are enabled (EI), the correct value may not be read if acknowledging an interrupt and reading the bit conflict.**

After reset: 47H R/W Address: FFFFF110H to FFFFF17CH

| | <7> | <6> | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| xxICn | xxIFn | xxMKn | 0 | 0 | 0 | xxPRn2 | xxPRn1 | xxPRn0 |

| xxIFn | Interrupt request flag[Note] |
|---|---|
| 0 | Interrupt request not issued |
| 1 | Interrupt request issued |

| xxMKn | Interrupt mask flag |
|---|---|
| 0 | Interrupt servicing enabled |
| 1 | Interrupt servicing disabled (pending) |

| xxPRn2 | xxPRn1 | xxPRn0 | Interrupt priority specification bit |
|---|---|---|---|
| 0 | 0 | 0 | Specifies level 0 (highest). |
| 0 | 0 | 1 | Specifies level 1. |
| 0 | 1 | 0 | Specifies level 2. |
| 0 | 1 | 1 | Specifies level 3. |
| 1 | 0 | 0 | Specifies level 4. |
| 1 | 0 | 1 | Specifies level 5. |
| 1 | 1 | 0 | Specifies level 6. |
| 1 | 1 | 1 | Specifies level 7 (lowest). |

**Note** The flag xxIFn is reset automatically by the hardware if an interrupt request signal is acknowledged.

**Remark** xx: Identification name of each peripheral unit (see **Table 19-3 Interrupt Control Registers (xxICn)**)
n: Peripheral unit number (see **Table 19-3 Interrupt Control Registers (xxICn)**).

The addresses and bits of the interrupt control registers are as follows.

### 21.8.2 Releasing sub-IDLE mode/low-voltage sub-IDLE mode

The sub-IDLE mode/low-voltage sub-IDLE mode is released by a non-maskable interrupt request signal (NMI pin input, INTWDT2 signal), unmasked external interrupt request signal (INTP0 to INTP7 pin input), unmasked internal interrupt request signal from the peripheral functions operable in the sub-IDLE mode/low-voltage sub-IDLE mode, or reset signal (reset by $\overline{\text{RESET}}$ pin input, WDT2RES signal, low-voltage detector (LVI), or clock monitor (CLM)). The PLL returns to the operating status it was in before the sub-IDLE mode was set. It returns to the stop status in the low-voltage sub-IDLE mode.

When the sub-IDLE mode is released by an interrupt request signal, the subclock operation mode is set.

When the low-voltage sub-IDLE mode is released by an interrupt request signal, the low-voltage subclock operation mode is set.

For releasing low-voltage subclock operation mode, see **21.7.3 Releasing low-voltage subclock operation mode**.

**(1) Releasing sub-IDLE mode/low-voltage sub-IDLE mode by non-maskable interrupt request signal or unmasked maskable interrupt request signal**

The sub-IDLE mode/low-voltage sub-IDLE mode is released by a non-maskable interrupt request signal or an unmasked maskable interrupt request signal, regardless of the priority of the interrupt request. If the sub-IDLE mode/low-voltage sub-IDLE mode is set in an interrupt servicing routine, however, an interrupt request signal that is issued later is serviced as follows.

**Table 21-15. Operation After Releasing Sub-IDLE Mode/Low-Voltage IDLE Mode by Interrupt Request Signal**

| Release Source | Interrupt Acknowledgment Status | Status After Release | Operation After Release |
|---|---|---|---|
| Reset | Disabled (DI) | – | Normal reset operation |
| | Enabled (EI) | | |
| Non-maskable interrupt request signal (excluding multiple interrupts) | Disabled (DI) | – | The interrupt request is acknowledged when the sub-IDLE mode/low-voltage sub-IDLE mode is released. |
| | Enabled (EI) | | |
| Maskable interrupt request signal | Disabled (DI) | – | The sub-IDLE mode/low-voltage sub-IDLE mode is released but the interrupt request that is the release source is not acknowledged. The interrupt request itself is retained. The processing that was being executed before shifting to the sub-IDLE mode/low-voltage sub-IDLE mode is executed. |
| | Enabled (EI) | • An interrupt request with a priority higher than that of the release source is being serviced. | The sub-IDLE mode/low-voltage sub-IDLE mode is released but the interrupt request that is the release source is not acknowledged. The interrupt request itself is retained. The interrupt that was being serviced before shifting to the sub-IDLE mode/low-voltage sub-IDLE mode is serviced. |
| | | • An interrupt request with a priority lower than that of the release source is being serviced. | The interrupt request is acknowledged when the sub-IDLE mode/low-voltage sub-IDLE mode is released. |

**Cautions1. An interrupt request signal that is disabled by setting the PSC.NMI2M, PSC.NMI0M, and PSC.INTM bits to 1 (interrupt disabled) is invalid and cannot release the sub-IDLE mode/low-voltage sub-IDLE mode.**

**2. When the sub-IDLE mode/low-voltage sub-IDLE mode are released, 12 cycles of the subclock (about 366 $\mu$ s) elapse from when the interrupt request signal that releases the sub-IDLE mode is generated to when the mode is released.**

## 22.4 Operation

### 22.4.1 Reset operation via $\overline{\text{RESET}}$ pin

When a low level is input to the $\overline{\text{RESET}}$ pin, the system is reset, and each hardware unit is initialized.

When the level of the $\overline{\text{RESET}}$ pin is changed from low to high, the reset status ends.

The $\overline{\text{RESET}}$ pin has an internal noise elimination circuit that uses analog delay (60 ns (TYP.)) to prevent malfunction caused by noise.

**Table 22-1. Hardware Status on $\overline{\text{RESET}}$ Pin Input**

| Item | During Reset | After Reset |
|---|---|---|
| Main clock oscillator ($f_X$) | Oscillation stops | Oscillation starts |
| Subclock oscillator ($f_{XT}$) | Oscillation continues | |
| Internal oscillator | Oscillation stops | Oscillation starts |
| Peripheral clock ($f_X$ to $f_X$/1,024) | Operation stops | Operation starts after securing oscillation stabilization time |
| Internal system clock ($f_{CLK}$), CPU clock ($f_{CPU}$) | Operation stops | Operation starts after securing oscillation stabilization time (initialized to $f_{XX}$/8) |
| CPU | Initialized | Program execution starts at address 00000000H after securing oscillation stabilization time |
| Watchdog timer 2 | Operation stops (initialized to 0) | Counts up from 0 with internal oscillator clock as source clock. |
| RTC | Operation continues | |
| Internal RAM | Undefined if power-on reset or CPU access and reset input conflict (data is damaged). Otherwise value immediately after reset input is retained. | |
| I/O lines (ports/alternate-function pins) | High impedance[Note] | |
| On-chip peripheral I/O registers | Initialized to specified status, OCDM register is set (01H). | |
| Other on-chip peripheral functions | Operation stops | Operation can be started after securing oscillation stabilization time |

**Note** When the power is turned on, the following pins may output an undefined level temporarily even during reset.

- P10/ANO0 pin
- P53/SIB2/KR3/TIQ00/TOQ00/RTP03/DDO pin

**Caution The OCDM register is initialized by the $\overline{\text{RESET}}$ pin input. Therefore, note with caution that, if a high level is input to the P05/$\overline{\text{DRST}}$ pin immediately after a reset ends before the OCDM.OCDM0 bit is cleared, the on-chip debug mode may be entered. For details, see CHAPTER 4 PORT FUNCTIONS.**

### 29.1.4 Registers

**(1) On-chip debug mode register (OCDM)**

This register is used to specify whether a pin provided with an on-chip debug function is used as an on-chip debug pin or as an ordinary port/peripheral function pin. It also is used to disconnect the internal pull-down resistor of the P05/INTP2/$\overline{\text{DRST}}$ pin.

This register is a special register and can be written only in a combination of specific sequences (see **3.4.7 Special registers**).

The OCDM register can be written only while a low level is input to the P05/INTP2/$\overline{\text{DRST}}$ pin.

This register can be read or written in 8-bit or 1-bit units.

After reset: 01H[Note] R/W Address: FFFFF9FCH

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | <0> |
|---|---|---|---|---|---|---|---|---|
| OCDM | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OCDM0 |

| OCDM0 | Operation mode |
|---|---|
| 0 | Selects normal operation mode (in which a pin that functions alternately as on-chip debug function pin is used as a port/peripheral function pin) and disconnects the on-chip pull-down resistor of the P05/INTP2/$\overline{\text{DRST}}$ pin. |
| 1 | When P05/INTP2/$\overline{\text{DRST}}$ pin is low:<br>Normal operation mode (in which a pin that functions alternately as an on-chip debug function pin is used as a port/peripheral function pin)<br>When P05/INTP2/$\overline{\text{DRST}}$ pin is high:<br>On-chip debug mode (in which a pin that functions alternately as an on-chip debug function pin is used as an on-chip debug mode pin) |

**Note** $\overline{\text{RESET}}$ input sets this register to 01H. After reset by the WDT2RES signal, clock monitor (CLM), or low-voltage detector (LVI), however, the value of the OCDM register is retained.

**Cautions 1. When using the DDI, DDO, DCK, and DMS pins not as on-chip debug pins but as port pins after external reset, one of the following actions must be taken.**

- **Input a low level to the P05/INTP2/$\overline{\text{DRST}}$ pin.**
- **Set the OCDM0 bit. In this case, take the following actions.**
  **<1> Clear the OCDM0 bit to 0.**
  **<2> Fix the P05/INTP2/$\overline{\text{DRST}}$ pin to low level until <1> is completed.**

**2. The P05/INTP2/$\overline{\text{DRST}}$ pin has an on-chip pull-down resistor. This resistor is disconnected when the OCDM0 flag is cleared to 0.**

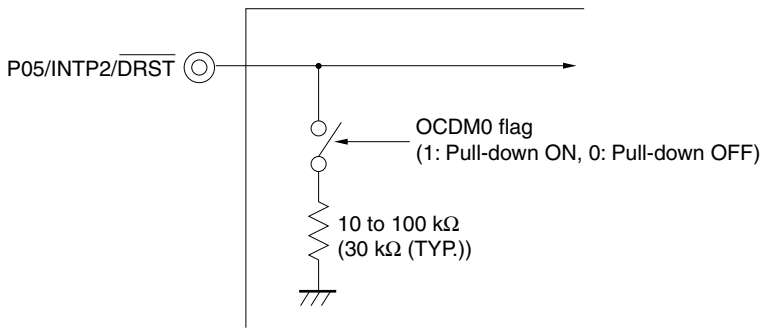


**Table 29-4. Wiring Between V850ES/JE3-L and MINICUBE2**

| Pin Configuration of MINICUBE2 (QB-MINI2) | | | With CSIB0-HS | | With CSIB3-HS | | With UARTA0 | |
|---|---|---|---|---|---|---|---|---|
| Signal Name | I/O | Pin Function | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. |
| SI/RxD | Input | Pin to receive commands and data from V850ES/JE3-L | P41/SOB0 | 29 | P911/SOB3 | 15 | P30/TXDA0 | 45 |
| SO/TxD | Output | Pin to transmit commands and data to V850ES/JE3-L | P40/SIB0 | 28 | P910/SIB3 | 16 | P31/RXDA0 | 32 |
| SCK | Output | Clock output pin for 3-wire serial communication | P42/$\overline{\text{SCKB0}}$ | 30 | P912/$\overline{\text{SCKB3}}$ | 14 | Not needed | – |
| CLK | Output | Pin outputting clock signal to V850ES/JE3-L | Not needed | – | Not needed | – | Not needed | – |
| RESET_OUT | Output | Pin outputting reset signal to V850ES/JE3-L | $\overline{\text{RESET}}$ | 10 | $\overline{\text{RESET}}$ | 10 | $\overline{\text{RESET}}$ | 10 |
| FLMD0 | Output | Output pin to set V850ES/JE3-L to debug mode or programming mode | FLMD0 | 42 | FLMD0 | 42 | FLMD0 | 42 |
| FLMD1 | Output | Output pin to set programming mode | PDL5/FLMD1 | 49 | PDL5/FLMD1 | 49 | PDL5/FLMD1 | 49 |
| HS | Input | Handshake signal for CSI0 + HS communication | PCM0 | 54 | PCM0 | 54 | Not needed | – |
| GND | – | Ground | $V_{SS}$ | 7 | $V_{SS}$ | 7 | $V_{SS}$ | 7 |
| | | | $AV_{SS}$ | 2 | $AV_{SS}$ | 2 | $AV_{SS}$ | 2 |
| | | | $EV_{SS}$ | 25 | $EV_{SS}$ | 25 | $EV_{SS}$ | 25 |
| RESET_IN | Input | Reset input pin on the target system | | | | | | |

**($T_A$ = −40 to +85°C, $V_{DD}$ = $EV_{DD}$ = $AV_{REF0}$, $V_{SS}$ = $EV_{SS}$ = $AV_{SS}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Output voltage, high | $V_{OH1}$ | P02, P03, P05, P30, P31, P40 to P42, P50 to P55, P90, P91, P96, P97, P914, P915 | Per pin $I_{OH}$ = −1.0 mA | Total of all pins −20 mA | $EV_{DD}$ − 1.0 | | $EV_{DD}$ | V |
| | | | Per pin $I_{OH}$ = −100 μA | Total of all pins −2.0 mA | $EV_{DD}$ − 0.5 | | $EV_{DD}$ | V |
| | $V_{OH2}$ | PCM0, PDL5 | Per pin $I_{OH}$ = −1.0 mA | Total of all pins −2 mA | $EV_{DD}$ − 1.0 | | $EV_{DD}$ | V |
| | | | Per pin $I_{OH}$ = −100 μA | Total of all pins −0.2 mA | $EV_{DD}$ − 0.5 | | $EV_{DD}$ | V |
| | $V_{OH3}$ | P70 to P74 | Per pin $I_{OH}$ = −0.4 mA | Total of all pins −2.0 mA | $AV_{REF0}$ − 1.0 | | $AV_{REF0}$ | V |
| | | | Per pin $I_{OH}$ = −100 μA | Total of all pins −0.5 mA | $AV_{REF0}$ − 0.5 | | $AV_{REF0}$ | V |
| Output voltage, low | $V_{OL1}$ | P02, P03, P05, P30, P31, P42, P50 to P55, P96, P97, P914, P915 | Per pin $I_{OL}$ = 1.0 mA | Total of all pins 20 mA | 0 | | 0.4 | V |
| | $V_{OL2}$ | P40, P41, P90, P91 | Per pin $I_{OL}$ = 3.0 mA | | 0 | | 0.4 | V |
| | $V_{OL3}$ | PCM0, PDL5 | Per pin $I_{OL}$ = 1.0 mA | Total of all pins 2 mA | 0 | | 0.4 | V |
| | $V_{OL4}$ | P70 to P74 | Per pin $I_{OL}$ = 0.4 mA | Total of all pins 2.0 mA | 0 | | 0.4 | V |
| Software pull-down resistor[Note] | $R_1$ | P05 | $V_I$ = $V_{DD}$ | | 10 | 20 | 100 | kΩ |

**Note** $\overline{\text{DRST}}$ pin only (controlled by OCDM register)

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

**2.** When the $I_{OH}$ and $I_{OL}$ conditions are not satisfied for a pin but the total value of all pins is satisfied, only that pin does not satisfy the DC characteristics.

# CHAPTER 32 ELECTRICAL SPECIFICATIONS (V850ES/JE3-L) (Target)

## 32.1 Absolute Maximum Ratings

**Absolute Maximum Ratings ($T_A$ = 25°C) (1/2)**

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}$ | −0.5 to +4.6 | V |
| | $EV_{DD}$ | $V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}$ | −0.5 to +4.6 | V |
| | $AV_{REF0}$ | $V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}$ | −0.5 to +4.6 | V |
| | $AV_{REF1}$ | $V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}$ | −0.5 to +4.6 | V |
| | $V_{SS}$ | $V_{SS} = EV_{SS} = AV_{SS}$ | −0.5 to +0.5 | V |
| | $AV_{SS}$ | $V_{SS} = EV_{SS} = AV_{SS}$ | −0.5 to +0.5 | V |
| | $EV_{SS}$ | $V_{SS} = EV_{SS} = AV_{SS}$ | −0.5 to +0.5 | V |
| Input voltage | $V_{I1}$ | P97 to P915, PCM0, PDL5, $\overline{\text{RESET}}$, FLMD0 | −0.5 to $EV_{DD}$ + 0.5 Note 1 | V |
| | $V_{I2}$ | P10 | −0.5 to $AV_{REF1}$ + 0.5 Note 1 | V |
| | $V_{I3}$ | X1 | −0.5 to $V_{DD}$ + 0.5 Note 1 | V |
| | | X2 | −0.5 to $V_{RO}$ Note 2 + 0.5 Note 1 | |
| | $V_{I4}$ | P02 to P06, P30 to P35, P38, P39, P40 to P42, P50 to P55, P90 to P94, P96 | −0.5 to +6.0 | V |
| | $V_{I5}$ | XT1, XT2 | −0.5 to $V_{RO}$ Note 2 + 0.5 | V |
| Analog input voltage | $V_{IAN}$ | P70 to P79 | −0.5 to $AV_{REF0}$ + 0.5 Note 1 | V |

**Notes 1.** Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

**2.** On-chip regulator output voltage

**Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to $V_{DD}$, $V_{CC}$, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.**

**2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**The ratings and conditions indicated for DC characteristics, AC characteristics, and operating conditions represent the quality assurance range during normal operation.**

**Remark** Unless specified otherwise, the ratings of alternate-function pins are the same as those of port pins.

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| Symbol | Name | Unit | Page |
|---|---|---|---|
| INTR9H | External interrupt rising edge specification register 9H | INTC | 745 |
| ISPR | In-service priority register | INTC | 733 |
| KRIC | Interrupt control register | INTC | 729 |
| KRM | Key return mode register | KR | 752 |
| LOCKR | Lock register | CG | 193 |
| LVIIC | Interrupt control register | INTC | 729 |
| LVIM | Low voltage detection register | LVI | 805 |
| LVIS | Low voltage detection level select register | LVI | 806 |
| NFC | Noise elimination control register | INTC | 747 |
| OCDM | On-chip debug mode register | DCU | 845 |
| OCKS0 | IIC division clock select register 0 | $I^2C$ | 635 |
| OCKS1 | IIC division clock select register 1 | $I^2C$ | 635 |
| OSTS | Oscillation stabilization time select register | Standby | 758 |
| P0 | Port 0 register | Port | 100 |
| P1 | Port 1 register | Port | 105 |
| P3 | Port 3 register | Port | 107 |
| P3H | Port 3 register H | Port | 107 |
| P3L | Port 3 register L | Port | 107 |
| P4 | Port 4 register | Port | 114 |
| P5 | Port 5 register | Port | 116 |
| P7H | Port 7 register H | Port | 122 |
| P7L | Port 7 register L | Port | 122 |
| P9 | Port 9 register | Port | 125 |
| P9H | Port 9 register H | Port | 125 |
| P9L | Port 9 register L | Port | 125 |
| PC | Program counter | CPU | 52 |
| PCC | Processor clock control register | CG | 185 |
| PCM | Port CM register | Port | 136 |
| PDL | Port DL register | Port | 138 |
| PDLL | Port DL register L | Port | 138 |
| PF0 | Port 0 function register | Port | 104 |
| PF3 | Port 3 function register | Port | 113 |
| PF3H | Port 3 function register H | Port | 113 |
| PF3L | Port 3 function register L | Port | 113 |
| PF4 | Port 4 function register | Port | 115 |
| PF5 | Port 5 function register | Port | 120 |
| PF9 | Port 9 function register | Port | 135 |
| PF9H | Port 9 function register H | Port | 135 |
| PF9L | Port 9 function register L | Port | 135 |
| PFC0 | Port 0 function control register | Port | 103 |
| PFC3 | Port 3 function control register | Port | 111 |
| PFC3H | Port 3 function control register H | Port | 111 |
| PFC3L | Port 3 function control register L | Port | 111 |

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| Mnemonic | Operand | Opcode | Operation | Execution Clock | | | Flags | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | i | r | l | CY | OV | S | Z | SAT |
| SUB | reg1,reg2 | rrrrr001101RRRRR | GR[reg2]←GR[reg2]–GR[reg1] | 1 | 1 | 1 | × | × | × | × | |
| SUBR | reg1,reg2 | rrrrr001100RRRRR | GR[reg2]←GR[reg1]–GR[reg2] | 1 | 1 | 1 | × | × | × | × | |
| SWITCH | reg1 | 00000000010RRRRR | adr←(PC+2) + (GR [reg1] logically shift left by 1)<br>PC←(PC+2) + (sign-extend<br>(Load-memory (adr,Halfword))<br>logically shift left by 1 | 5 | 5 | 5 | | | | | |
| SXB | reg1 | 00000000101RRRRR | GR[reg1]←sign-extend<br>(GR[reg1] (7 : 0)) | 1 | 1 | 1 | | | | | |
| SXH | reg1 | 00000000111RRRRR | GR[reg1]←sign-extend<br>(GR[reg1] (15 : 0)) | 1 | 1 | 1 | | | | | |
| TRAP | vector | 0000011111iiiii<br>0000000100000000 | EIPC ←PC+4 (Restored PC)<br>EIPSW ←PSW<br>ECR.EICC ←Interrupt code<br>PSW.EP ←1<br>PSW.ID ←1<br>PC ←00000040H<br>(when vector is 00H to 0FH)<br>00000050H<br>(when vector is 10H to 1FH) | 3 | 3 | 3 | | | | | |
| TST | reg1,reg2 | rrrrr001011RRRRR | result←GR[reg2] AND GR[reg1] | 1 | 1 | 1 | | 0 | × | × | |
| TST1 | bit#3,disp16[reg1] | 11bbb111110RRRRR<br>ddddddddddddddd | adr←GR[reg1]+sign-extend(disp16)<br>Z flag←Not (Load-memory-bit (adr,bit#3)) | 3<br>Note 3 | 3<br>Note 3 | 3<br>Note 3 | | | | × | |
| | reg2, [reg1] | rrrrr111111RRRRR<br>0000000011100110 | adr←GR[reg1]<br>Z flag←Not (Load-memory-bit (adr,reg2)) | 3<br>Note 3 | 3<br>Note 3 | 3<br>Note 3 | | | | × | |
| XOR | reg1,reg2 | rrrrr001001RRRRR | GR[reg2]←GR[reg2] XOR GR[reg1] | 1 | 1 | 1 | | 0 | × | × | |
| XORI | imm16,reg1,reg2 | rrrrr110101RRRRR<br>iiiiiiiiiiiiiiii | GR[reg2]←GR[reg1] XOR zero-extend (imm16) | 1 | 1 | 1 | | 0 | × | × | |
| ZXB | reg1 | 00000000100RRRRR | GR[reg1]←zero-extend (GR[reg1] (7 : 0)) | 1 | 1 | 1 | | | | | |
| ZXH | reg1 | 00000000110RRRRR | GR[reg1]←zero-extend (GR[reg1] (15 : 0)) | 1 | 1 | 1 | | | | | |

**Notes 1.** ddddddddd: Higher 8 bits of disp9.

**2.** 3 if there is an instruction that rewrites the contents of the PSW immediately before.

**3.** If there is no wait state (3 + the number of read access wait states).

**4.** n is the total number of list12 load registers. (According to the number of wait states. Also, if there are no wait states, n is the total number of list12 registers. If n = 0, same operation as when n = 1)

**5.** RRRRR: other than 00000.

**6.** The lower halfword data only are valid.

**7.** ddddddddddddddddddddd: The higher 21 bits of disp22.

**8.** ddddddddddddddd: The higher 15 bits of disp16.

**9.** According to the number of wait states (1 if there are no wait states).

**10.** b: bit 0 of disp16.

**11.** According to the number of wait states (2 if there are no wait states).