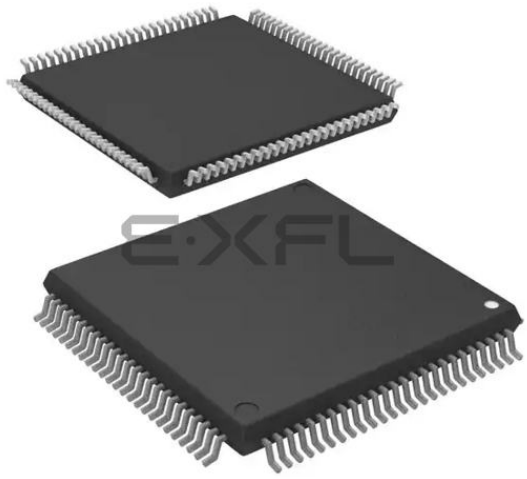
Renesas Electronics America Inc - UPD70F3841GC-UEU-AX Datasheet



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Applications of "Embedded - Microcontrollers"

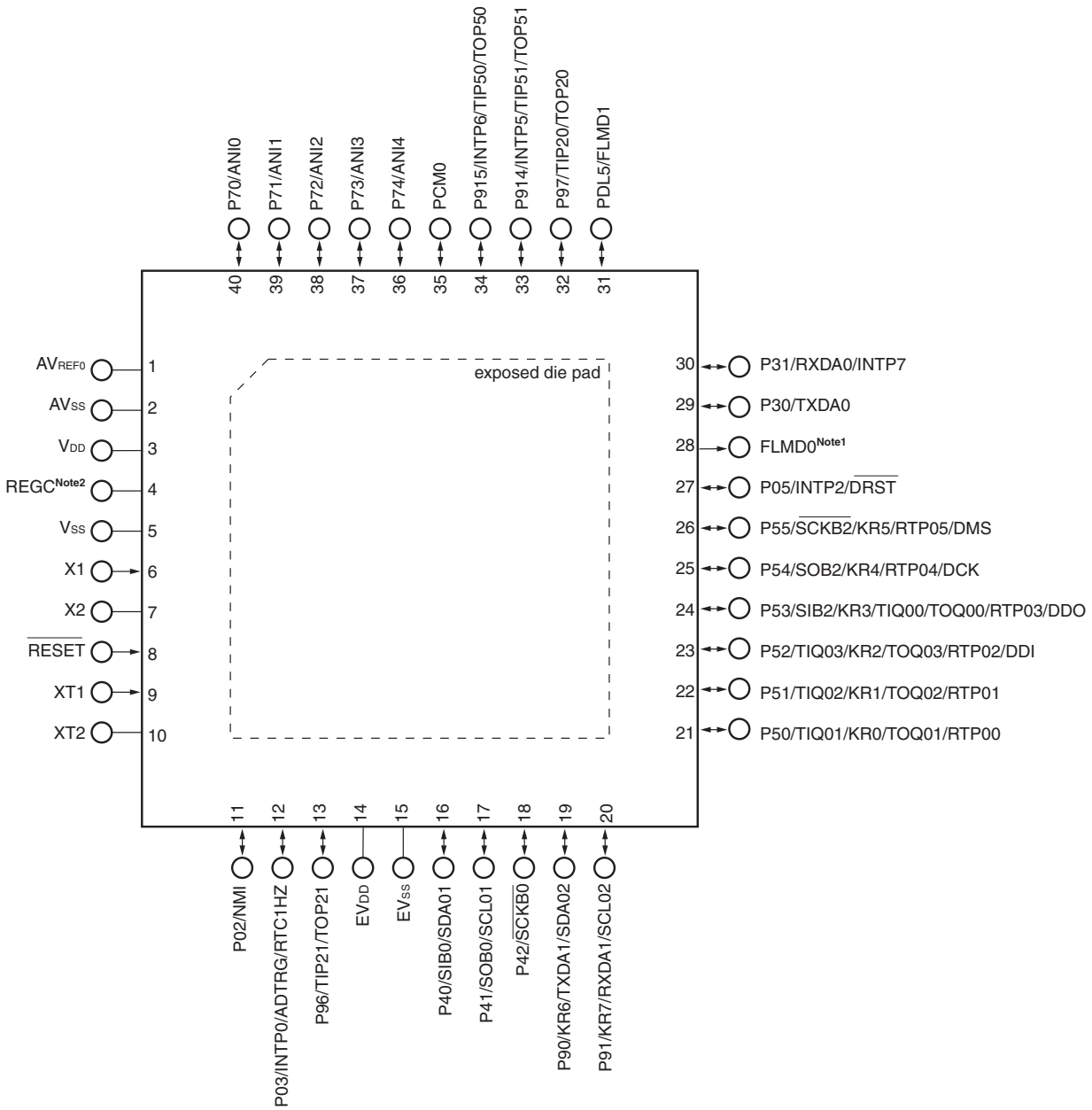
Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	83
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3841gc-ueu-ax

1.5 Pin Configuration (Top View)

- V850ES/JC3-L

  40-pin plastic WQFN (6 × 6)

μPD70F3797K8-4B4-AX μPD70F3798K8-4B4-AX μPD70F3799K8-4B4-AX
μPD70F3800K8-4B4-AX μPD70F3838K8-4B4-AX



Notes 1. The FLMD0 pin is used in flash programming. Connect this pin to V_{SS} in the normal operation mode.

2. Connect the REGC pin to V_{SS} via a 4.7 μF (recommended value) capacitor.

(2/2)

Pin	Alternate Function	Pin No.			I/O Circuit Type	Recommended Connection of Unused Pin
		JC3L (40)	JC3L (48)	JE3L		
P70 to P74	ANI0 to ANI4	40 to 36	48 to 44	64 to 60	11-G	Input: Independently connect to AV_{REF0} or AV_{SS} via a resistor. Output: Leave open.
P75	ANI5	–	43	59		
P76 to P79	ANI6 to ANI9	–	–	58 to 55		
P90	KR6/TDXA1/SDA02	19	23	31	10-D	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P91	KR7/RXDA1/SCL02	20	24	32		
P92	TIP41/TOP41/TXDA4	–	–	33		
P93	TIP40/TOP40/RXDA4	–	–	34		
P94	TIP31/TOP31/TXDA5	–	–	21		
P96	TIP21/TOP21	13	15	22		
P97	SIB1/TIP20/TOP20	–	38	50		
	TIP20/TOP20	32	–	–		
P98	SOB1	–	39	51	10-G	
P99	$\overline{SCKB1}$	–	36	48	10-D	
P910	SIB3	–	–	16		
P911	SOB3	–	–	15	10-G	
P912	$\overline{SCKB3}$	–	–	14	10-D	
P913	INTP4	–	–	13		
P914	INTP5/TIP51/TOP51	33	40	52		
P915	INTP6/TIP50/TOP50	34	41	53		
PCM0	–	35	42	54	5	
PDL5	FLMD1	31	37	49		
AV_{REF0}	–	1	1	1	–	Directly connect to V_{DD} and always supply power.
AV_{REF1}	–	–	4	4	–	
AV_{SS}	–	2	2	2	–	Directly connect to V_{SS} and always supply power.
EV_{DD}	–	14	16	24	–	Directly connect to V_{DD} and always supply power.
EV_{SS}	–	15	17	25	–	Directly connect to V_{SS} and always supply power.
FLMD0	–	28	32	42	–	Directly connect to V_{SS} in a mode other than the flash memory programming mode.
REGC	–	4	6	6	–	Connection of regulator output stabilization capacitance (4.7 μF (recommended value))
$\overline{RESET}$	–	8	10	10	2	–
V_{DD}	–	3	5	5	–	–
V_{SS}	–	5	7	7	–	–
X1	–	6	8	8	–	–
X2	–	7	9	9	–	–
XT1	–	9	11	11	16-C	Connect to V_{SS}.
XT2	–	10	12	12	16-C	Leave open.

Remark JC3L (40): V850ES/JC3-L (40-pin products)
JC3L (48): V850ES/JC3-L (48-pin products)
JE3L : V850ES/JE3-L

(3) Port 4 mode control register (PMC4)

After reset: 00H R/W Address: FFFFF448H

	7	6	5	4	3	2	1	0
PMC4	0	0	0	0	0	PMC42	PMC41	PMC40

PMC42	Specification of pin operation
0	I/O port (P42)
1	$\overline{\text{SCKB0}}$ I/O

PMC41	Specification of pin operation
0	I/O port (P41)
1	SOB0 output/SCL01 I/O

PMC40	Specification of pin operation
0	I/O port (P40)
1	SIB0 input/SDA01 I/O

(4) Port 4 function control register (PFC4)

After reset: 00H R/W Address: FFFFF468H

	7	6	5	4	3	2	1	0
PFC4	0	0	0	0	0	0	PFC41	PFC40

PFC41	Specification of P41 pin alternate function
0	SOB0 output
1	SCL01 I/O

PFC40	Specification of P40 pin alternate function
0	SIB0 input
1	SDA01 I/O

(5) Port 4 function register (PF4)

After reset: 00H R/W Address: FFFFFC68H

	7	6	5	4	3	2	1	0
PF4	0	0	0	0	0	PF42	PF41	PF40

PF4n	Specification of normal output (CMOS output) or N-ch open-drain output (n = 0 to 2)
0	Normal output (CMOS output)
1	N-ch open-drain output

Caution When an output pin is pulled up to EV_{DD} or higher, be sure to set the PF4n bit to 1.

(1) Port DL register (PDL)

After reset: 0000H (output latch) R/W Address: PDL FFFFF004H, PDLL FFFFF004H

	15	14	13	12	11	10	9	8
PDL	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
(PDLL)	0	0	PDL5	0	0	0	0	0

PDL5	Output data control (in output mode)
0	Outputs 0
1	Outputs 1

Remark The PDL register can be read or written in 16-bit units.
However, when using the lower 8 bits as the PDLL register, PDL can be read or written in 8-bit or 1-bit units.

(2) Port DL mode register (PMDL)

After reset: FFFFH R/W Address: PMDL FFFFF024H, PMDLL FFFFF024H

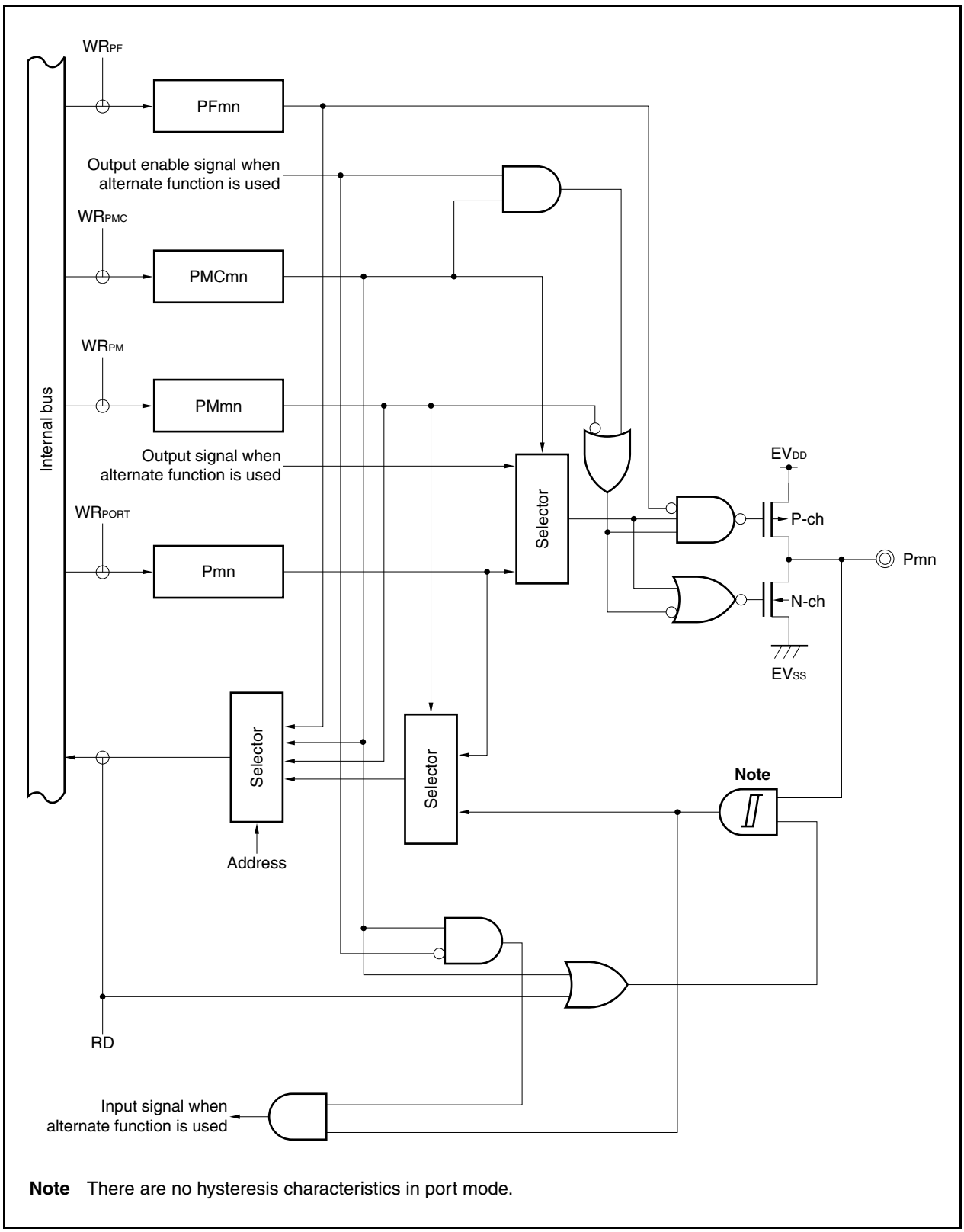
	15	14	13	12	11	10	9	8
PMDL	1	1	1	1	1	1	1	1

	7	6	5	4	3	2	1	0
(PMDLL)	1	1	PMDL5	1	1	1	1	1

PMDL5	I/O mode control
0	Output mode
1	Input mode

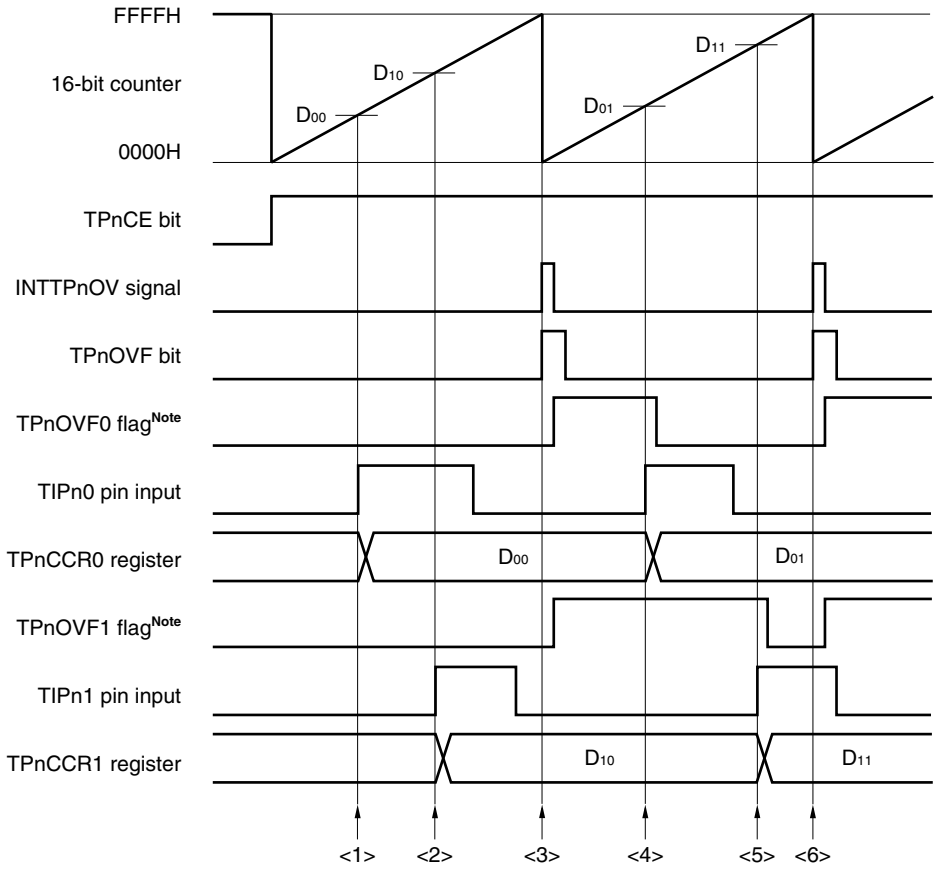
Remark The PMDL register can be read or written in 16-bit units.
However, when using the lower 8 bits as the PMDLL register, PMDL can be read or written in 8-bit or 1-bit units.

Figure 4-8. Block Diagram of Type E-3



Note There are no hysteresis characteristics in port mode.

Figure 6-61. Example of Resolving Problem When Two Capture Registers Are Used By Using Overflow Interrupt



Note The TPnOVF0 and TPnOVF1 flags are set on the internal RAM by software.

<1> The TPnCCR0 register is read (the default value of the TIPn0 pin input is set).

<2> The TPnCCR1 register is read (the default value of the TIPn1 pin input is set).

<3> An overflow occurs. The TPnOVF0 and TPnOVF1 flags are set to 1 in the overflow interrupt servicing, and the TPnOVF bit is cleared to 0.

<4> The TPnCCR0 register is read.
The TPnOVF0 flag is read. The TPnOVF0 flag is 1, so it is cleared to 0.
Because the TPnOVF0 flag was 1, the pulse width can be calculated by (10000H + D_{01} − D_{00}).

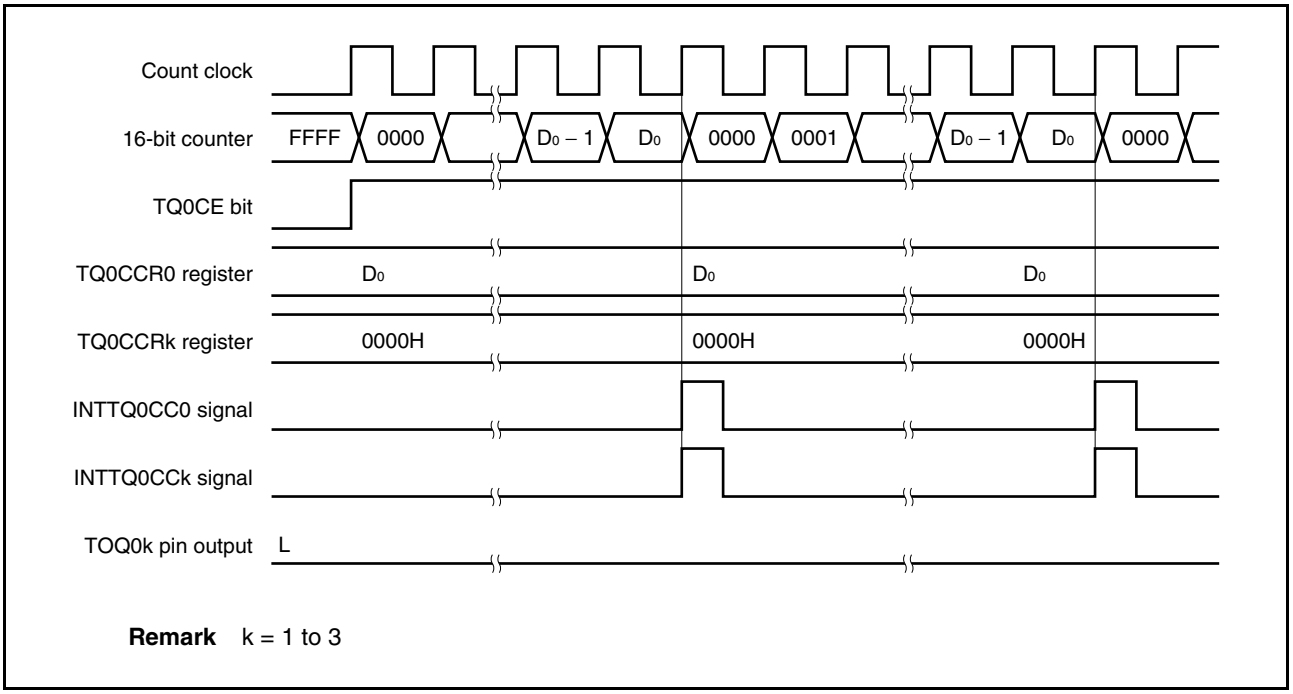
<5> The TPnCCR1 register is read.
The TPnOVF1 flag is read. The TPnOVF1 flag is 1, so it is cleared to 0 (the TPnOVF0 flag was cleared in <4>; the TPnOVF1 flag remained 1).
Because the TPnOVF1 flag is 1, the pulse width can be calculated by (10000H + D_{11} − D_{10}) (correct).

<6> Same as <3>.

(b) Outputting a 0% or 100% PWM waveform

To output a 0% waveform, clear the TQ0CCRk register to 0000H.

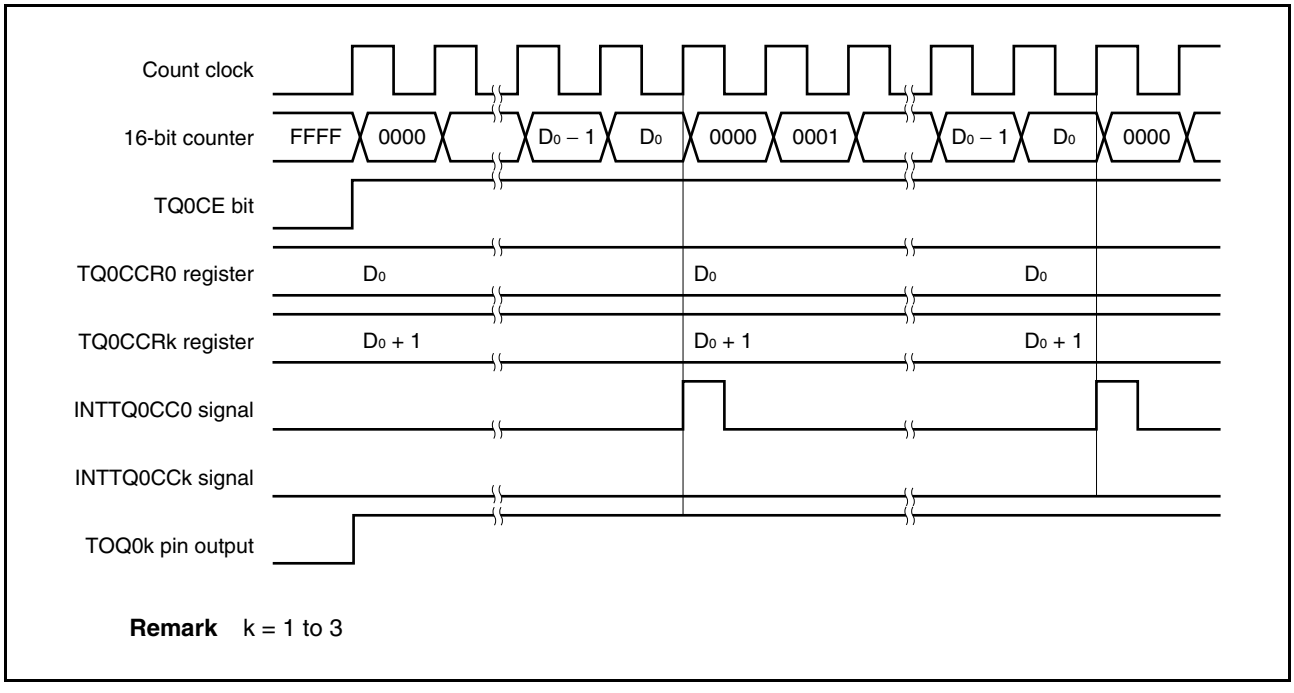
Figure 7-49. Outputting 0% PWM Waveform



Remark k = 1 to 3

To output a 100% waveform, set the value of TQ0CCR0 register + 1 to the TQ0CCRk register. If the value of the TQ0CCR0 register is FFFFH, a 100% waveform cannot be output.

Figure 7-50. Outputting 100% PWM Waveform



Remark k = 1 to 3

(3) UARTAn control register 2 (UAnCTL2)

The UAnCTL2 register is an 8-bit register that selects the baud rate (serial transfer speed) clock of UARTAn.

The baud rate clock is generated by dividing the serial clock specified by this register by two.

This register can be read or written in 8-bit units.

Reset sets this register to FFH.

Caution Either clear the UAnCTL0.UAnPWR bit to 0, or clear the UAnTXE and UAnRXE bits to 0, 0, before rewriting the UAnCTL2 register.

After reset FFH R/W Address: UA0CTL2 FFFFFA02H, UA1CTL2 FFFFFA12H, UA2CTL2 FFFFFA22H

	7	6	5	4	3	2	1	0
UAnCTL2	UAnBRS7	UAnBRS6	UAnBRS5	UAnBRS4	UAnBRS3	UAnBRS2	UAnBRS1	UAnBRS0

UAn BRS7	UAn BRS6	UAn BRS5	UAn BRS4	UAn BRS3	UAn BRS2	UAn BRS1	UAn BRS0	Default (k)	Serial clock
0	0	0	0	0	0	×	×	×	Setting prohibited
0	0	0	0	0	1	0	0	4	$f_{UCLK}/4$
0	0	0	0	0	1	0	1	5	$f_{UCLK}/5$
0	0	0	0	0	1	1	0	6	$f_{UCLK}/6$
:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	0	252	$f_{UCLK}/252$
1	1	1	1	1	1	0	1	253	$f_{UCLK}/253$
1	1	1	1	1	1	1	0	254	$f_{UCLK}/254$
1	1	1	1	1	1	1	1	255	$f_{UCLK}/255$

Remark f_{UCLK}: Clock frequency selected by the UAnCTL1.UAnCKS3 to UAnCTL1.UAnCKS0 bits

To set the baud rate, perform the following calculation for setting the UAnCTL1 and UAnCTL2 registers (when using the internal clock).

<1> Set k to fxx/(2 × target baud rate) and m to 0.
<2> If k is 256 or greater (k ≥ 256), reduce k to half (k/2) and increment m by 1 (m + 1).
<3> Repeat Step <2> until k becomes less than 256 (k < 256).
<4> Round off the first decimal point of k to the nearest whole number.
If k is 256 after round-off, reduce k to half (k/2) and increment m by 1 (m + 1) to obtain k = 128.
<5> Set the value of m to the UAnCTL1 register and the value of k to the UAnCTL2 register.

Example: When fxx = 20 MHz and target baud rate = 153,600 bps
<1> k = 20,000,000/(2 × 153,600) = 65.10…, m = 0
<2>, <3> k = 65.10… < 256, m = 0
<4> Set value of UAnCTL2 register: k = 65 = 41H, set value of UAnCTL1 register: m = 0

Actual baud rate = 20,000,000/(2 × 65)
= 153,846 [bps]

Baud rate error = {20,000,000/(2 × 65 × 153,600) − 1} × 100
= 0.160 [%]

Representative examples of baud rate settings are shown below.

Table 15-6. Baud Rate Generator Setting Data

Baud Rate (bps)	fxx = 20 MHz			fxx = 16 MHz			fxx = 10 MHz		
	UAnCTL1	UAnCTL2	ERR (%)	UAnCTL1	UAnCTL2	ERR (%)	UAnCTL1	UAnCTL2	ERR (%)
300	08H	82H	0.16	07H	D0H	0.16	07H	82H	0.16
600	07H	82H	0.16	06H	D0H	0.16	06H	82H	0.16
1200	06H	82H	0.16	05H	D0H	0.16	05H	82H	0.16
2400	05H	82H	0.16	04H	D0H	0.16	04H	82H	0.16
4800	04H	82H	0.16	03H	D0H	0.16	03H	82H	0.16
9600	03H	82H	0.16	02H	D0H	0.16	02H	82H	0.16
19200	02H	82H	0.16	01H	D0H	0.16	01H	82H	0.16
31250	01H	A0H	0	01H	80H	0	00H	A0H	0
38400	01H	82H	0.16	00H	D0H	0.16	00H	82H	0.16
76800	00H	82H	0.16	00H	68H	0.16	00H	41H	0.16
153600	00H	41H	0.16	00H	34H	0.16	00H	21H	−1.36
312500	00H	20H	0	00H	1AH	−1.54	00H	10H	0
625000	00H	10H	0	00H	0DH	−1.54	00H	08H	0

Remark fxx: Main clock frequency
ERR: Baud rate error (%)

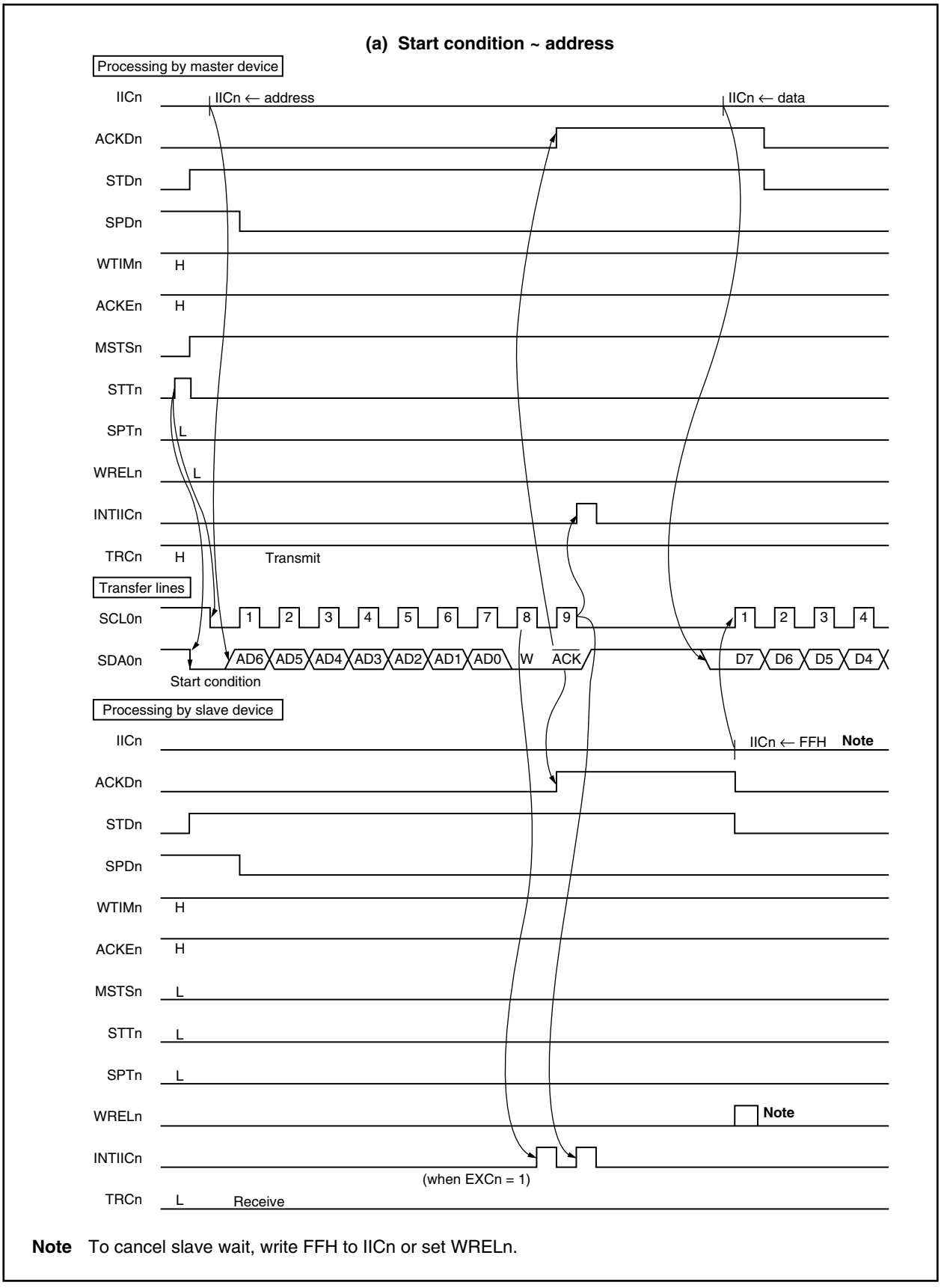
16.6.9 Continuous transfer mode (master mode, transmission/reception mode)

MSB first (CBnCTL0.CBnDIR bit = 0), communication type 1 (CBnCTL1.CBnCKP and CBnCTL1.CBnDAP bits = 00), communication clock (f_{CCLK}) = f_{XX}/2 (CBnCTL1.CBnCKS2 to CBnCTL1.CBnCKS0 bits = 000), transfer data length = 8 bits (CBnCTL2.CBnCL3 to CBnCTL2.CBnCL0 bits = 0000)

The flowchart in Figure 16-21 shows the operation where the specified number of transmit/receive data items are transmitted are received in the master mode. Operations are repeated until all the specified data items are transmitted/received. If an overrun error occurs, however, transfer ends. Perform error processing as necessary. For details about the overrun error, see **16.6.13 Reception errors**.

The operation timing in Figure 16-22 shows a case where no error occurred.

Figure 17-23. Example of Master to Slave Communication (When 9-Clock Wait Is Selected for Both Master and Slave) (1/3)



Note To cancel slave wait, write FFH to IICn or set WRELn.

(8) Bus arbitration for CPU

Because the DMA controller is a higher priority bus master than the CPU, a CPU access that takes place during DMA transfer is held pending until the DMA transfer cycle is completed and the bus is released to the CPU.

However, the CPU can access the internal ROM and the internal RAM for which DMA transfer is not being executed.

- The CPU can access the internal ROM when DMA transfer is being executed between the on-chip peripheral I/O and the internal RAM.

(9) Registers/bits that must not be rewritten during DMA transfer

Set up the following registers during one of the periods below when a DMA transfer is not under execution (n = 0 to 3).

[Registers]

- DSAnH, DSAnL, DDAnH, DDAnL, DBCn, and DADCn registers
- DTFRn.IFCn5 to DTFRn.IFCn0 bits

[Timing of setting]

- Period from after reset to start of the first DMA transfer
- Period from after channel initialization to start of DMA transfer
- Period from after completion of DMA transfer (TCn bit = 1) to start of the next DMA transfer

(10) Be sure to set the following register bits to 0 (n = 0 to 3).

- Bits 14 to 10 of DSAnH register
- Bits 14 to 10 of DDAnH register
- Bits 15, 13 to 8, and 3 to 0 of DADCn register
- Bits 6 to 3 of DCHCn register

(11) DMA start factor

Do not start multiple DMA channels with the same start factor. If multiple channels are started with the same factor, DMA for which a channel has already been set may starts or a DMA channel with a lower priority may be acknowledged before a DMA channel with a higher priority. The operation cannot be guaranteed in this case.

(2) External interrupt falling, rising edge specification register 3 (INTF3, INTR3)

The INTF3 and INTR3 registers are 8-bit registers that specify detection of the falling and rising edges of the external interrupt pin (INTP7).

These registers can be read or written in 8-bit or 1-bit units.

Reset sets these registers to 00H.

Cautions 1. When switching from the port function to the external interrupt function (alternate function), an edge might be detected. Therefore, set the INTF31 and INTR31 bits to 00, and then specify the external interrupt function (PMC3.PMC31 bit = 1).

When switching from the external interrupt function to the port function, an edge might be detected as well. Therefore, set the INTF31 and INTR31 bits to 00, and then specify the port function (PMC3.PMC31 bit = 0).

2. The INTP7 pin and RXDA0 pin are alternate-function pins. When using the pin as the RXDA0 pin, disable edge detection for the INTP7 alternate-function pin (clear the INTF3.INTF31 bit and the INRT3.INTR31 bit to 0). When using the pin as the INTP7 pin, stop UARTA0 reception (clear the UA0CTL0.UA0RXE bit to 0).

After reset: 00H R/W Address: INTF3 FFFFFC06H, INTR3 FFFFFC26H

	7	6	5	4	3	2	1	0
INTF3	0	0	0	0	0	0	INTF31	0
							INTP7	
INTR3	0	0	0	0	0	0	INTR31	0
							INTP7	

Remark For how to specify a valid edge, see **Table 19-5**.

Table 19-5. Valid Edge Specification

INTF31	INTR31	Valid Edge Specification
0	0	No edge detected
0	1	Rising edge
1	0	Falling edge
1	1	Both rising and falling edges

Caution Be sure to clear the INTF31 and INTR31 bits to 00 when these registers are not used for the INTP7 pin.

20.2 Pin Functions

The key input pins that are used as key interrupts are also used for the other functions shown in **Table 20-2**. To use these pins as key interrupts, this function must be specified by setting the relevant registers (see **Table 4-17 Settings When Pins Are Used for Alternate Functions**).

Table 20-2. Pin Functions

Pin No.	Port Function	Key Input Function	Other Functions
37	P50	KR0	P50/TIQ01/TOQ01/RTP00
38	P51	KR1	P51/TIQ02/TOQ02/RTP01
39	P52	KR2	P52/TIQ03/TOQ03/RTP02/DDI
40	P53	KR3	P53/SIB2/TIQ00/TOQ00/RTP03/DDO
41	P54	KR4	P54/SOB2/RTP04/DCK
42	P55	KR5	P55/$\overline{\text{SCKB2}}$/RTP05/DMS
61	P90	KR6	P90/A0/TXDA1/SDA02
62	P91	KR7	P91/A1/RXDA1/SCL02

20.3 Registers

(1) Key return mode register (KRM)

The KRM register controls the KR0 to KR7 signals by using the KRM0 to KRM7 bits.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF300H

	7	6	5	4	3	2	1	0
KRM	KRM7	KRM6	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0

KRMn	Control of key return mode
0	Do not detect key return signal
1	Detect key return signal

Caution Clear the KRM register to 00H before rewriting it.

Figure 22-2. Timing of Reset Operation by $\overline{\text{RESET}}$ Pin Input

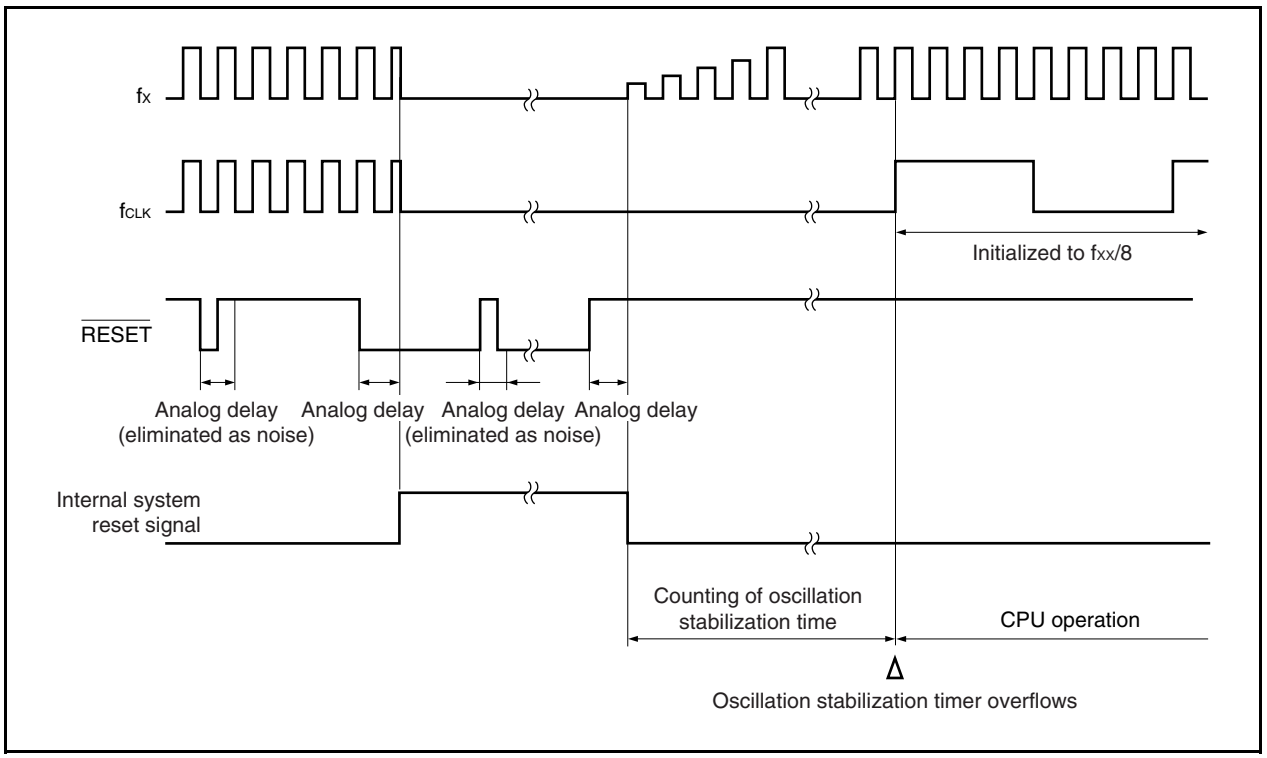
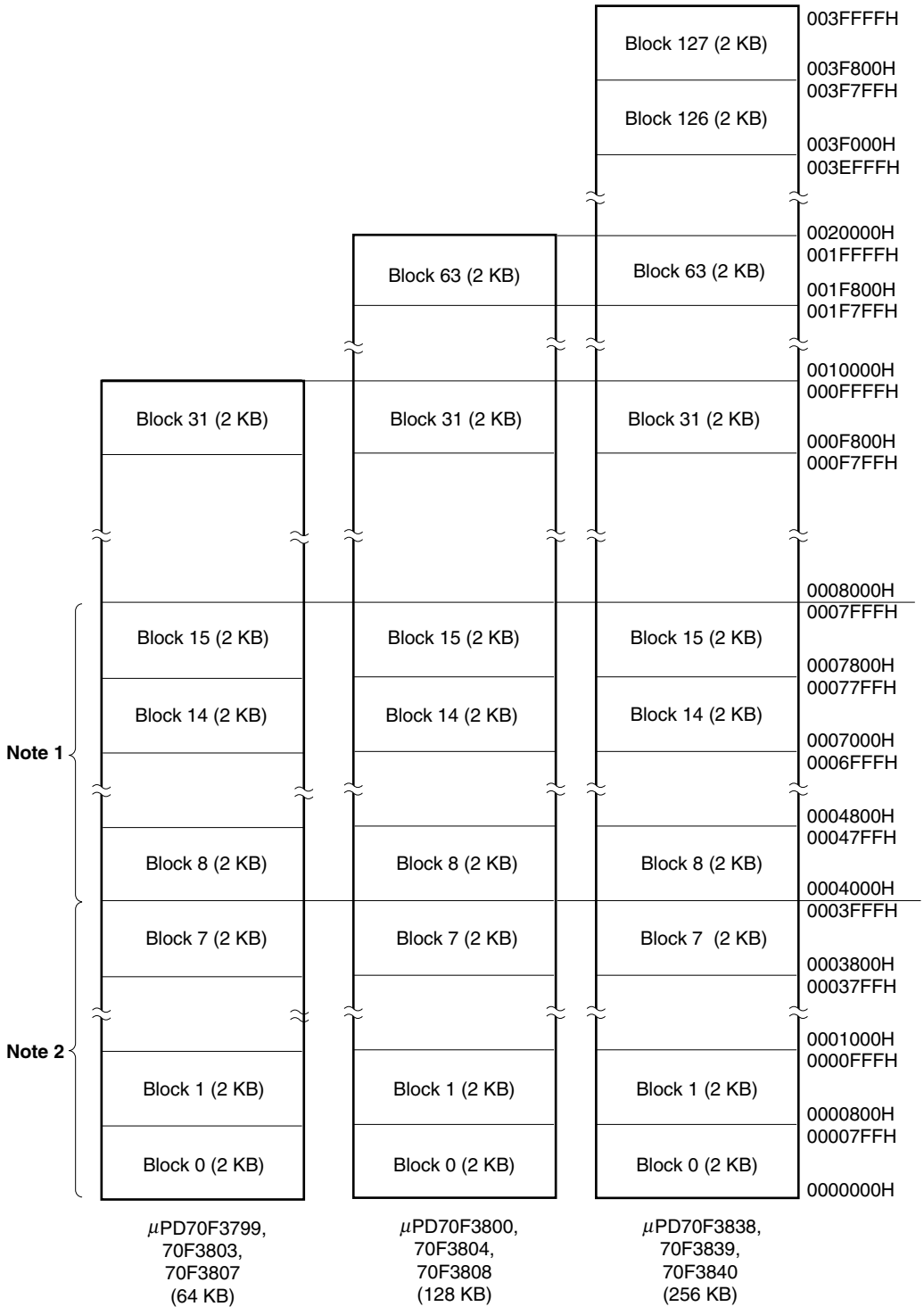


Figure 28-1. Flash Memory Mapping (2/2)



Notes 1. Area to be replaced with the boot area by the boot swap function

2. Boot area

29.2.2 Mask function

Only reset signals can be masked.

The maskable signals in the debugger (ID850QB) and the corresponding V850ES/JC3-L and V850ES/JE3-L functions are listed below.

Table 29-5. Mask Functions

Maskable Signals in ID850QB	Corresponding V850ES/JC3-L and V850ES/JE3-L Functions
NMI0	–
NMI1	–
NMI2	–
STOP	–
HOLD	–
RESET	Reset signal generation by $\overline{\text{RESET}}$ pin input
WAIT	–

30.8 Peripheral Function Characteristics

30.8.1 Interrupt timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.2 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI high-level width	t_{WNIH}		500		ns
NMI low-level width	t_{WNIL}		500		ns
INTPn[Note] high-level width	t_{WITH}	n = 0, 2, 5 to 7	500		ns
INTPn[Note] low-level width	t_{WITL}	n = 0, 2, 5 to 7	500		ns

Note The characteristics of INTPn is the same as the $\overline{DRST}$ pin (P05/INTP2/$\overline{DRST}$).

Remark The NMI and INTPn pins have the analog noise elimination function (n = 0, 2, 5 to 7).

30.8.2 Key return timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.2 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
KRn high-level width	t_{WKRH}		500		ns
KRn low-level width	t_{WKRL}		500		ns

Remarks 1. n = 0 to 7

2. The KRn pin has an analog noise elimination function.

30.8.3 Timer timing

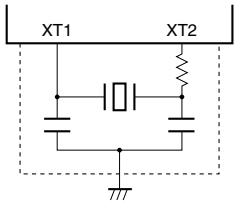
(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.2 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TI high-level width	t_{TIH}	TIP20, TIP21, TIP50, TIP51, TIQ00 to TIQ03	2T + 20		ns
TI low-level width	t_{TIL}		2T + 20		ns

Remark T = 1/fxx

31.4.2 Subclock oscillator characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = 2.2 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Resonator	Circuit Example	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2				10	s

Notes 1. The oscillation frequency shown above indicates only oscillator characteristics. Use the V850ES/JC3-L (48-pin) so that the internal operation conditions do not exceed the ratings shown in **AC Characteristics**, **DC Characteristics**, and operating conditions.

2. Time required from when V_{DD} reaches the oscillation voltage range (2.2 V (MIN.)) to when the crystal resonator stabilizes.

Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subclock oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the main clock oscillator.
Particular care is therefore required with the wiring method when the subclock is used.

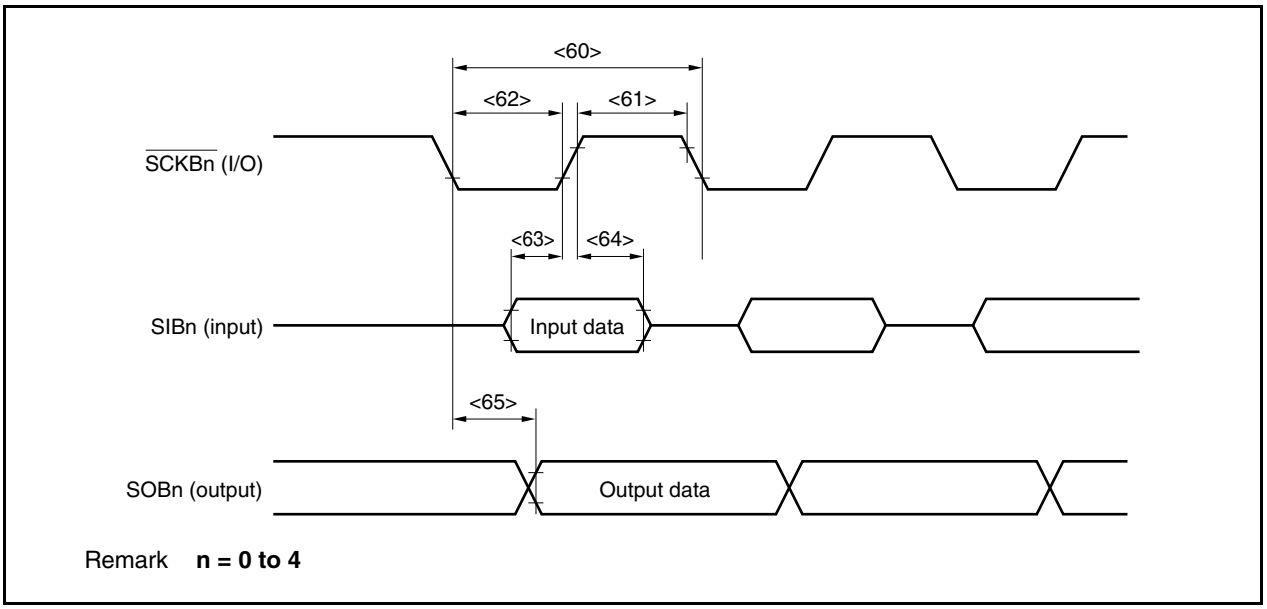
3. For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

(2) Slave mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCY2}	<60>	2.7 V ≤ V_{DD} ≤ 3.6 V	125		ns
			2.2 V ≤ V_{DD} < 2.7 V	800		ns
$\overline{SCKBn}$ high-level width	t_{KH2}	<61>	2.2 V ≤ V_{DD} ≤ 3.6 V	54.5		ns
$\overline{SCKBn}$ low-level width	t_{KL2}	<62>	2.2 V ≤ V_{DD} ≤ 3.6 V	54.5		ns
SIBn setup time (to $\overline{SCKBn}$↑)	t_{SIK2}	<63>	2.7 V ≤ V_{DD} ≤ 3.6 V	27		ns
			2.2 V ≤ V_{DD} < 2.7 V	100		ns
SIBn hold time (from $\overline{SCKBn}$↑)	t_{KSI2}	<64>	2.7 V ≤ V_{DD} ≤ 3.6 V	27		ns
			2.2 V ≤ V_{DD} < 2.7 V	100		ns
Delay time from $\overline{SCKBn}$↓ to SOBn output	t_{KSO2}	<65>	2.7 V ≤ V_{DD} ≤ 3.6 V		27	ns
			2.2 V ≤ V_{DD} < 2.7 V		95	ns

Remark n = 0 to 4



Remark **n = 0 to 4**