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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	83
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3842f1-cah-a

CHAPTER 1 INTRODUCTION

The V850ES/JC3-L and V850ES/JE3-L are one of the products in the Renesas Electronics V850 single-chip microcontroller series designed for low-power operation for real-time control applications.

1.1 General

The V850ES/JC3-L and V850ES/JE3-L are 32-bit single-chip microcontrollers that include the V850ES CPU core and peripheral functions such as ROM/RAM, timer/counters, serial interfaces, an A/D converter, a D/A converter.

In addition to high real-time response characteristics and 1-clock-pitch basic instructions, the The V850ES/JC3-L and V850ES/JE3-L feature multiply instructions, saturated operation instructions, bit manipulation instructions, etc., realized by a hardware multiplier, as optimum instructions for digital servo control applications. Moreover, as a real-time control system, the V850ES/JC3-L and V850ES/JE3-L enable an extremely high cost-performance for applications that require super low power consumption, such as PC peripheral device, ECR peripheral device, and industrial instrument.

1.3 Application Fields

Digital cameras, electrical power meters, mobile terminals, digital home electronics, other consumer devices

.

1.4 Ordering Information

1.4.1 V850ES/JC3-L

Part Number	Package	Internal Flash Memory
μPD70F3797K8-4B4-AX	40-pin plastic WQFN (6 × 6)	16 KB
μPD70F3798K8-4B4-AX	40-pin plastic WQFN (6 × 6)	32 KB
μPD70F3799K8-4B4-AX	40-pin plastic WQFN (6 × 6)	64 KB
μPD70F3800K8-4B4-AX	40-pin plastic WQFN (6 × 6)	128 KB
μPD70F3838K8-4B4-AX	40-pin plastic WQFN (6 × 6)	256 KB
μPD70F3801GA-GAM-AX	48-pin plastic LQFP (fine pitch) (7 × 7)	16 KB
μPD70F3802GA-GAM-AX	48-pin plastic LQFP (fine pitch) (7 × 7)	32 KB
μPD70F3803GA-GAM-AX	48-pin plastic LQFP (fine pitch) (7 × 7)	64 KB
μPD70F3804GA-GAM-AX	48-pin plastic LQFP (fine pitch) (7 × 7)	128 KB
μPD70F3839GA-GAM-AX	48-pin plastic LQFP (fine pitch) (7 × 7)	256 KB
μPD70F3801K8-5B4-AX	48-pin plastic WQFN (7 × 7)	16 KB
μPD70F3802K8-5B4-AX	48-pin plastic WQFN (7 × 7)	32 KB
μPD70F3803K8-5B4-AX	48-pin plastic WQFN (7 × 7)	64 KB
μPD70F3804K8-5B4-AX	48-pin plastic WQFN (7 × 7)	128 KB
μPD70F3839K8-5B4-AX	48-pin plastic WQFN (7 × 7)	256 KB

Remark The V850ES/JC3-L is a lead-free product.

1.4.2 V850ES/JE3-L

Part Number	Package	Internal Flash Memory
μPD70F3805GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	16 KB
μPD70F3806GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	32 KB
μPD70F3807GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	64 KB
μPD70F3808GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	128 KB
μPD70F3840GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	256 KB

Remark The V850ES/JE3-L is a lead-free product.

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Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
FFFFF152H	Interrupt control register (INTCB0R/INTIIC1)	CB0RIC/IICIC1	R/W	√	√		47H
FFFFF154H	Interrupt control register (INTCB0T)	CB0TIC		√	√		47H
FFFFF156H	Interrupt control register (INTCB1R)	CB1RIC		√	√		47H
FFFFF158H	Interrupt control register (INTCB1T)	CB1TIC		√	√		47H
FFFFF15AH	Interrupt control register (INTCB2R)	CB2RIC		√	√		47H
FFFFF15CH	Interrupt control register (INTCB2T)	CB2TIC		√	√		47H
FFFFF15EH	Interrupt control register (INTCB3R)	CB3RIC		√	√		47H
FFFFF160H	Interrupt control register (INTCB3T)	CB3TIC		√	√		47H
FFFFF162H	Interrupt control register (INTUA0R/INTCB4R)	UA0RIC/CB4RIC		√	√		47H
FFFFF164H	Interrupt control register (INTUA0T/INTCB4T)	UA0TIC/CB4TIC		√	√		47H
FFFFF166H	Interrupt control register (INTUA1R/INTIIC2)	UA1RIC/IICIC2		√	√		47H
FFFFF168H	Interrupt control register (INTUA1T)	UA1TIC		√	√		47H
FFFFF16AH	Interrupt control register (INTUA2R/INTIIC0)	UA2RIC/IICIC0		√	√		47H
FFFFF16CH	Interrupt control register (INTUA2T)	UA2TIC		√	√		47H
FFFFF16EH	Interrupt control register (INTAD)	ADIC		√	√		47H
FFFFF170H	Interrupt control register (INTDMA0)	DMAIC0		√	√		47H
FFFFF172H	Interrupt control register (INTDMA1)	DMAIC1		√	√		47H
FFFFF174H	Interrupt control register (INTDMA2)	DMAIC2		√	√		47H
FFFFF176H	Interrupt control register (INTDMA3)	DMAIC3		√	√		47H
FFFFF178H	Interrupt control register (INTKR)	KRIC		√	√		47H
FFFFF17AH	Interrupt control register (INTWTI/INTRTC2)	WTIIC/RTC2IC		√	√		47H
FFFFF17CH	Interrupt control register (INTWT/INTRTC0)	WTIC/RTC0IC		√	√		47H
FFFFF17EH	Interrupt control register (INTRTC1)	RTC1C		√	√		47H
FFFFF1FAH	In-service priority register	ISPR	R	√	√		00H
FFFFF1FCH	Command register	PRCMD	W		√		Undefined
FFFFF1FEH	Power save control register	PSC[Note]	R/W	√	√		00H
FFFFF200H	A/D converter mode register 0	ADA0M0		√	√		00H
FFFFF201H	A/D converter mode register 1	ADA0M1		√	√		00H
FFFFF202H	A/D converter channel specification register	ADA0S		√	√		00H
FFFFF203H	A/D converter mode register 2	ADA0M2		√	√		00H
FFFFF204H	Power-fail compare mode register	ADA0PFM		√	√		00H
FFFFF205H	Power-fail compare threshold value register	ADA0PFT		√	√		00H
FFFFF210H	A/D conversion result register 0	ADA0CR0	R			√	Undefined
FFFFF211H	A/D conversion result register 0H	ADA0CR0H			√		Undefined
FFFFF212H	A/D conversion result register 1	ADA0CR1				√	Undefined
FFFFF213H	A/D conversion result register 1H	ADA0CR1H			√		Undefined
FFFFF214H	A/D conversion result register 2	ADA0CR2				√	Undefined
FFFFF215H	A/D conversion result register 2H	ADA0CR2H			√		Undefined
FFFFF216H	A/D conversion result register 3	ADA0CR3				√	Undefined
FFFFF217H	A/D conversion result register 3H	ADA0CR3H			√		Undefined

Note This is a special register.

(2) Port 0 mode register (PM0)

(a) V850ES/JC3-L (40-pin), V850ES/JC3-L (48-pin)

After reset: FFH R/W Address: FFFFF420H

	7	6	5	4	3	2	1	0
PM0	1	1	PM05	1	PM03	PM02	1	1

PM0n	I/O mode control (n = 2, 3, 5)
0	Output mode
1	Input mode

(b) V850ES/JE3-L

After reset: FFH R/W Address: FFFFF420H

	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	1	1

PM0n	I/O mode control (n = 2 to 6)
0	Output mode
1	Input mode

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(c) V850ES/JE3-L (2/2)

PMC97	Specification of pin operation
0	I/O port (P97)
1	SIB1 input/TIP20 input/TOP20 output

PMC96	Specification of pin operation
0	I/O port (P96)
1	TIP21 input/TOP21 output

PMC94	Specification of pin operation
0	I/O port (P94)
1	TIP31 input/TOP31 output

PMC93	Specification of pin operation
0	I/O port (P93)
1	TIP40 input/TOP40 output

PMC92	Specification of pin operation
0	I/O port (P92)
1	TIP41 input/TOP41 output

PMC91	Specification of pin operation
0	I/O port (P91)
1	KR7 input/RXDA1 input/SCL02 I/O

PMC90	Specification of pin operation
0	I/O port (P90)
1	KR6 input/TXDA1 output/SDA02 I/O

Remarks 1. The PMC9 register can be read or written in 16-bit units.
However, when using the higher 8 bits of the PMC9 register as the PMC9H register and the lower 8 bits as the PMC9L register, PMC9 can be read or written in 8-bit or 1-bit units.

2. To read/write bits 8 to 15 of the PMC9 register in 8-bit or 1-bit units, specify them as bits 0 to 7 of the PMC9H register.

(6) Port 9 alternate function specifications

PFCE915	PFC915	Specification of P915 pin alternate function
0	0	Setting prohibited
0	1	INTP6 input
1	0	TIP50 input
1	1	TOP50 output

PFCE914	PFC914	Specification of P914 pin alternate function
0	0	Setting prohibited
0	1	INTP5 input
1	0	TIP51 input
1	1	TOP51 output

PFC913 Note1	Specification of P913 pin alternate function
0	Setting prohibited
1	INTP4 input

PFC912 Note1	Specification of P912 pin alternate function
0	Setting prohibited
1	$\overline{\text{SCKB3}}$ I/O

PFC911 Note1	Specification of P911 pin alternate function
0	Setting prohibited
1	SOB3 output

PFC910 Note1	Specification of P910 pin alternate function
0	Setting prohibited
1	SIB3 input

PFC99 Note2	Specification of P99 pin alternate function
0	Setting prohibited
1	$\overline{\text{SCKB1}}$ I/O

PFC98 Note2	Specification of P98 pin alternate function
0	Setting prohibited
1	SOB1 output

PFCE97	PFC97	Specification of P97 pin alternate function
0	0	Setting prohibited
0	1	SIB1 input Note2
1	0	TIP20 input
1	1	TOP20 output

Notes 1. V850ES/JE3-L only
2. V850ES/JC3-L (48-pin), V850ES/JE3-L only

4.4 Block Diagrams

Figure 4-5. Block Diagram of Type A-1

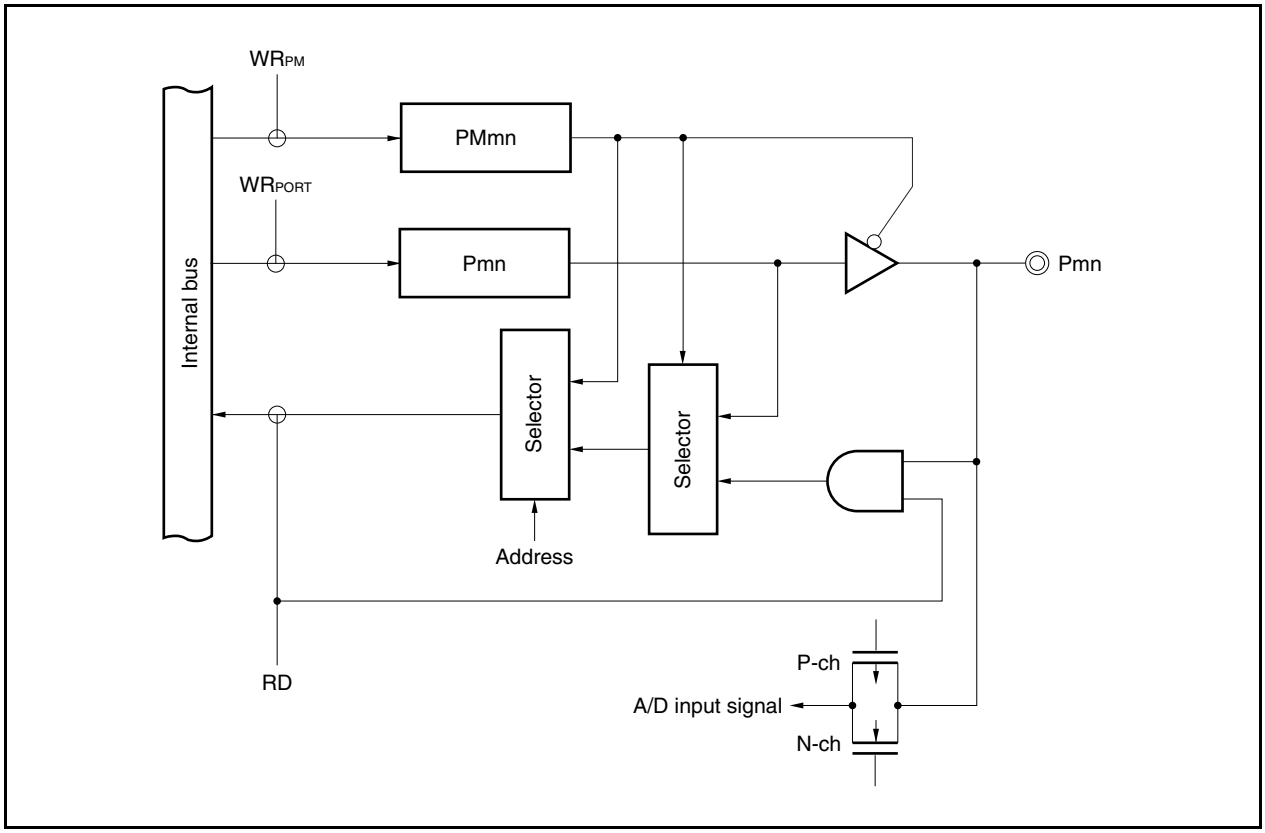
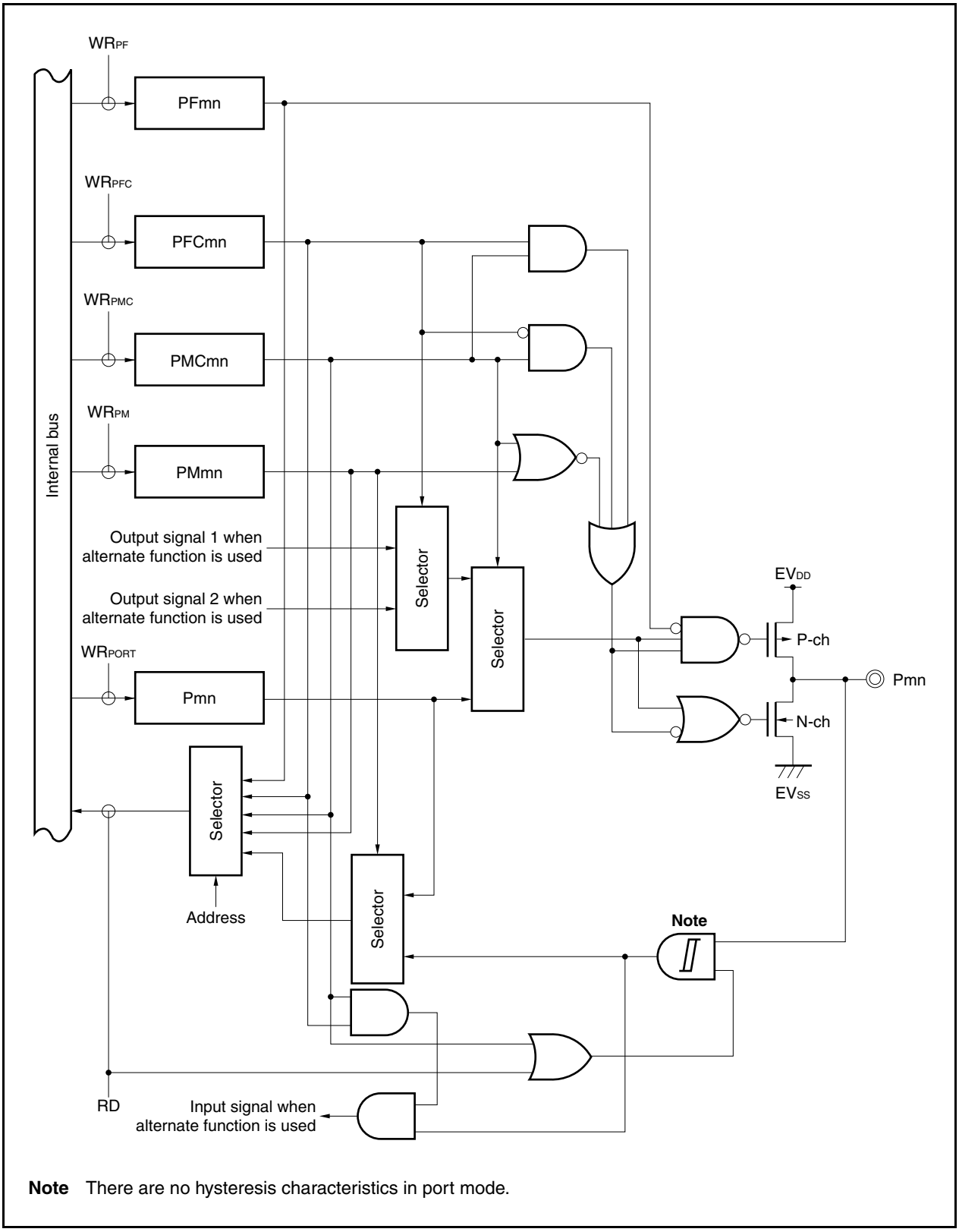


Figure 4-12. Block Diagram of Type G-12

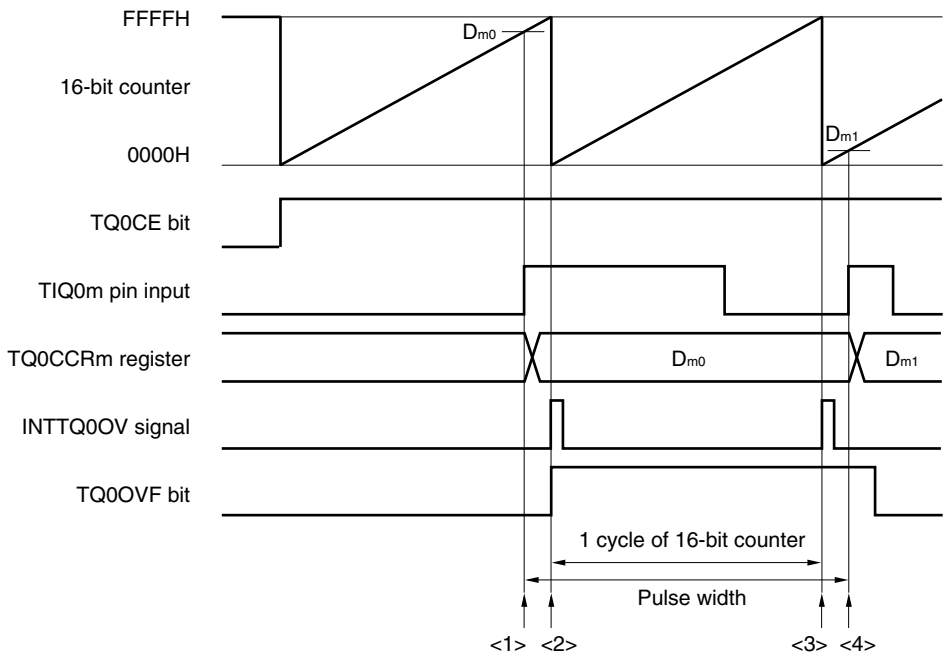


Note There are no hysteresis characteristics in port mode.

(d) Processing of overflow if capture trigger interval is long

If the pulse width is greater than one cycle of the 16-bit counter, care must be exercised because an overflow may occur more than once between the first capture trigger and the next. First, an example of incorrect processing is shown below.

Figure 7-63. Example of Incorrect Processing When Capture Trigger Interval Is Long (When Using TIQ0m)



The following problem may occur when a long pulse width is measured in the free-running timer mode.

<1> The TQ0CCRm register is read (the default value of the TIQ0m pin input is set).
<2> An overflow occurs. There is no software processing.
<3> An overflow occurs a second time. There is no software processing.
<4> The TQ0CCRm register is read.
The TQ0OVF bit is read. The TQ0OVF bit is 1, so it is cleared to 0.
Because the TQ0OVF bit was 1, the pulse width can be calculated by (10000H + D_{m1} − D_{m0}) (incorrect).
Actually, the pulse width should be (20000H + D_{m1} − D_{m0}) because an overflow occurred twice.

Remark m = 0 to 3

If an overflow occurs twice or more when the capture trigger interval is long, the correct pulse width may not be obtained.
If the capture trigger interval is long, slow the count clock to lengthen one cycle of the 16-bit counter, or use software to resolve the problem. An example of how to use software to resolve the problem is shown below.

(2) Using pulse width measurement mode

(a) Clearing the overflow flag (TQ0OVF)

The overflow flag (TQ0OVF) can be cleared to 0 by reading the TQ0OVF bit and, if its value is 1, either clearing the bit to 0 by using the CLR1 instruction or by writing 8-bit data (with bit 0 as “0”) to the TQ0OPT0 register.

7.4.8 Timer output operations

The following table shows the operations and output levels of the TOQ00 to TOQ03 pins.

Table 7-8. Timer Output Control in Each Mode

Operation Mode	TOQ00 Pin	TOQ01 Pin	TOQ02 Pin	TOQ03 Pin
Interval timer mode	Square wave output			
External event count mode	–			
External trigger pulse output mode	Square wave output	External trigger pulse output	External trigger pulse output	External trigger pulse output
One-shot pulse output mode		One-shot pulse output	One-shot pulse output	One-shot pulse output
PWM output mode		PWM output	PWM output	PWM output
Free-running timer mode	Square wave output (only when compare function is used)			
Pulse width measurement mode	–			

Table 7-9. Truth Table of TOQ00 to TOQ03 Pins Under Control of Timer Output Control Bits

TQ0IOC0.TQ0OLm Bit	TQ0IOC0.TQ0OEm Bit	TQ0CTL0.TQ0CE Bit	Level of TOQ0m Pin
0	0	×	Low-level output
	1	0	Low-level output
		1	Low level immediately before counting, high level after counting is started
1	0	×	High-level output
	1	0	High-level output
		1	High level immediately before counting, low level after counting is started

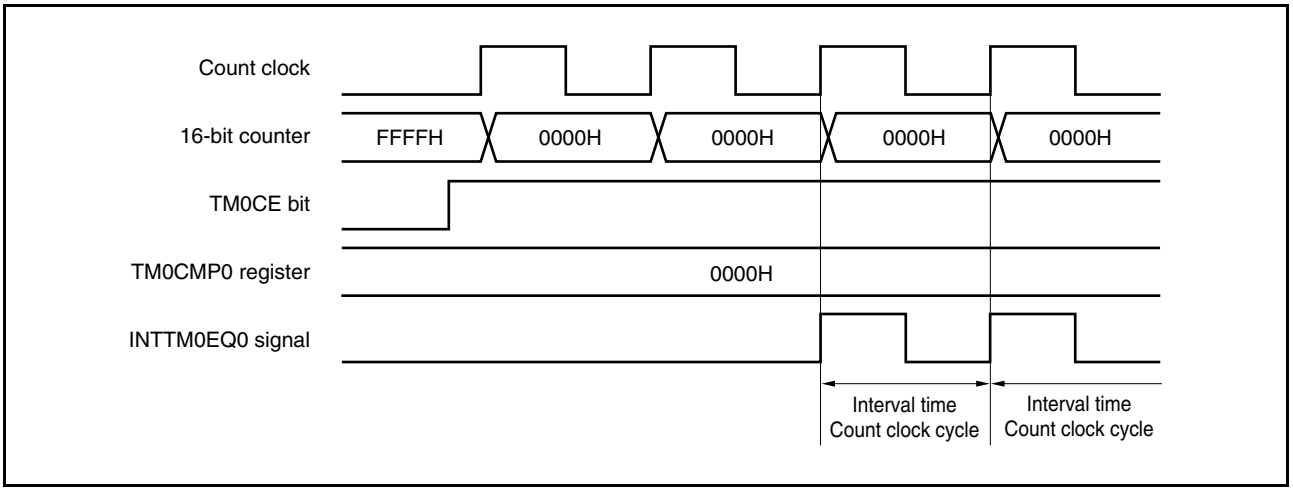
Remark m = 0 to 3

(2) Using interval timer mode

(a) Operation when TM0CMP0 register is set to 0000H

When the TM0CMP0 register is set to 0000H, the INTTM0EQ0 signal is generated for each count clock cycle. The value of the 16-bit counter is always 0000H.

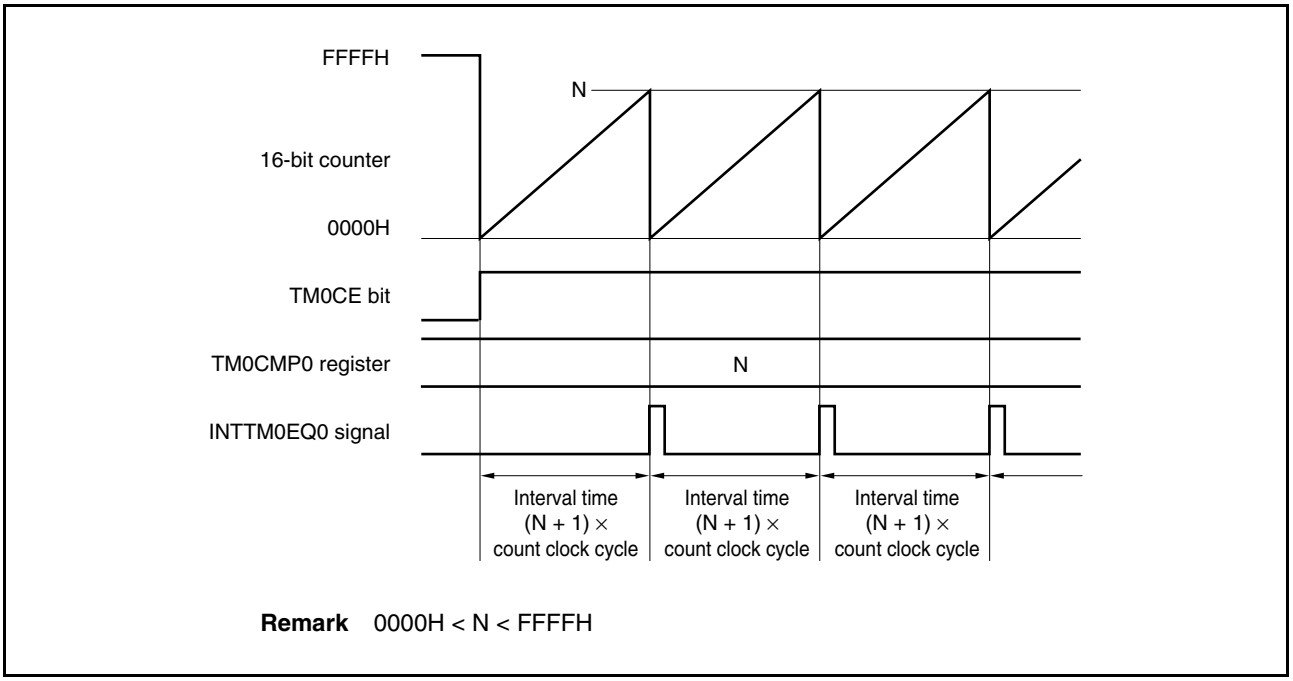
Figure 8-6. Operation of Interval Timer When TM0CMP0 Register Is Set to 0000H



(b) Operation when TM0CMP0 register is set to *N*

When the TM0CMP0 register is set to *N*, the 16-bit counter increments up to *N* and is reset to 0000H in synchronization with the next increment timing. The INTTM0EQ0 signal is then generated.

Figure 8-7. Operation of Interval Timer When TM0CMP0 Register is Set to Other Than 0000H, FFFFH



Remark 0000H < N < FFFFH

(4) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

<1> When WTIMn bit = 0 (after restart, address mismatch (= not extension code))

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1		▲2					▲3		Δ4

▲1: IICSn register = 0010X010B

▲2: IICSn register = 0010X000B

▲3: IICSn register = 00000X10B

Δ 4: IICSn register = 00000001B

Remark ▲:Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

<2> When WTIMn bit = 1 (after restart, address mismatch (= not extension code))

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1	▲2		▲3				▲4		Δ5

▲1: IICSn register = 0010X010B

▲2: IICSn register = 0010X110B

▲3: IICSn register = 0010XX00B

▲4: IICSn register = 00000X10B

Δ 5: IICSn register = 00000001B

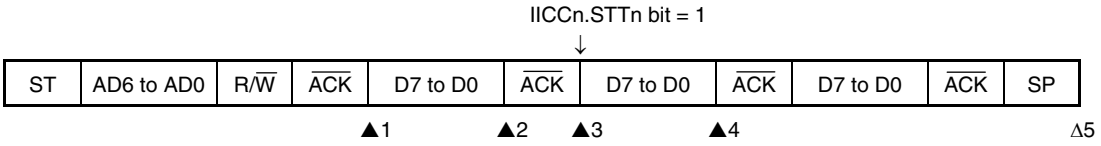
Remark ▲:Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

(6) When arbitration loss occurs due to low level of SDA0n pin when attempting to generate a restart condition

<1> When WTIMn bit = 0



▲1: IICSn register = 1000X110B

▲2: IICSn register = 1000X000B (WTIMn bit = 1)

▲3: IICSn register = 1000XX00B (WTIMn bit = 0)

▲4: IICSn register = 01000000B (Example: When ALDn bit is read during interrupt servicing)

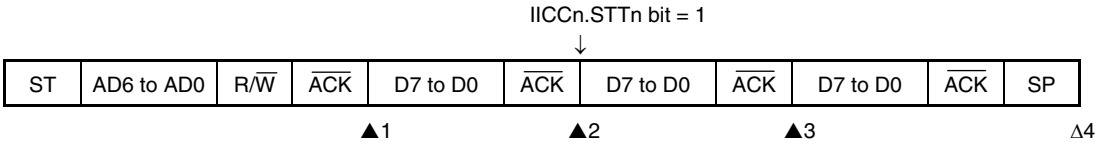
Δ 5: IICSn register = 00000001B

Remark ▲:Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

<2> When WTIMn bit = 1



▲1: IICSn register = 1000X110B

▲2: IICSn register = 1000XX00B

▲3: IICSn register = 01000100B (Example: When ALDn bit is read during interrupt servicing)

Δ 4: IICSn register = 00000001B

Remark ▲:Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

19.3.3 Priorities of maskable interrupts

The INTC can acknowledge an interrupt while servicing another. Interrupts that occur at the same time are serviced according to their priority order.

There are two types of priority level control: control based on the programmable priority levels that are specified by the interrupt priority level specification bit (xxPRn) of the interrupt control register (xxICn), and control based on the default priority levels. Programmable priority control classifies interrupt request signals into eight levels according to the setting of the xxPRn flag. When multiple interrupts having the same priority level specified by the xxPRn bit occur at the same time, the interrupts are serviced according to the priority levels assigned to the corresponding interrupt requests (default priority level) beforehand. For details, see **Table 19-1 Interrupt Source List**.

For details about multiple interrupts, see **19.7 Multiple Interrupt Servicing Control**.

Remark xx: Identification name of each peripheral unit (see **Table 19-3 Interrupt Control Registers (xxICn)**)
n: Peripheral unit number (see **Table 19-3 Interrupt Control Registers (xxICn)**).

CHAPTER 24 LOW-VOLTAGE DETECTOR (LVI)

24.1 Functions

The low-voltage detector (LVI) has the following functions.

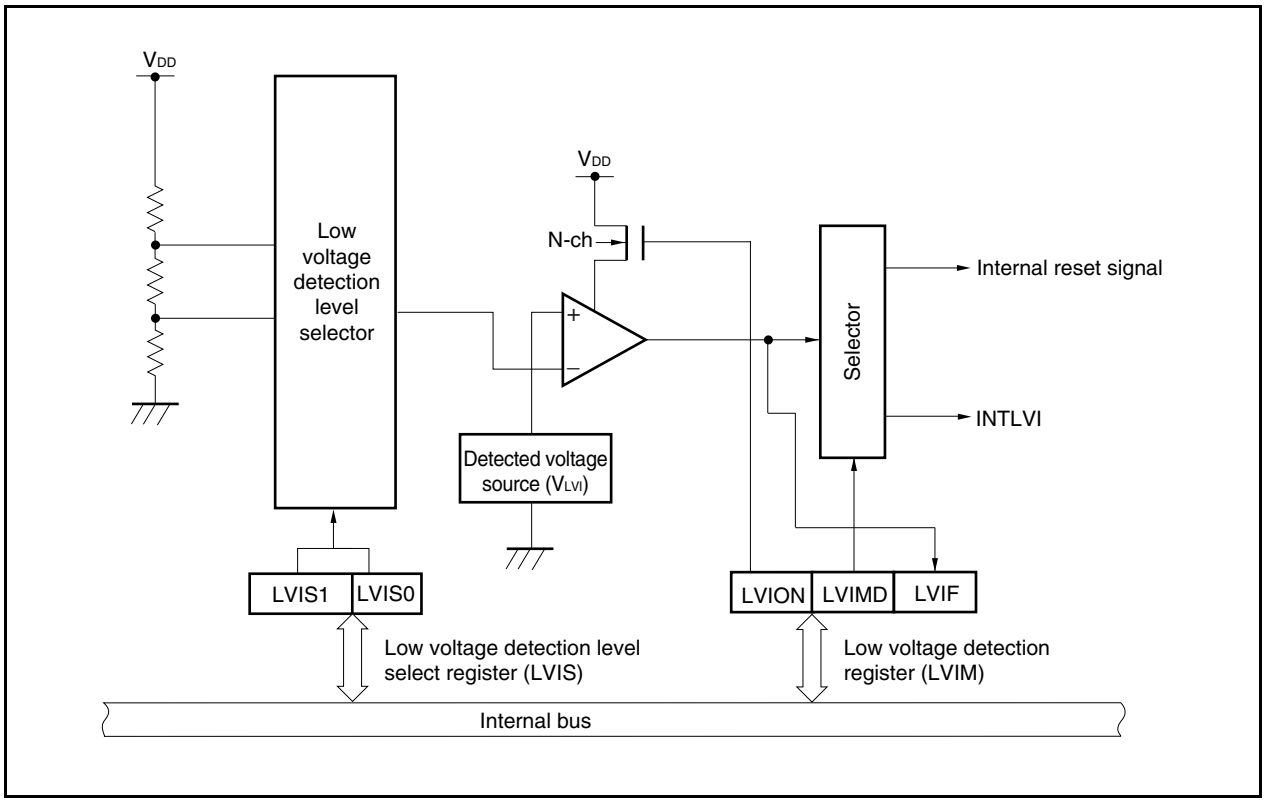
- If interrupt occurrence at low-voltage detection is selected as the operation mode, the low-voltage detector compares the supply voltage (V_{DD}) and the detection voltage (V_{LVI}), and generates an internal interrupt signal when the supply voltage drops below or rises above the detection voltage.
- If reset occurrence at low-voltage detection is selected as the operation mode, the low-voltage detector generates an internal reset signal when the supply voltage (V_{DD}) drops below the detection voltage (V_{LVI}).
- The level of the supply voltage to be detected can be changed by software.
- Interrupt or reset signal can be selected by software.
- The low-voltage detector is operable in the standby mode.

If a reset occurs when the low-voltage detector is selected to generate a reset signal, the RESF.LVIRF bit is set to 1. For details about the RESF register, see **22.3 Register to Check Reset Source**.

24.2 Configuration

The block diagram of the low-voltage detector is shown below.

Figure 24-1. Block Diagram of Low-Voltage Detector

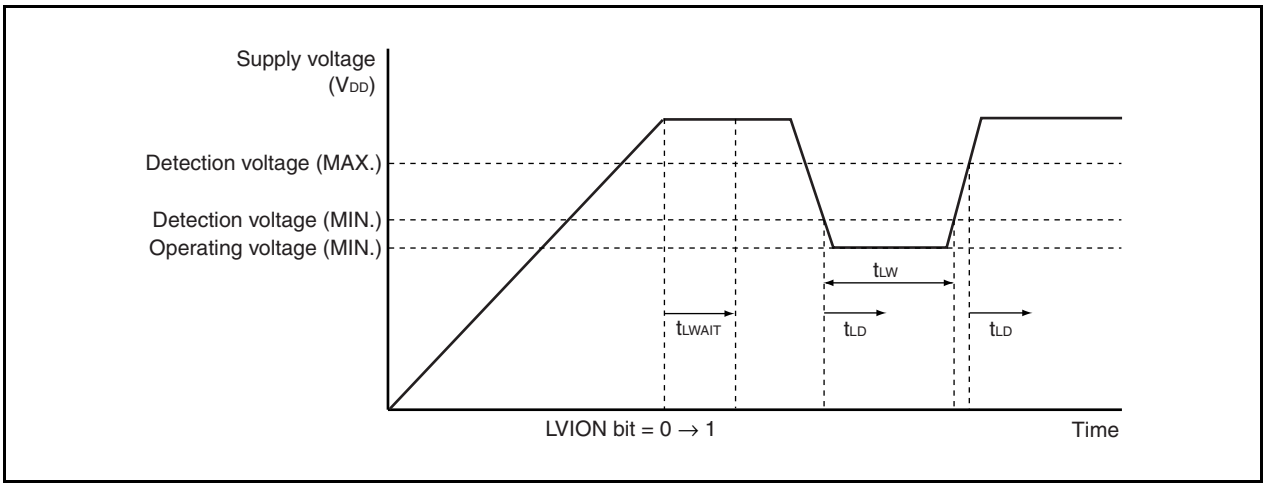


30.8.8 LVI circuit characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.2 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVI0}		2.7	2.8	2.9	V
	V_{LVI1}		2.2	2.3	2.4	V
Response time[Note]	t_{LD}	At rising edge: After V_{DD} reaches V_{LVI0}/V_{LVI1} (MAX.) At falling edge: After V_{DD} has dropped to V_{LVI0}/V_{LVI1}(MIN.)		0.2	2.0	ms
Minimum pulse width	t_{LW}	V_{DD} = V_{LVI0}/V_{LVI1} (MIN.)	0.2			ms
Reference voltage stabilization wait time	t_{LWAIT}	After V_{DD} reaches V_{LVI0}/V_{LVI1} (MAX.)		0.1	0.2	ms

Note Time required to detect the detection voltage and output an interrupt or reset signal.



31.6.2 Supply current characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.[Note 1]	MAX.[Note 2]	Unit
Supply current[Note 3]	I_{DD1}	Normal operation	f_{XX} = 20 MHz (f_X = 5 MHz)[Note 4]		8.2[Note 5]	20	mA
			f_{XX} = 10 MHz (f_X = 10 MHz), PLL off[Note 4]		4.1[Note 5]	10	mA
	I_{DD2}	HALT mode	f_{XX} = 20 MHz (f_X = 5 MHz)[Note 4]		5.3	14	mA
	I_{DD3}	IDLE1 mode	f_{XX} = 5 MHz (f_X = 5 MHz), PLL off[Note 4]		0.5	1	mA
	I_{DD4}	IDLE2 mode	f_{XX} = 5 MHz (f_X = 5 MHz), PLL off[Note 4]		0.21	0.5	mA
	I_{DD5}	Subclock operation mode	f_{XT} = 32.768 kHz, main clock stopped, internal oscillator stopped, PLL off REGOVL0 = 02H (low-voltage subclock operation mode)		9.6		μA
	I_{DD6}	Sub-IDLE mode	f_{XT} = 32.768 kHz, main clock stopped, internal oscillator stopped, PLL off REGOVL0 = 02H (low-voltage sub-IDLE mode)		1.9	30	μA
	I_{DD7}	STOP mode	Subclock stopped, internal oscillator stopped REGOVL0 = 01H (low-voltage STOP mode) T_A = 25°C		1.1	3.0	μA
			Subclock stopped, internal oscillator stopped REGOVL0 = 01H (low-voltage STOP mode) T_A = 85°C			25	μA
			Subclock operating, internal oscillator stopped REGOVL0 = 01H (low-voltage STOP mode)		1.9	30	μA
	I_{DD8}	Self programming mode	f_{XX} = 20 MHz (f_X = 5 MHz)		14	24	mA
LVI current	I_{LVI}				1.2	3	μA
WDT, internal oscillation current	I_{WDT}				5		μA

Notes 1. TYP. current is a value at V_{DD} = EV_{DD} = 3.3 V, T_A = 25°C.
The TYP. value is not a value guaranteed for each device.

2. MAX. current is a value at which the characteristic in question is at the worst-case value at V_{DD} = EV_{DD} = 3.6 V, T_A = –40 to +85°C.

3. Total of V_{DD} and EV_{DD} currents. Currents I_{LVI} and I_{WDT} flowing through the output buffers, A/D converter, D/A converter, and on-chip pull-down resistor are not included.

4. TYP. value indicates the current value when "RTC" or "watch timer + TMM (count by watch timer interrupt)" operate as peripheral functions.
MAX. value indicates the current value when all the functions operable in a range in which the pin status is not changed operate as peripheral functions.
However, I_{LVI} and I_{WDT} are excluded.

5. TYP. value of I_{DD1} is a value when all instructions are executed.

Remark For details about the operating voltage, see **31.3 Operating Conditions**.

31.8.6 I²C bus mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = 2.2 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter		Symbol		Normal Mode		High-Speed Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCL0n clock frequency		f_{CLK}		0	100	0	400	kHz
Bus free time (Between start and stop conditions)		t_{BUF}	<66>	4.7	–	1.3	–	μs
Hold time[Note 1]		$t_{HD:STA}$	<67>	4.0	–	0.6	–	μs
SCL0n clock low-level width		t_{LOW}	<68>	4.7	–	1.3	–	μs
SCL0n clock high-level width		t_{HIGH}	<69>	4.0	–	0.6	–	μs
Setup time for start/restart conditions		$t_{SU:STA}$	<70>	4.7	–	0.6	–	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	<71>	5.0	–	–	–	μs
	I²C mode			0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	<72>	250	–	100[Note 4]	–	ns
SDA0n and SCL0n signal rise time		t_R	<73>	–	1000	20 + 0.1Cb[Note 5]	300	ns
SDA0n and SCL0n signal fall time		t_F	<74>	–	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	<75>	4.0	–	0.6	–	μs
Pulse width of spike suppressed by input filter		t_{SP}	<76>	–	–	0	50	ns
Capacitance load of each bus line		Cb		–	400	–	400	pF

Notes 1. At the start condition, the first clock pulse is generated after the hold time.

2. The system requires a minimum of 300 ns hold time internally for the SDA0n signal (at $V_{IHmin.}$ of SCL0n signal) in order to occupy the undefined area at the falling edge of SCL0n.

3. If the system does not extend the SCL0n signal low hold time (t_{LOW}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.

4. The high-speed mode I²C bus can be used in the normal-mode I²C bus system. In this case, set the high-speed mode I²C bus so that it meets the following conditions.

- If the system does not extend the SCL0n signal's low state hold time:
  $t_{SU:DAT} \geq 250$ ns
- If the system extends the SCL0n signal's low state hold time:
  Transmit the following data bit to the SDA0n line prior to the SCL0n line release ($t_{Rmax.} + t_{SU:DAT}$ = 1,000 + 250 = 1,250 ns: Normal mode I²C bus specification).

5. Cb: Total capacitance of one bus line (unit: pF)

Remark n = 0 to 2

CHAPTER 32 ELECTRICAL SPECIFICATIONS (V850ES/JE3-L) (Target)

32.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	$V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	EV_{DD}	$V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	AV_{REF0}	$V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	AV_{REF1}	$V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	V_{SS}	$V_{SS} = EV_{SS} = AV_{SS}$	−0.5 to +0.5	V
	AV_{SS}	$V_{SS} = EV_{SS} = AV_{SS}$	−0.5 to +0.5	V
	EV_{SS}	$V_{SS} = EV_{SS} = AV_{SS}$	−0.5 to +0.5	V
Input voltage	V_{I1}	P97 to P915, PCM0, PDL5, $\overline{\text{RESET}}$, FLMD0	−0.5 to EV_{DD} + 0.5 Note 1	V
	V_{I2}	P10	−0.5 to AV_{REF1} + 0.5 Note 1	V
	V_{I3}	X1	−0.5 to V_{DD} + 0.5 Note 1	V
		X2	−0.5 to V_{RO} Note 2 + 0.5 Note 1	
	V_{I4}	P02 to P06, P30 to P35, P38, P39, P40 to P42, P50 to P55, P90 to P94, P96	−0.5 to +6.0	V
	V_{I5}	XT1, XT2	−0.5 to V_{RO} Note 2 + 0.5	V
Analog input voltage	V_{IAN}	P70 to P79	−0.5 to AV_{REF0} + 0.5 Note 1	V

Notes 1. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

2. On-chip regulator output voltage

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

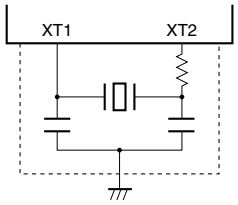
2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics, AC characteristics, and operating conditions represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the ratings of alternate-function pins are the same as those of port pins.

32.4.2 Subclock oscillator characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = 2.2 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Resonator	Circuit Example	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2				10	s

Notes 1. The oscillation frequency shown above indicates only oscillator characteristics. Use the V850ES/JE3-L so that the internal operation conditions do not exceed the ratings shown in **AC Characteristics**, **DC Characteristics**, and operating conditions.

2. Time required from when V_{DD} reaches the oscillation voltage range (2.2 V (MIN.)) to when the crystal resonator stabilizes.

Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subclock oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the main clock oscillator.
Particular care is therefore required with the wiring method when the subclock is used.

3. For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.