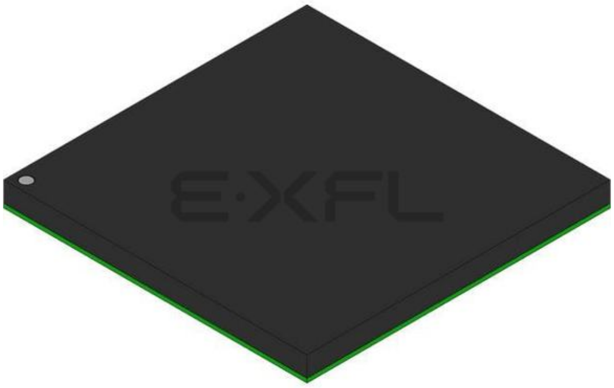

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=kmpc8313cvragdb

1.10 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the MPC8313E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

1.11 DMA Controller, Dual I^{2}C, DUART, Local Bus Controller, and Timers

The MPC8313E provides an integrated four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Supports misaligned transfers

There are two I^{2}C controllers. These synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. The 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8313E local bus controller (LBC) port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The three user programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM or UPM controller. The FCM provides a glueless interface to parallel-bus NAND Flash E2PROM devices. The FCM contains three basic configuration register groups—BR*n*, OR*n*, and FMR. Both may exist in the same system. The local bus can operate at up to 66 MHz.

The MPC8313E system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8313E. The MPC8313E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value[1]	Unit	Current Requirement
Core supply voltage	V_{DD}	1.0 V ± 50 mV	V	469 mA
Internal core logic constant power	V_{DDC}	1.0 V ± 50 mV	V	377 mA
SerDes internal digital power	$XCOREV_{DD}$	1.0	V	170 mA
SerDes internal digital ground	$XCOREV_{SS}$	0.0	V	—
SerDes I/O digital power	$XPADV_{DD}$	1.0	V	10 mA
SerDes I/O digital ground	$XPADV_{SS}$	0.0	V	—
SerDes analog power for PLL	$SDAV_{DD}$	1.0 V ± 50 mV	V	10 mA
SerDes analog ground for PLL	$SDAV_{SS}$	0.0	V	—
Dedicated 3.3 V analog power for USB PLL	USB_PLL_PWR3	3.3 V ± 300 mV	V	2–3 mA
Dedicated 1.0 V analog power for USB PLL	USB_PLL_PWR1	1.0 V ± 50 mV	V	2–3 mA
Dedicated analog ground for USB PLL	USB_PLL_GND	0.0	V	—
Dedicated USB power for USB bias circuit	USB_VDDA_BIAS	3.3 V ± 300 mV	V	4–5 mA
Dedicated USB ground for USB bias circuit	USB_VSSA_BIAS	0.0	V	—
Dedicated power for USB transceiver	USB_VDDA	3.3 V ± 300 mV	V	75 mA
Dedicated ground for USB transceiver	USB_VSSA	0.0	V	—
Analog power for e300 core APLL	AV_{DD1} [6]	1.0 V ± 50 mV	V	2–3 mA
Analog power for system APLL	AV_{DD2} [6]	1.0 V ± 50 mV	V	2–3 mA
DDR1 DRAM I/O voltage (333 MHz, 32-bit operation)	GV_{DD}	2.5 V ± 125 mV	V	131 mA
DDR2 DRAM I/O voltage (333 MHz, 32-bit operation)	GV_{DD}	1.8 V ± 80 mV	V	140 mA
Differential reference voltage for DDR controller	MV_{REF}	1/2 DDR supply ($0.49 \times GV_{DD}$ to $0.51 \times GV_{DD}$)	V	—
Standard I/O voltage	NV_{DD}	3.3 V ± 300 mV[2]	V	74 mA
eTSEC2 I/O supply	LV_{DDA}	2.5 V ± 125 mV/ 3.3 V ± 300 mV	V	22 mA
eTSEC1/USB DR I/O supply	LV_{DDB}	2.5 V ± 125 mV/ 3.3 V ± 300 mV	V	44 mA
Supply for eLBC IOs	LV_{DD}	3.3 V ± 300 mV	V	16 mA
Analog and digital ground	V_{SS}	0.0	V	—
Junction temperature range	T_A/T_J [3]	0 to 105	°C	

3 Power Characteristics

The estimated typical power dissipation, not including I/O supply power, for this family of MPC8313E devices is shown in this table. Table 5 shows the estimated typical I/O power dissipation.

Table 4. MPC8313E Power Dissipation[1]

Core Frequency (MHz)	CSB Frequency (MHz)	Typical[2]	Maximum for Rev. 1.0 Silicon[3]	Maximum for Rev. 2.x or Later Silicon[3]	Unit
333	167	820	1020	1200	mW
400	133	820	1020	1200	mW

Note:

1. The values do not include I/O supply power or AV_{DD}, but do include core, USB PLL, and a portion of SerDes digital power (not including $XCOREV_{DD}$, $XPADV_{DD}$, or $SDAV_{DD}$, which all have dedicated power supplies for the SerDes PHY).
2. Typical power is based on a voltage of V_{DD} = 1.05 V and an artificial smoker test running at room temperature.
3. Maximum power is based on a voltage of V_{DD} = 1.05 V, a junction temperature of T_J = 105°C, and an artificial smoker test.

This table describes a typical scenario where blocks with the stated percentage of utilization and impedances consume the amount of power described.

Table 5. MPC8313E Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	NV_{DD} (3.3 V)	LV_{DDA}/ LV_{DDB} (3.3 V)	LV_{DDA}/ LV_{DDB} (2.5 V)	LV_{DD} (3.3 V)	Unit	Comments
DDR 1, 60% utilization, 50% read/write R_s = 22 Ω R_t = 50 Ω single pair of clock capacitive load: data = 8 pF, control address = 8 pF, clock = 8 pF	333 MHz, 32 bits	—	0.355	—	—	—	—	W	—
	266 MHz, 32 bits	—	0.323	—	—	—	—	W	—
DDR 2, 60% utilization, 50% read/write R_s = 22 Ω R_t = 75 Ω single pair of clock capacitive load: data = 8 pF, control address = 8 pF, clock = 8 pF	333 MHz, 32 bits	0.266	—	—	—	—	—	W	—
	266 MHz, 32 bits	0.246	—	—	—	—	—	W	—
PCI I/O load = 50 pF	33 MHz	—	—	0.120	—	—	—	W	—
	66 MHz	—	—	0.249	—	—	—	W	—
Local bus I/O load = 20 pF	66 MHz	—	—	—	—	—	0.056	W	—
	50 MHz	—	—	—	—	—	0.040	W	—
TSEC I/O load = 20 pF	MII, 25 MHz	—	—	—	0.008	—	—	W	Multiple by number of interface used
	RGMII, 125 MHz	—	—	—	0.078	0.044	—	W	

5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications.

Table 10. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock and power applied to SYS_CLK_IN when the device is in PCI host mode	32	—	$t_{SYS\_CLK\_IN}$	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock and power applied to PCI_SYNC_IN when the device is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3] and $\overline{\text{CFG\_CLK\_IN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	$t_{SYS\_CLK\_IN}$	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR configuration signal drivers with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to turn on POR configuration signal drivers with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:
1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the SYS_CLK_IN input, and PCI_SYNC_IN period depends on the value of $\overline{\text{CFG\_CLKIN\_DIV}}$.
2. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. It is only valid when the device is in PCI host mode.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$.

This table provides the PLL lock times.

Table 11. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
PLL lock times	—	100	µs	—

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface. Note that DDR SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Note
Output leakage current	I_{OZ}	–9.9	–9.9	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Note:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 16. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM when GV_{DD}(typ) = 1.8 V.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	—

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Silicon Rev 2.x or Later

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK[*n*] cycle time, MCK[*n*]/$\overline{\text{MCK}}$[*n*] crossing	t_{MCK}	6	10	ns	2
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz	t_{DDKHAS}	 2.1 2.5	 — —	ns	3
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz	t_{DDKHAX}	 2.0 2.7	 — —	ns	3
$\overline{\text{MCS}}$[*n*] output setup with respect to MCK 333 MHz 266 MHz	t_{DDKHCS}	 2.1 3.15	 — —	ns	3
$\overline{\text{MCS}}$[*n*] output hold with respect to MCK 333 MHz 266 MHz	t_{DDKHCX}	 2.0 2.7	 — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS 333 MHz 266 MHz	t_{DDKHDS}, t_{DDKLDS}	 800 900	 — —	ps	5
MDQ//MDM output hold with respect to MDQS 333 MHz 266 MHz	t_{DDKHDX}, t_{DDKLDX}	 750 1000	 — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

This figure provides the AC test load for the DDR bus.

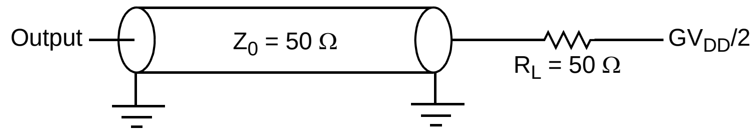

Figure 7. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 22. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.0	NV_{DD} + 0.3	V
Low-level input voltage NV_{DD}	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	NV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current (0 V ≤V_{IN} ≤ NV_{DD})	I_{IN}	—	±5	μA

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all the media independent interface (MII), reduced gigabit media independent interface (RGMII), serial gigabit media independent interface (SGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the MII interface can be operated at 3.3 V. The RMII and SGMII interfaces can be operated at either 3.3 or 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for *Gigabit Ethernet Physical Layer Device Specification Version 1.2*a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.5, "Ethernet Management Interface Electrical Characteristics."

8.1.1 TSEC DC Electrical Characteristics

All RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

NOTE

eTSEC should be interfaced with peripheral operating at same voltage level.

Table 24. MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DDA}/LV_{DDB}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LV_{DDA} or LV_{DDB} = Min	2.40	LV_{DDA} + 0.3 or LV_{DDB} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LV_{DDA} or LV_{DDB} = Min	V_{SS}	0.50	V
Input high voltage	V_{IH}	—	—	2.0	LV_{DDA} + 0.3 or LV_{DDB} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DDA} or LV_{DDB}		—	40	μA
Input low current	I_{IL}	V_{IN}[1] = VSS		–600	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 25. RGMII/RTBI DC Electrical Characteristics

Parameters	Symbol	Conditions	Min	Max	Unit
Supply voltage 2.5 V	LV_{DDA}/LV_{DDB}	—	2.37	2.63	V

Table 25. RGMII/RTBI DC Electrical Characteristics (continued)

Parameters	Symbol	Conditions		Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DDA} or LV_{DDB} = Min	2.00	LV_{DDA} + 0.3 or LV_{DDB} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DDA} or LV_{DDB} = Min	V_{SS} – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DDA} or LV_{DDB} = Min	1.7	LV_{DDA} + 0.3 or LV_{DDB} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DDA} or LV_{DDB} = Min	–0.3	0.70	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DDA} or LV_{DDB}		—	10	μA
Input low current	I_{IL}	V_{IN}[1] = V_{SS}		–15	—	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.2 MII, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for MII, RMII, RGMII, and RTBI are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 26. MII Transmit AC Timing Specifications

At recommended operating conditions with $LV_{DDA}/LV_{DDB}/NV_{DD}$ of 3.3 V ± 0.3 V.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

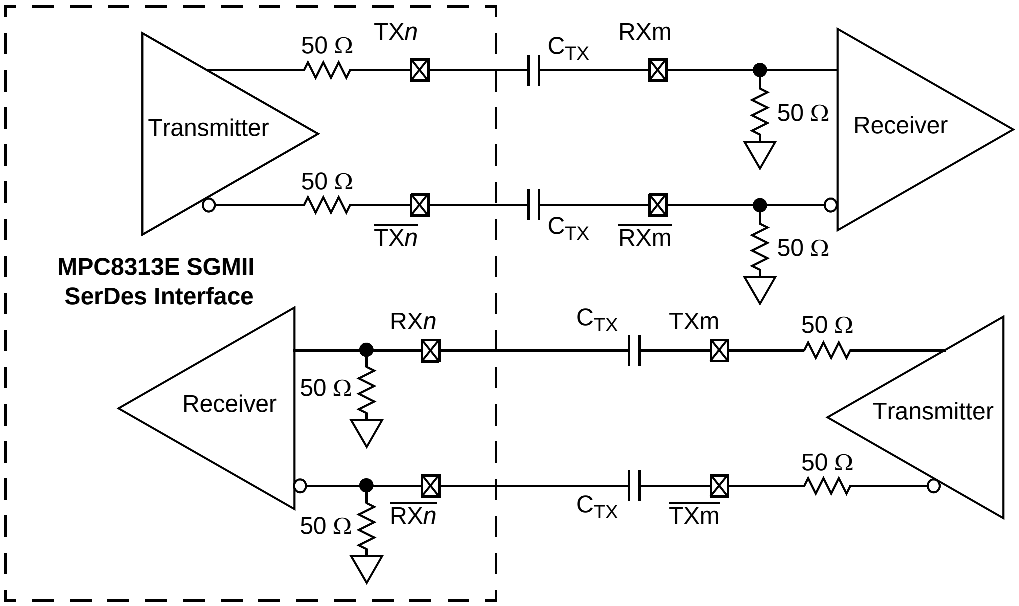

Figure 15. 4-Wire AC-Coupled SGMII Serial Link Connection Example

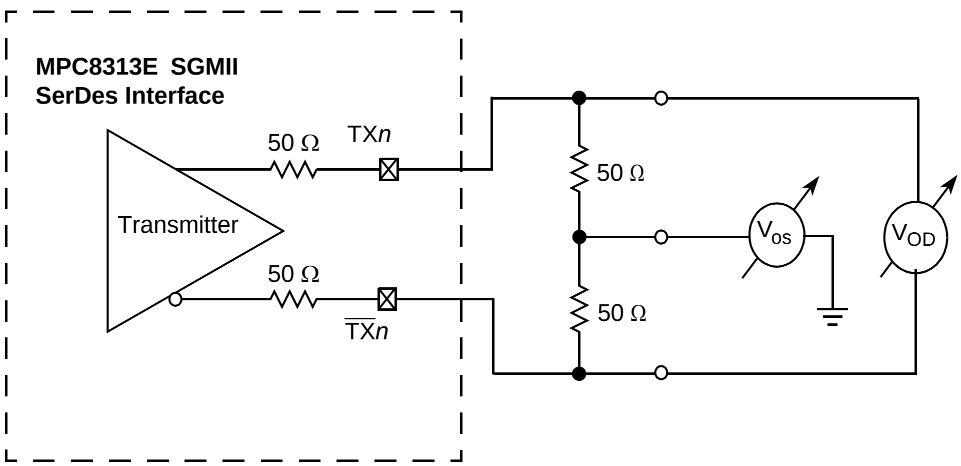

Figure 16. SGMII Transmitter DC Measurement Circuit

Table 33. SGMII DC Receiver Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$XCOREV_{DD}$	0.95	1.0	1.05	V	
DC Input voltage range			N/A			1
Input differential voltage	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2
Loss of signal threshold	VL_{OS}	30	—	100	mV	
Input AC common mode voltage	V_{CM_ACp-p}	—	—	100	mV	3
Receiver differential input impedance	Z_{RX_DIFF}	80	100	120	Ω	
Receiver common mode input impedance	Z_{RX_CM}	20	—	35	Ω	

Table 35. SGMII Receive AC Timing Specifications (continued)

At recommended operating conditions with $XCOREV_{DD}$ = 1.0 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Total jitter tolerance	JT	0.65	—	—	UI p-p	1
Bit error ratio	BER	—	—	10^{-12}		
Unit interval	UI	799.92	800	800.08	ps	2
AC coupling capacitor	C_{TX}	5	—	200	nF	3

Notes:

1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.

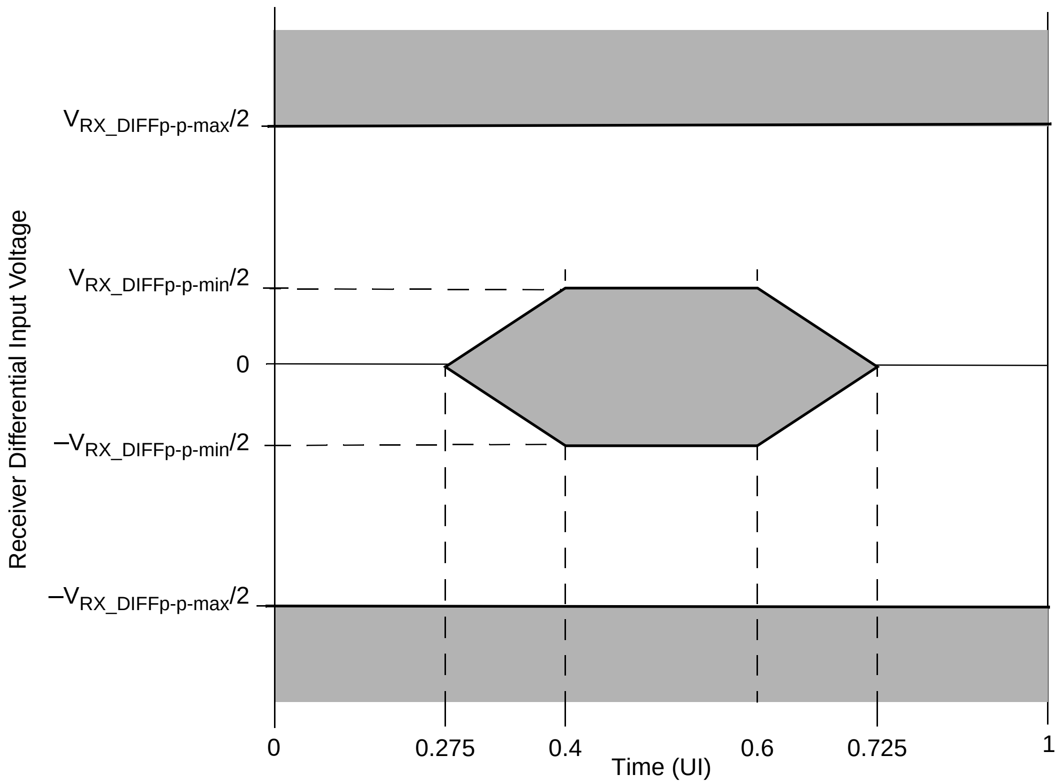

Figure 17. SGMII Receiver Input Compliance Mask

Table 36. eTSEC IEEE 1588 AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	—	—	ns	2

Notes:

1. T_{RX_CLK} is the max clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for a description of TMR_CTRL registers.
2. It need to be at least two times of clock period of clock selected by TMR_CTRL[CKSEL]. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 3600, 280, and 56 ns, respectively.

8.5 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, RMII, RGMII, SGMII, and RTBI are specified in Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics.”

8.5.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. Table 37 provide the DC electrical characteristics for MDIO and MDC.

Table 37. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	NV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	NV_{DD} = Min	2.10	NV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	NV_{DD} = Min	V_{SS}	0.50	V
Input high voltage	V_{IH}	—		2.0	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input high current	I_{IH}	NV_{DD} = Max	V_{IN}[1] = 2.1 V	—	40	μA
Input low current	I_{IL}	NV_{DD} = Max	V_{IN} = 0.5 V	–600	—	μA

9 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

9.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 22 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TX*n* and $\overline{\text{TX}n}$) or a receiver input (RX*n* and $\overline{\text{RX}n}$). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-ended swing

   The transmitter output signals and the receiver input signals TX*n*, $\overline{\text{TX}n}$, RX*n*, and $\overline{\text{RX}n}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

2. Differential output voltage, V_{OD} (or differential output swing):

   The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{TXn} - V_{\overline{TXn}}$. The V_{OD} value can be either positive or negative.

3. Differential input voltage, V_{ID} (or differential input swing):

   The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{RXn} - V_{\overline{RXn}}$. The V_{ID} value can be either positive or negative.

4. Differential peak voltage, V_{DIFFp}

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

5. Differential peak-to-peak, $V_{DIFFp\text{-}p}$

   Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp\text{-}p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{OD}|$.

6. Differential waveform

   The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{TX}n}$, for example) from the non-inverting signal (TX*n*, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 22 as an example for differential waveform.

7. Common mode voltage, V_{cm}

This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8313E SerDes reference clock input's DC requirement.

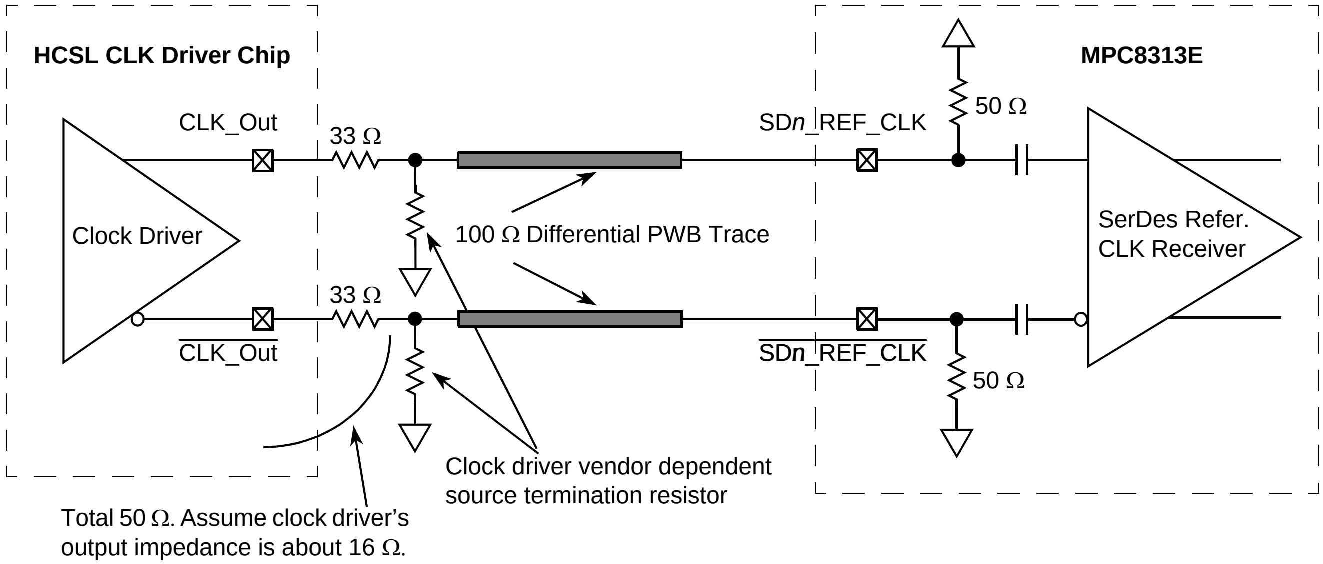

Figure 27. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8313E SerDes reference clock input's allowed range (100 to 400 mV), the AC-coupled connection scheme must be used. It assumes the LVDS output driver features a 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

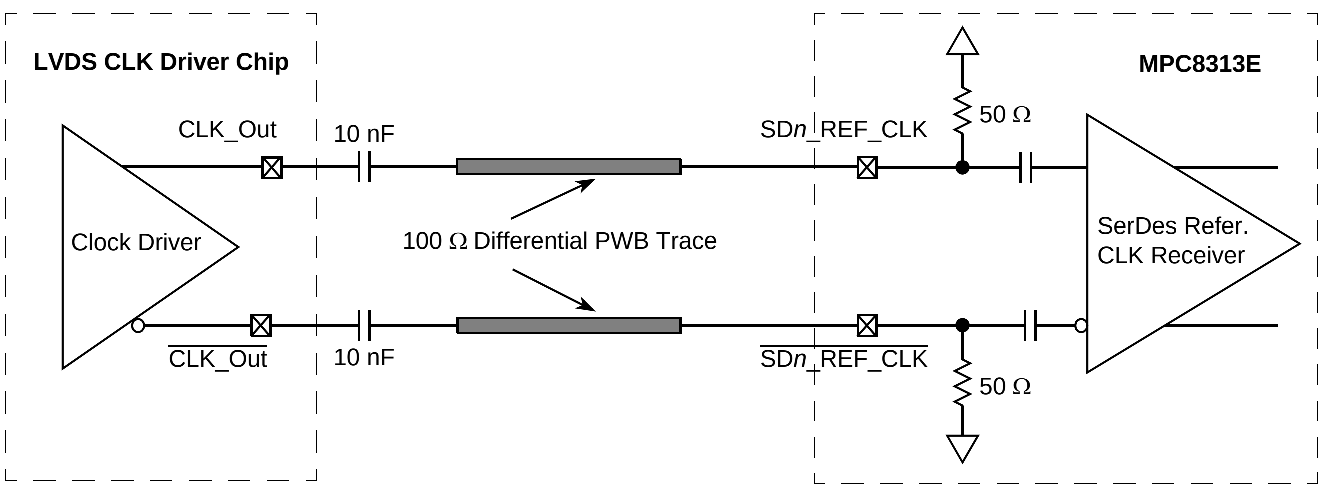

Figure 28. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the MPC8313E SerDes reference clock input's DC requirement, AC coupling has to be used. Figure 29

Table 47. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Note
JTAG external clock to output high impedance: Boundary-scan data TDO	t_{JTKLDZ} t_{JTKLOZ}	2 2	19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 34). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

This figure provides the AC test load for TDO and the boundary-scan outputs.

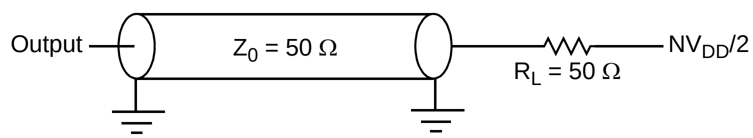

Figure 41. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

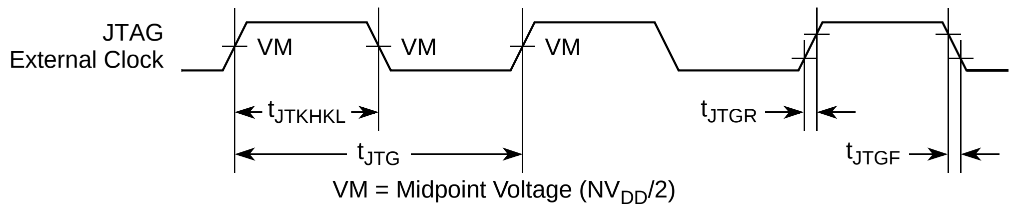

Figure 42. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

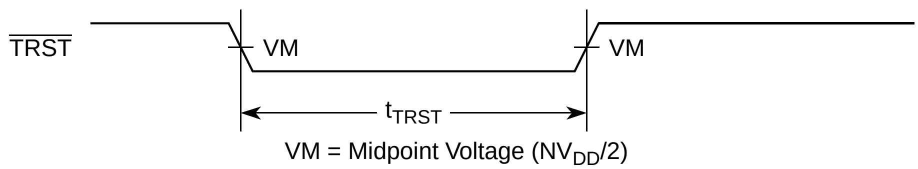

Figure 43. $\overline{\text{TRST}}$ Timing Diagram

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TSEC1_TXD1/TSEC_1588_PP2	AD6	O	LV_{DDB}	—
TSEC1_TXD0/USBDR_STP/TSEC_1588_PP3	AD5	O	LV_{DDB}	—
TSEC1_TX_EN/TSEC_1588_ALARM1	AB7	O	LV_{DDB}	—
TSEC1_TX_ER/TSEC_1588_ALARM2	AB8	O	LV_{DDB}	—
TSEC1_GTX_CLK125	AE1	I	LV_{DDB}	—
TSEC1_MDC/LB_POR_CFG_BOOT_ECC_DIS	AF6	O	NV_{DD}	9, 11
TSEC1_MDIO	AB9	I/O	NV_{DD}	—
ETSEC2				
TSEC2_COL/GTM1_TIN4/GTM2_TIN3/GPIO15	AB4	I/O	LV_{DDA}	—
TSEC2_CRS/$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$/GPIO16	AB3	I/O	LV_{DDA}	—
TSEC2_GTX_CLK/$\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$/GPIO17	AC1	I/O	LV_{DDA}	12
TSEC2_RX_CLK/GTM1_TIN2/GTM2_TIN1/GPIO18	AC2	I/O	LV_{DDA}	—
TSCE2_RX_DV/$\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$/GPIO19	AA3	I/O	LV_{DDA}	—
TSEC2_RXD3/GPIO20	Y5	I/O	LV_{DDA}	—
TSEC2_RXD2/GPIO21	AA4	I/O	LV_{DDA}	—
TSEC2_RXD1/GPIO22	AB2	I/O	LV_{DDA}	—
TSEC2_RXD0/GPIO23	AA5	I/O	LV_{DDA}	—
TSEC2_RX_ER/$\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$/GPIO24	AA2	I/O	LV_{DDA}	—
TSEC2_TX_CLK/GPIO25	AB1	I/O	LV_{DDA}	—
TSEC2_TXD3/CFG_RESET_SOURCE0	W3	I/O	LV_{DDA}	—
TSEC2_TXD2/CFG_RESET_SOURCE1	Y1	I/O	LV_{DDA}	—
TSEC2_TXD1/CFG_RESET_SOURCE2	W5	I/O	LV_{DDA}	—
TSEC2_TXD0/CFG_RESET_SOURCE3	Y3	I/O	LV_{DDA}	—
TSEC2_TX_EN/GPIO26	AA1	I/O	LV_{DDA}	—
TSEC2_TX_ER/GPIO27	W1	I/O	LV_{DDA}	—
SGMII PHY				
TXA	U3	O		—
$\overline{\text{TXA}}$	V3	O		—
RXA	U1	I		—
$\overline{\text{RXA}}$	V1	I		—
TXB	P4	O		—
$\overline{\text{TXB}}$	N4	O		—

Table 65. System PLL Multiplication Factors (continued)

RCWL[SPMF]	System PLL Multiplication Factor
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

Note:

1. If RCWL[DDRCM] and RCWL[LBCM] are both cleared, the system PLL VCO frequency = (CSB frequency) × (System PLL VCO Divider).
2. If either RCWL[DDRCM] or RCWL[LBCM] are set, the system PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO Divider).
3. The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz

As described in Section 20, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (SYS_CLK_IN or PCI_SYNC_IN) and the internal coherent system bus clock (*csb_clk*). This table shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN/PCI_SYNC_IN ratios.

Table 66. CSB Frequency Options

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* :Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			24	25	33.33	66.67
			csb_clk Frequency (MHz)			
High	0010	2:1				133
High	0011	3:1			100	
High	0100	4:1		100	133	
High	0101	5:1	120	125	167	
High	0110	6:1	144	150		
Low	0010	2:1				133
Low	0011	3:1			100	
Low	0100	4:11		100	133	
Low	0101	5:1	120	125	167	
Low	0110	6:1	144	150		

1 CFG_CLKIN_DIV select the ratio between SYS_CLK_IN and PCI_SYNC_OUT.

2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Table 69. Package Thermal Characteristics for TEPBGAII (continued)

Characteristic	Board Type	Symbol	TEPBGA II	Unit	Note
Junction-to-case	—	$R_{\theta JC}$	8	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	7	°C/W	6

Note:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

21.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

21.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)
T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

21.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter

24 Revision History

This table summarizes a revision history for this document.

Table 73. Document Revision History

Rev. Number	Date	Substantive Change(s)
4	11/2011	• In Table 2, added following notes: – Note 3: Min temperature is specified with T_A; Max temperature is specified with T_J – Note 4: All Power rails must be connected and power applied to the MPC8313 even if the IP interfaces are not used. – Note 5: All I/O pins should be interfaced with peripherals operating at same voltage level. – Note 6: This voltage is the input to the filter discussed in Section 22.2, “PLL Power Supply Filtering.” and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter • Decoupled PCI_CLK and SYS_CLK_IN rise and fall times in Table 8. Relaxed maximum rise/fall time of SYS_CLK_IN to 4ns. • Added a note in Table 27 stating “The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm." • In Table 30: – Changed max value of t_{skrgt} in “Data to clock input skew (at receiver)” row from 2.8 to 2.6. – Added Note 7, stating that, “The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm.” • Added a note stating “eTSEC should be interfaced with peripheral operating at same voltage level” in Section 8.1.1, “TSEC DC Electrical Characteristics.” • TSEC1_MDC and TSEC_MDIO are powered at 3.3V by NVDD. Replaced LVDDA/LVDDB with NVDD and removed instances of 2.5V at several places in Section 8.5, “Ethernet Management Interface Electrical Characteristics.” • In Table 43, changed min/max values of t_{CLK_TOL} from 0.05 to 0.005. • In Table 62: – Added Note 2 for LGPL4 in showing LGPL4 as open-drain. – Removed Note 2 from TSEC1_MDIO. – Added Note 10: This pin has an internal pull-up. – Added Note 11: This pin has an internal pull-down. – Added Note 12: “In MII mode, GTX_CLK should be pulled down by 300 Ω to V_{SS}” to TSEC1_GTX_CLK and TSEC2_GTX_CLK. • In Section 19.1, “Package Parameters for the MPC8313E TEPBGAII,” replaced "5.5 Sn/0.5 Cu/4 Ag" with "Sn/3.5 Ag." • Added foot note 3 in Table 65 stating “The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.” • In Table 72: – Added AD = 266 and D = 266. – Added “C = 2.2” in “Revision level” column. – Added Note 4. • Changed resitor from 1.0 Ω to 10 Ω in Figure 58. • Replaced LCCR with LCRR throughout. • Added high-speed to USB Phy description.
3	01/2009	• Table 72, in column aa, changed to AG = 400 MHz.
2.2	12/2008	• Made cross-references active for sections, figures, and tables.
2.1	12/2008	• Added Figure 2, after Table 2 and renumbered the following figures.

Table 73. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
1	3/2008	• In Table 63, added LBC_PM_REF_10 & LSRCID3 as muxed with USBDR_PCTL1 • In Table 63, added LSRCID2 as muxed with USBDR_PCTL0 • In Table 63, added LSRCID1 as muxed with USBDR_PWRFAULT • In Table 63, added LSRCID0 as muxed with USBDR_DRIVE_VBUS • In Table 63, moved T1, U2,& V2 from V_{DD} to XCOREVDD. • In Table 63, moved P2, R2, & T3 from V_{SS} to XCOREVSS. • In Table 63, moved P5, & U4 from V_{DD} to XPADVDD. • In Table 63, moved P3, & V4 from V_{SS} to XPADVSS. • In Table 63, removed “Double with pad” for AV_{DD1} and AV_{DD2} and moved AV_{DD1} and AV_{DD2} to Power and Ground Supplies section • In Table 63, added impedance control requirements for SD_IMP_CAL_TX (100 ohms to GND) and SD_IMP_CAL_RX (200 ohms to GND). • In Table 63, updated muxing in pinout to show new options for selecting IEEE 1588 functionality. Added footnote 8 • In Table 63, updated muxing in pinout to show new LBC ECC boot enable control muxed with eTSEC1_MDC • Added pin type information for power supplies. • Removed N1 and N3 from Vss section of Table 63. Added Therm0 and Therm1 (N1 and N3, respectively). Added note 7 to state: “Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.” • In Table 65 corrected maximum frequency of Local Bus Frequency from “33–66” to 66 MHz • In Table 65 corrected maximum frequency of PCI from “24–66” to 66 MHz • Added “which is determined by RCWLR[COREPLL],” to the note in Section 20.2, “Core PLL Configuration” about the VCO divider. • Added “(VCOD)” next to VCO divider column in Table 68. Added footnote stating that core_clk frequency must not exceed its maximum, so 2.5:1 and 3:1 *core_clk:csb_clk* ratios are invalid for certain *csb_clk* values. • In Table 69, notes were confusing. Added note 3 for VCO column, note 4 for CSB (*csb_clk*) column, note 5 for USB ref column, and note 6 to replace “Note 1”. Clarified note 4 to explain erratum eTSEC40. • In Table 69, updated note 6 to specify USB reference clock frequencies limited to 24 and 48 for rev. 2 silicon. • Replaced Table 71 “Thermal Resistance for TEPBGAII with Heat Sink in Open Flow”. • Removed last row of Table 19. • Removed 200 MHz rows from Table 21 and Table 5. • Changed VIH minimum spec from 2.0 to 2.1 for clock, PIC, JTAG, SPI, and reset pins in Table 9, Table 47, Table 54, Table 59, and Table 61. • Added Figure 4 showing the DDR input timing diagram. • In Table 19, removed “MDM” from the “MDQS-MDQ/MECC/MDM” text under the Parameter column for the tCISKEW parameter. MDM is an output signal and should be removed from the input AC timing spec table (tCISKEW). • Added “and power” to rows 2 and 3 in Table 10 • Added the sentence “Once both the power supplies...” and PORESET to Section 2.2, “Power Sequencing,” and Figure 3. • In Figure 35, corrected “USB0_CLK/USB1_CLK/DR_CLK” with “USBDR_CLK” • In Table 42, clarified that AC specs are for ULPI only.
0	6/2007	Initial release.