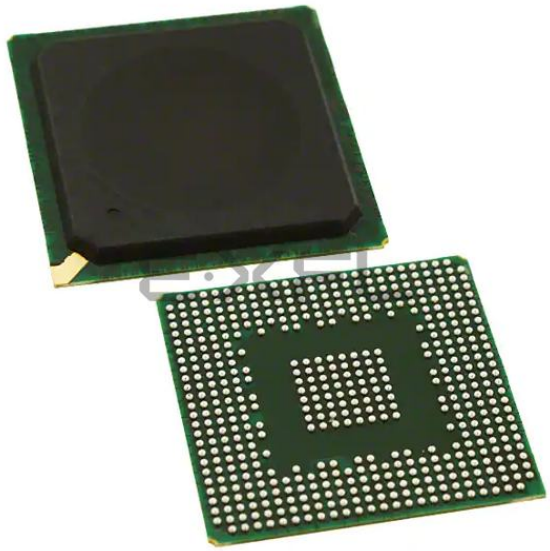

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8313czqaffb

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value[1]	Unit	Current Requirement
Core supply voltage	V_{DD}	1.0 V ± 50 mV	V	469 mA
Internal core logic constant power	V_{DDC}	1.0 V ± 50 mV	V	377 mA
SerDes internal digital power	$XCOREV_{DD}$	1.0	V	170 mA
SerDes internal digital ground	$XCOREV_{SS}$	0.0	V	—
SerDes I/O digital power	$XPADV_{DD}$	1.0	V	10 mA
SerDes I/O digital ground	$XPADV_{SS}$	0.0	V	—
SerDes analog power for PLL	$SDAV_{DD}$	1.0 V ± 50 mV	V	10 mA
SerDes analog ground for PLL	$SDAV_{SS}$	0.0	V	—
Dedicated 3.3 V analog power for USB PLL	USB_PLL_PWR3	3.3 V ± 300 mV	V	2–3 mA
Dedicated 1.0 V analog power for USB PLL	USB_PLL_PWR1	1.0 V ± 50 mV	V	2–3 mA
Dedicated analog ground for USB PLL	USB_PLL_GND	0.0	V	—
Dedicated USB power for USB bias circuit	USB_VDDA_BIAS	3.3 V ± 300 mV	V	4–5 mA
Dedicated USB ground for USB bias circuit	USB_VSSA_BIAS	0.0	V	—
Dedicated power for USB transceiver	USB_VDDA	3.3 V ± 300 mV	V	75 mA
Dedicated ground for USB transceiver	USB_VSSA	0.0	V	—
Analog power for e300 core APLL	AV_{DD1} [6]	1.0 V ± 50 mV	V	2–3 mA
Analog power for system APLL	AV_{DD2} [6]	1.0 V ± 50 mV	V	2–3 mA
DDR1 DRAM I/O voltage (333 MHz, 32-bit operation)	GV_{DD}	2.5 V ± 125 mV	V	131 mA
DDR2 DRAM I/O voltage (333 MHz, 32-bit operation)	GV_{DD}	1.8 V ± 80 mV	V	140 mA
Differential reference voltage for DDR controller	MV_{REF}	1/2 DDR supply ($0.49 \times GV_{DD}$ to $0.51 \times GV_{DD}$)	V	—
Standard I/O voltage	NV_{DD}	3.3 V ± 300 mV[2]	V	74 mA
eTSEC2 I/O supply	LV_{DDA}	2.5 V ± 125 mV/ 3.3 V ± 300 mV	V	22 mA
eTSEC1/USB DR I/O supply	LV_{DDB}	2.5 V ± 125 mV/ 3.3 V ± 300 mV	V	44 mA
Supply for eLBC IOs	LV_{DD}	3.3 V ± 300 mV	V	16 mA
Analog and digital ground	V_{SS}	0.0	V	—
Junction temperature range	T_A/T_J [3]	0 to 105	°C	

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all the media independent interface (MII), reduced gigabit media independent interface (RGMII), serial gigabit media independent interface (SGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the MII interface can be operated at 3.3 V. The RMII and SGMII interfaces can be operated at either 3.3 or 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for *Gigabit Ethernet Physical Layer Device Specification Version 1.2*a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.5, "Ethernet Management Interface Electrical Characteristics."

8.1.1 TSEC DC Electrical Characteristics

All RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

NOTE

eTSEC should be interfaced with peripheral operating at same voltage level.

Table 24. MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DDA}/LV_{DDB}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LV_{DDA} or LV_{DDB} = Min	2.40	LV_{DDA} + 0.3 or LV_{DDB} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LV_{DDA} or LV_{DDB} = Min	V_{SS}	0.50	V
Input high voltage	V_{IH}	—	—	2.0	LV_{DDA} + 0.3 or LV_{DDB} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DDA} or LV_{DDB}		—	40	μA
Input low current	I_{IL}	V_{IN}[1] = VSS		–600	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 25. RGMII/RTBI DC Electrical Characteristics

Parameters	Symbol	Conditions	Min	Max	Unit
Supply voltage 2.5 V	LV_{DDA}/LV_{DDB}	—	2.37	2.63	V

8.2.2 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 30. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{DDB} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–0.5	—	0.5	ns
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.6	ns
Clock cycle duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Note:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the RTBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is $LV_{DDA}/2$ or $LV_{DDB}/2$.
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
7. The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

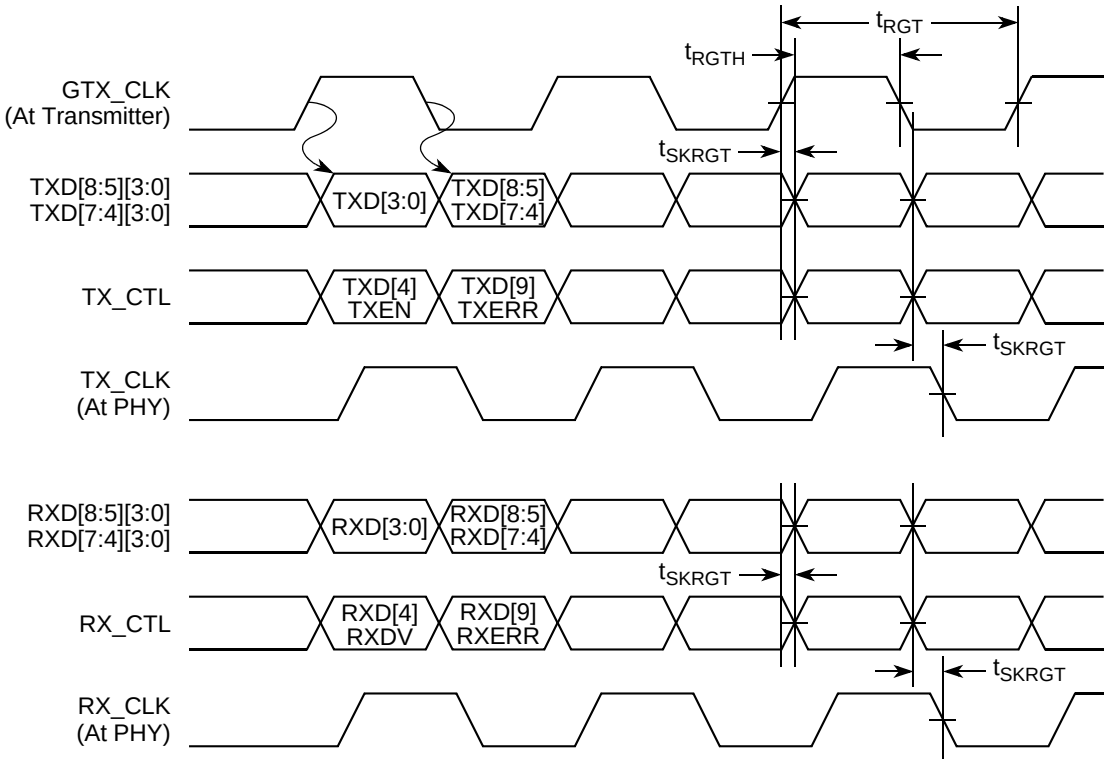


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-coupled serial link from the dedicated SerDes interface of MPC8313E as shown in Figure 15, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features a 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XCOREVSS. The reference circuit of the SerDes transmitter and receiver is shown in Figure 33.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in Section 22.5, "Connection Recommendations," as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the TSEC_GTX_CLK125 clock is not required for this port. Instead, the SerDes reference clock is required on SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ pins.

8.3.1 DC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 9, "High-Speed Serial Interfaces (HSSI)."

8.3.2 AC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

This table lists the SGMII SerDes reference clock AC requirements. Note that SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Table 31. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit
t_{REF}	REFCLK cycle time	—	8	—	ns
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps

8.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 32 and Table 33 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX[*n*] and $\overline{\text{SD\_TX}}$[*n*]) as depicted in Figure 16.

Table 32. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$XCOREV_{DD}$	0.95	1.0	1.05	V	
Output high voltage	V_{OH}	—	—	$XCOREV_{DD\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-max}}/2$	mV	1
Output low voltage	V_{OL}	$XCOREV_{DD\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-max}}/2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	
Output differential voltage[2, 3]	$\lvert V_{OD}\rvert$	323	500	725	mV	Equalization setting: 1.0x
Output offset voltage	V_{OS}	425	500	575	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	
Mismatch in a pair	ΔR_O	—	—	10	%	
Change in V_{OD} between 0 and 1	$\Delta\lvert V_{OD}\rvert$	—	—	25	mV	
Change in V_{OS} between 0 and 1	ΔV_{OS}	—	—	25	mV	
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	

Notes:

1. This will not align to DC-coupled SGMII. $XCOREV_{DD\text{-}Typ}$ = 1.0 V.
2. $\lvert V_{OD}\rvert = \lvert V_{TXn} - V_{\overline{TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $XCOREV_{DD\text{-}Typ}$ = 1.0 V, no common mode offset variation (V_{OS} = 500 mV), SerDes transmitter is terminated with 100-Ω differential load between TX[*n*] and $\overline{\text{TX}}$[*n*].
4. V_{OS} is also referred to as output common mode voltage.

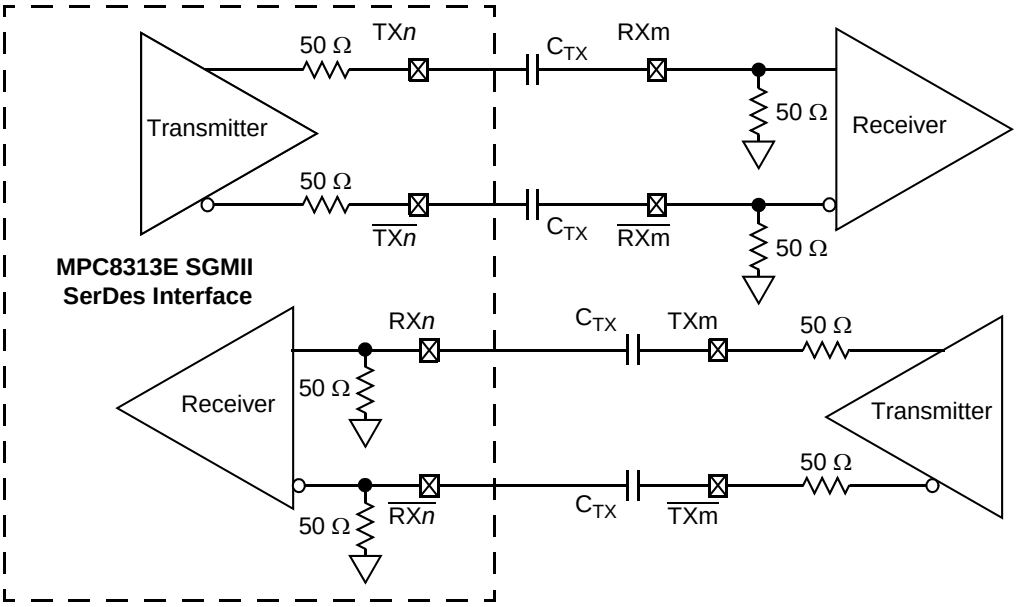


Figure 15. 4-Wire AC-Coupled SGMII Serial Link Connection Example

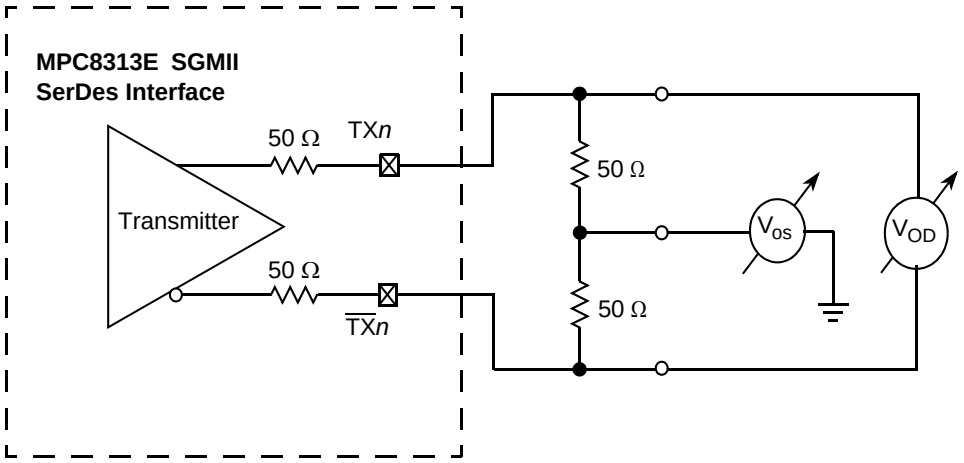


Figure 16. SGMII Transmitter DC Measurement Circuit

Table 33. SGMII DC Receiver Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$XCOREV_{DD}$	0.95	1.0	1.05	V	
DC Input voltage range			N/A			1
Input differential voltage	$V_{RX\_DIFFp\text{-}p}$	100	—	1200	mV	2
Loss of signal threshold	VL_{OS}	30	—	100	mV	
Input AC common mode voltage	$V_{CM\_ACp\text{-}p}$	—	—	100	mV	3
Receiver differential input impedance	Z_{RX_DIFF}	80	100	120	Ω	
Receiver common mode input impedance	Z_{RX_CM}	20	—	35	Ω	

of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

— For external DC-coupled connection, as described in Section 9.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 24 shows the SerDes reference clock input requirement for the DC-coupled connection scheme.

— For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to $XCOREV_{SS}$. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage ($XCOREV_{SS}$). Figure 25 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- Single-ended mode

— The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-to-peak (from V_{min} to V_{max}) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.

— The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 26 shows the SerDes reference clock input requirement for the single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC coupled externally. For the best noise performance, the reference of the clock could be DC or AC coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

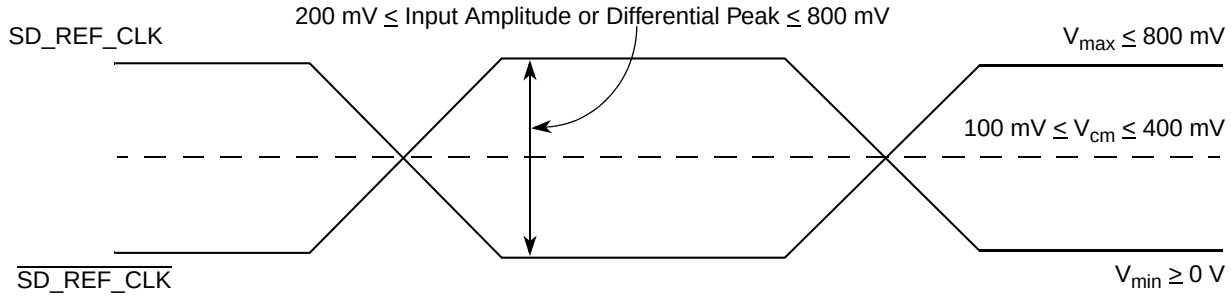


Figure 24. Differential Reference Clock Input DC Requirements (External DC-Coupled)

This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8313E SerDes reference clock input's DC requirement.

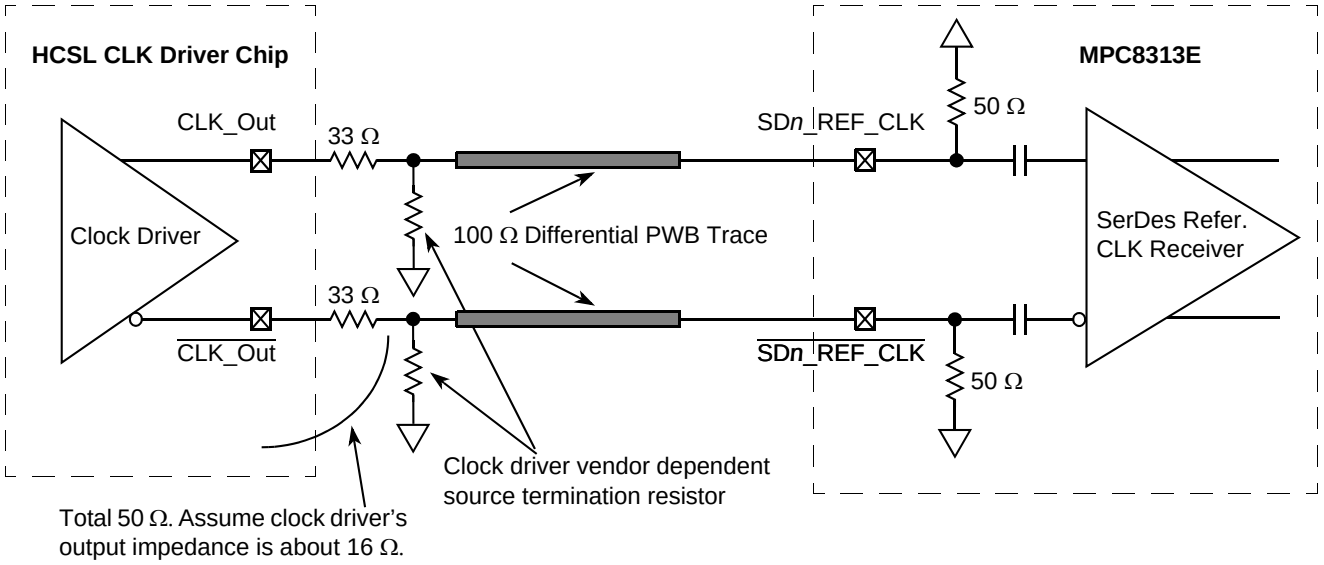


Figure 27. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8313E SerDes reference clock input's allowed range (100 to 400 mV), the AC-coupled connection scheme must be used. It assumes the LVDS output driver features a 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

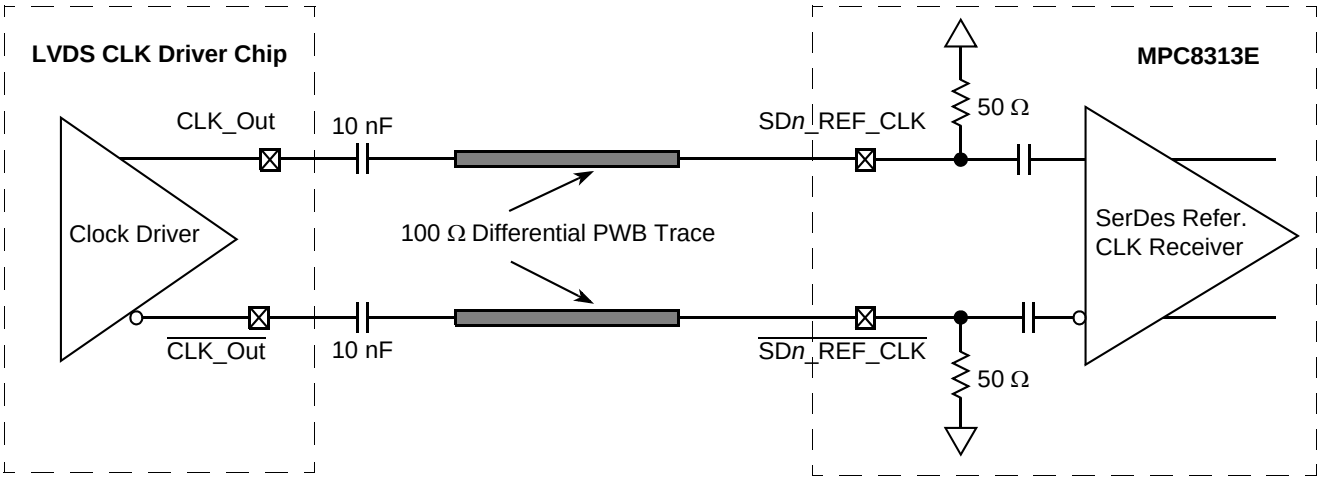


Figure 28. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the MPC8313E SerDes reference clock input's DC requirement, AC coupling has to be used. Figure 29

assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC coupling. Its value could be ranged from 140 to 240 Ω depending on the clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8313E SerDes3 reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Consult with the clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

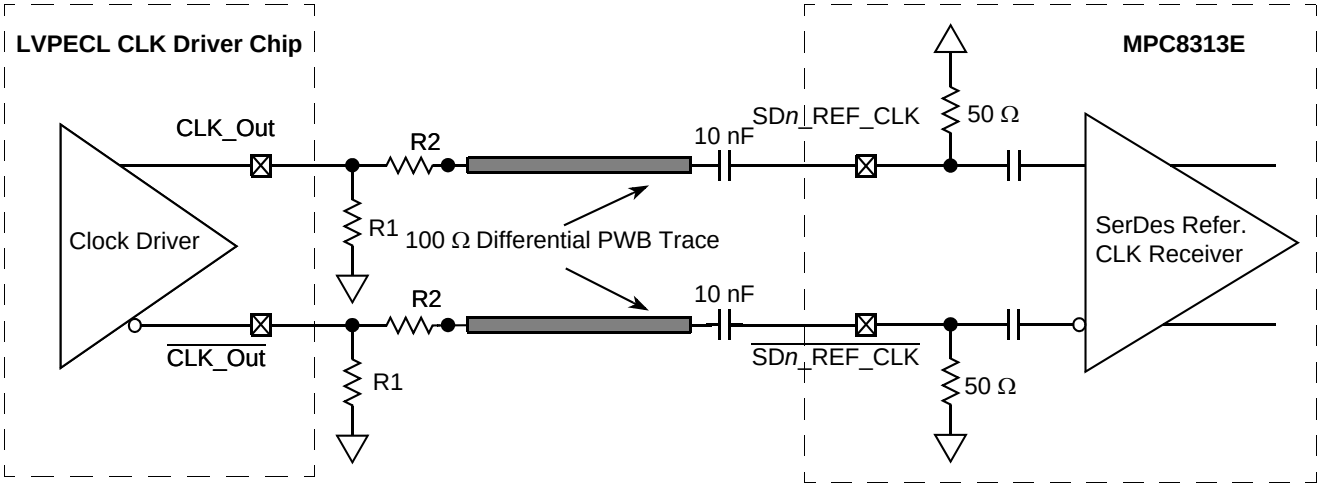


Figure 29. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the MPC8313E SerDes reference clock input's DC requirement.

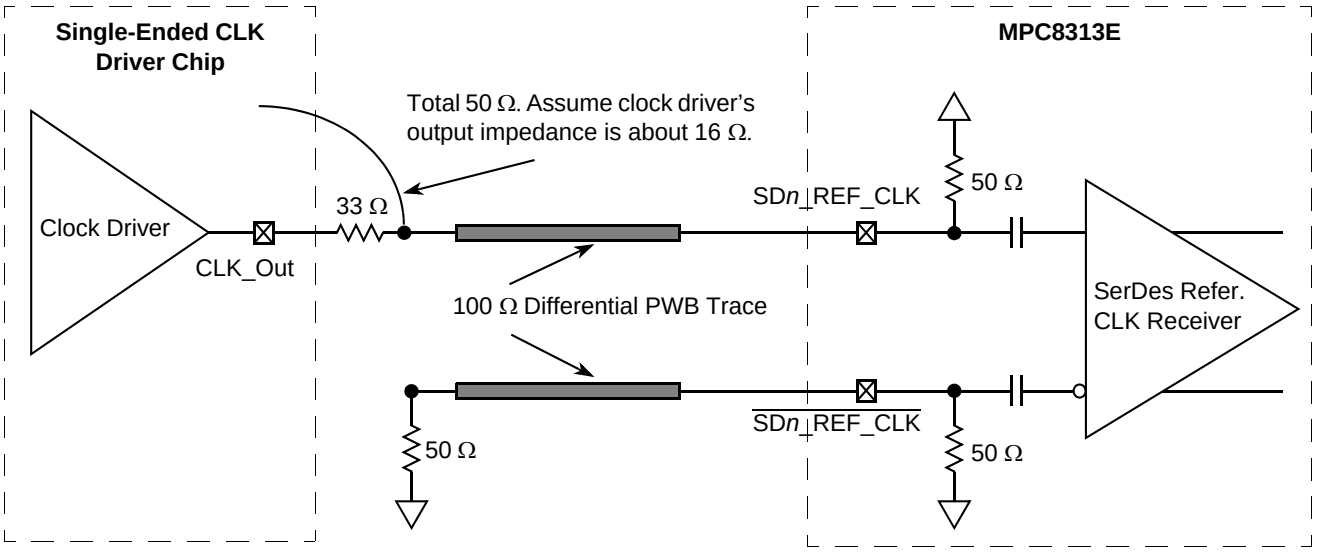


Figure 30. Single-Ended Connection (Reference Only)

11 Enhanced Local Bus

This section describes the DC and AC electrical specifications for the local bus interface.

11.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface.

Table 44. Local Bus DC Electrical Characteristics at 3.3 V

Parameter	Symbol	Min	Max	Unit
High-level input voltage for Rev 1.0	V_{IH}	2.0	LV_{DD} + 0.3	V
High-level input voltage for Rev 2.x or later	V_{IH}	2.1	LV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current, (V_{IN}[1] = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	±5	μA
High-level output voltage, (LV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	LV_{DD} – 0.2	—	V
Low-level output voltage, (LV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.2	V

Note: The parameters stated in above table are valid for all revisions unless explicitly mentioned.

11.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface.

Table 45. Local Bus General Timing Parameters

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
LALE output rise to LCLK negative edge	$t_{LALEHOV}$	—	3.0	ns	
LALE output fall to LCLK negative edge	$t_{LALETOT1}$	–1.5	—	ns	5
LALE output fall to LCLK negative edge	$t_{LALETOT2}$	–5.0	—	ns	6
LALE output fall to LCLK negative edge	$t_{LALETOT3}$	–4.5	—	ns	7
Local bus clock to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD	t_{LBKHOZ}	—	4	ns	8

This figure shows the PCI input AC timing conditions.

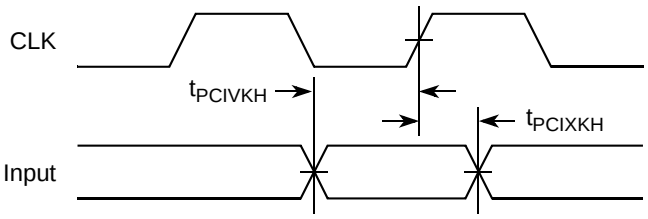


Figure 49. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

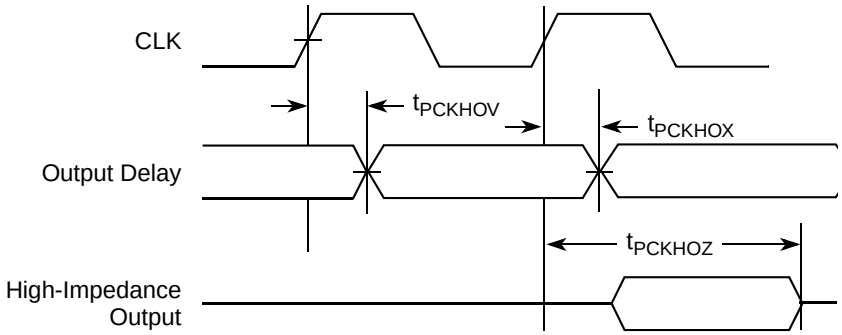


Figure 50. PCI Output AC Timing Measurement Condition

15 Timers

This section describes the DC and AC electrical specifications for the timers.

15.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the MPC8313E timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 53. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	±5	μA

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICOE*n*] parameters select whether the PCI_SYNC_OUT is driven out on the PCI_CLK_OUT*n* signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the SYS_CLK_IN signal should be tied to VSS.

As shown in Figure 57, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbc_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{\text{PCI\_SYNC\_IN} \times (1 + \sim\overline{\text{CFG\_CLKIN\_DIV}})\} \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~$\overline{\text{CFG\_CLKIN\_DIV}}$) is the SYS_CLK_IN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*, for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + \text{RCWL[DDRCM]})$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbc_clk* frequency is determined by the following equation:

$$lbc\_clk = csb\_clk \times (1 + \text{RCWL[LBCM]})$$

Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the a LBC clock divider to create the external local bus clock outputs (LCLK[0:1]). The LBC clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 63 specifies which units have a configurable clock frequency.

Table 65. System PLL Multiplication Factors (continued)

RCWL[SPMF]	System PLL Multiplication Factor
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

Note:
1. If RCWL[DDRCM] and RCWL[LBCM] are both cleared, the system PLL VCO frequency = (CSB frequency) × (System PLL VCO Divider).
2. If either RCWL[DDRCM] or RCWL[LBCM] are set, the system PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO Divider).
3. The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz

As described in Section 20, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (SYS_CLK_IN or PCI_SYNC_IN) and the internal coherent system bus clock (*csb_clk*). This table shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN/PCI_SYNC_IN ratios.

Table 66. CSB Frequency Options

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* :Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			24	25	33.33	66.67
			csb_clk Frequency (MHz)			
High	0010	2:1				133
High	0011	3:1			100	
High	0100	4:1		100	133	
High	0101	5:1	120	125	167	
High	0110	6:1	144	150		
Low	0010	2:1				133
Low	0011	3:1			100	
Low	0100	4:11		100	133	
Low	0101	5:1	120	125	167	
Low	0110	6:1	144	150		

1 CFG_CLKIN_DIV select the ratio between SYS_CLK_IN and PCI_SYNC_OUT.

2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

20.3 Example Clock Frequency Combinations

This table shows several possible frequency combinations that can be selected based on the indicated input reference frequencies, with RCWLR[LBCM] = 0 and RCWLR[DDRCM] =1, such that the LBC operates with a frequency equal to the frequency of *csb_clk* and the DDR controller operates at twice the frequency of *csb_clk*.

Table 68. System Clock Frequencies

						LBC(lbc_clk)				e300 Core(core_clk)				
SYS_ CLK_IN/ PCI_CLK	SPMF[1]	VCOD[2]	VCO[3]	CSB (*csb_clk*)[4]	DDR (ddr_clk)	/2	/4	/8	USB ref[5]	× 1	× 1.5	× 2	× 2.5	× 3
25.0	6	2	600.0	150.0	300.0	—	37.5	18.8	Note[6]	150.0	225	300	375	—
25.0	5	2	500.0	125.0	250.0	62.5	31.25	15.6	Note 6	125.0	188	250	313	375
33.3	5	2	666.0	166.5	333.0	—	41.63	20.8	Note 6	166.5	250	333	—	—
33.3	4	2	532.8	133.2	266.4	66.6	33.3	16.7	Note 6	133.2	200	266	333	400
48.0	3	2	576.0	144.0	288.0	—	36	18.0	48.0	144.0	216	288	360	—
66.7	2	2	533.4	133.3	266.7	66.7	33.34	16.7	Note 6	133.3	200	267	333	400

Note:

1. System PLL multiplication factor.
2. System PLL VCO divider.
3. When considering operating frequencies, the valid core VCO operating range of 400–800 MHz must not be violated.
4. Due to erratum eTSEC40, *csb_clk* frequencies of less than 133 MHz do not support gigabit Ethernet data rates. The core frequency must be 333 MHz for gigabit Ethernet operation. This erratum will be fixed in revision 2 silicon.
5. Frequency of USB PLL input reference.
6. USB reference clock must be supplied from a separate source as it must be 24 or 48 MHz, the USB reference must be supplied from a separate external source using USB_CLK_IN.

21 Thermal

This section describes the thermal specifications of the MPC8313E.

21.1 Thermal Characteristics

This table provides the package thermal characteristics for the 516, 27 × 27 mm TEPBGAII.

Table 69. Package Thermal Characteristics for TEPBGAII

Characteristic	Board Type	Symbol	TEPBGA II	Unit	Note
Junction-to-ambient natural convection	Single layer board (1s)	$R_{\theta JA}$	25	°C/W	1, 2
Junction-to-ambient natural convection	Four layer board (2s2p)	$R_{\theta JA}$	18	°C/W	1, 2, 3
Junction-to-ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	20	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	15	°C/W	1, 3
Junction-to-board	—	$R_{\theta JB}$	10	°C/W	4

Table 69. Package Thermal Characteristics for TEPBGAII (continued)

Characteristic	Board Type	Symbol	TEPBGA II	Unit	Note
Junction-to-case	—	$R_{\theta JC}$	8	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	7	°C/W	6

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

21.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

21.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)
T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

21.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)
T_B = board temperature at the package perimeter (°C)
$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51–8
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

21.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)
T_T = thermocouple temperature on top of package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

21.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to- ambient thermal resistance (°C/W)

21.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

21.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction to case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)
T_C = case temperature of the package
$R_{\theta JC}$ = junction-to-case thermal resistance
P_D = power dissipation

22 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8313E SYS_CLK_IN

22.1 System Clocking

The MPC8313E includes three PLLs.

1. The platform PLL (AV_{DD2}) generates the platform clock from the externally supplied SYS_CLK_IN input in PCI host mode or SYS_CLK_IN/PCI_SYNC_IN in PCI agent mode. The frequency ratio between the platform and SYS_CLK_IN is selected using the platform PLL ratio configuration bits as described in Section 20.1, “System PLL Configuration.”
2. The e300 core PLL (AV_{DD1}) generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 20.2, “Core PLL Configuration.”
3. There is a PLL for the SerDes block.

22.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1}, AV_{DD2}, and $SDAV_{DD}$, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 58, one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

This figure shows the PLL power supply filter circuits.

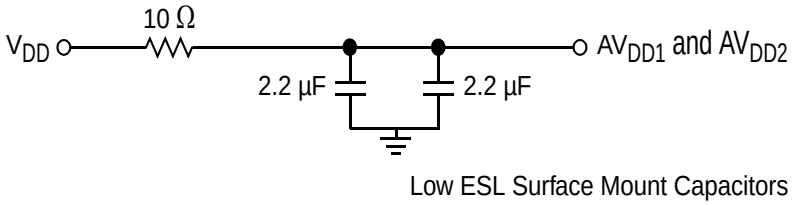
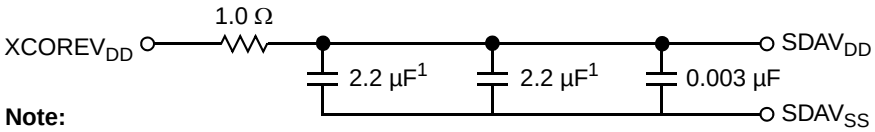


Figure 58. PLL Power Supply Filter Circuit

The $SDAV_{DD}$ signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit like the one shown in Figure 59. For maximum effectiveness, the filter circuit should be placed as closely as possible to the $SDAV_{DD}$ ball to ensure it filters out as much noise as possible. The ground connection should be near the $SDAV_{DD}$ ball. The 0.003-µF capacitor is closest to the ball, followed by the two 2.2-µF capacitors, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from traces from $SDAV_{DD}$ to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.

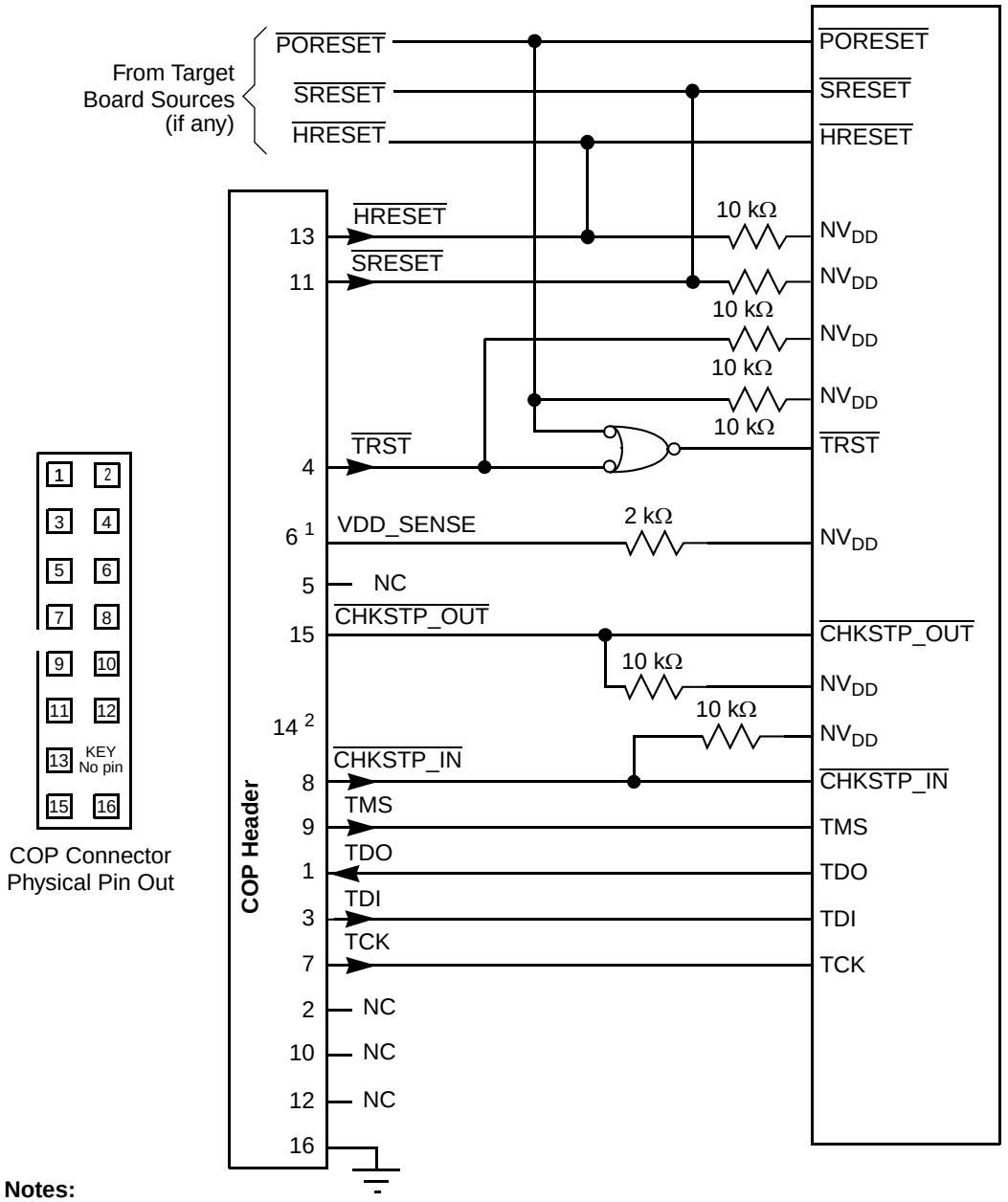


Note:
1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 59. SerDes PLL Power Supply Filter Circuit

Note the following:

- $SDAV_{DD}$ should be a filtered version of $XCOREV_{DD}$.



Notes:
1. Some systems require power to be fed from the application board into the debugger repeater card via the COP header. In this case the resistor value for VDD_SENSE should be around 20 Ω.
2. Key location; pin 14 is not physically present on the COP header.

Figure 61. JTAG Interface Connection

23 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 23.1, “Part Numbers Fully Addressed by this Document.”

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