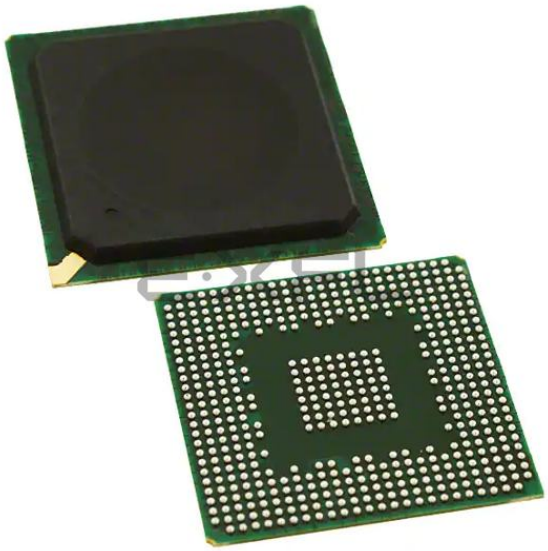

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8313evraffb

1.2 Serial Interfaces

The following interfaces are supported in the MPC8313E: dual UART, dual I^2C, and an SPI interface.

1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE Std 802.11i®, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are as follows:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-224, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

1.4 DDR Memory Controller

The MPC8313E DDR1/DDR2 memory controller includes the following features:

- Single 16- or 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 333 MHz
- Support for two physical banks (chip selects), each bank independently addressable
- 64-Mbit to 2-Gbit (for DDR1) and to 4-Gbit (for DDR2) devices with x8/x16/x32 data ports (no direct x4 support)
- Support for one 16-bit device or two 8-bit devices on a 16-bit bus, or one 32-bit device or two 16-bit devices on a 32-bit bus
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

1.5 PCI Controller

The MPC8313E PCI controller includes the following features:

- PCI specification revision 2.3 compatible
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

- Full and half-duplex Ethernet support (1000 Mbps supports only full-duplex):
  - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE 802.1 virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision
  - CRC generation and verification of inbound/outbound packets
  - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
  - Exact match on primary and virtual 48-bit unicast addresses
    - VRRP and HSRP support for seamless router fail-over
  - Up to 16 exact-match MAC addresses supported
  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status

1.8 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model supports 5 external and 34 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

1.9 Power Management Controller (PMC)

The MPC8313E power management controller includes the following features:

- Provides power management when the device is used in both host and agent modes
- Supports PCI power management 1.2 D0, D1, D2, D3hot, and D3cold states
- On-chip split power supply controlled through external power switch for minimum standby power
- Support for PME generation in PCI agent mode, PME detection in PCI host mode
- Supports wake-up from Ethernet (Magic Packet), USB, GPIO, and PCI (PME input as host)

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Note
Core supply voltage		V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage		AV_{DD}	–0.3 to 1.26	V	—
Core power supply for SerDes transceivers		$XCOREV_{DD}$	–0.3 to 1.26	V	—
Pad power supply for SerDes transceivers		$XPADV_{DD}$	–0.3 to 1.26	V	—
DDR and DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		NV_{DD}/LV_{DD}	–0.3 to 3.6	V	—
eTSEC, USB		LV_{DDA}/LV_{DDB}	–0.3 to 3.6	V	—
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Enhanced three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DDA} + 0.3) or –0.3 to (LV_{DDB} + 0.3)	V	4, 5
	Local bus, DUART, SYS_CLK_IN, system control, and power management, I^2C, and JTAG signals	NV_{IN}	–0.3 to (NV_{DD} + 0.3)	V	3, 5
	PCI	NV_{IN}	–0.3 to (NV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** NV_{IN} must not exceed NV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DDA}/LV_{DDB} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the MPC8313E. Note that the values in this table are the recommended and tested operating conditions. If a particular block is given a voltage falling within the range in the Recommended Value column, the MPC8313E is capable of delivering the amount of current listed in the Current Requirement column; this is the maximum current possible. Proper device operation outside of these conditions is not guaranteed.

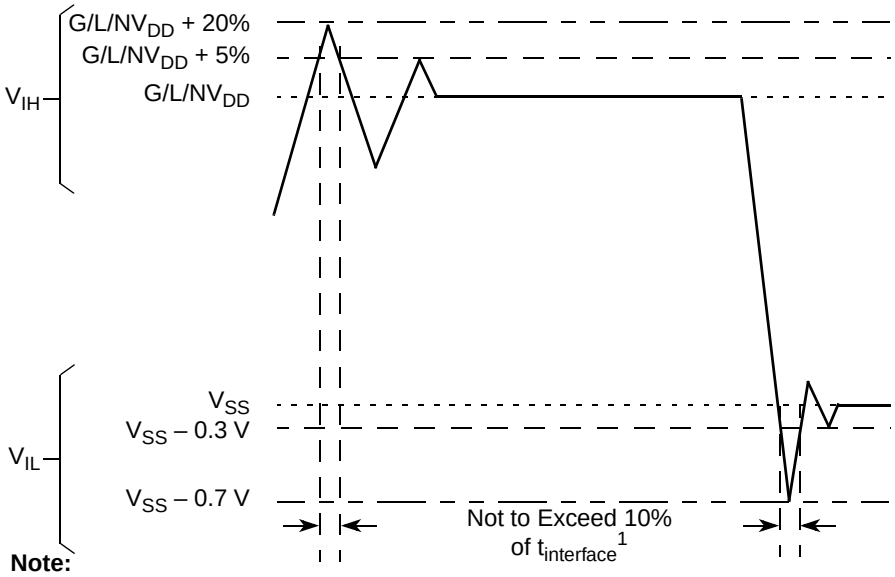
Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value[1]	Unit	Current Requirement

Note:

1. GV_{DD}, NV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. Some GPIO pins may operate from a 2.5-V supply when configured for other functions.
3. Min temperature is specified with T_A; Max temperature is specified with T_J.
4. All Power rails must be connected and power applied to the MPC8313 even if the IP interfaces are not used.
5. All I/O pins should be interfaced with peripherals operating at same voltage level.
6. This voltage is the input to the filter discussed in Section 22.2, "PLL Power Supply Filtering" and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter.

This figure shows the undershoot and overshoot voltages at the interfaces of the MPC8313E.



Note:

1. Note that $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/NV_{DD}/LV_{DD}

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	NV_{DD} = 3.3 V
PCI signals	25	
DDR signal	18	GV_{DD} = 2.5 V

This table provides the input AC timing specifications for the DDR SDRAM when GV_{DD}(typ) = 2.5 V.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	—

This table provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions. with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ	t_{CISKEW}	—	—	ps	1, 2
333 MHz	—	–750	750	—	—
266 MHz	—	–750	750	—	—

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[*n*] and any corresponding bit that is captured with MDQS[*n*]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

This figure illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

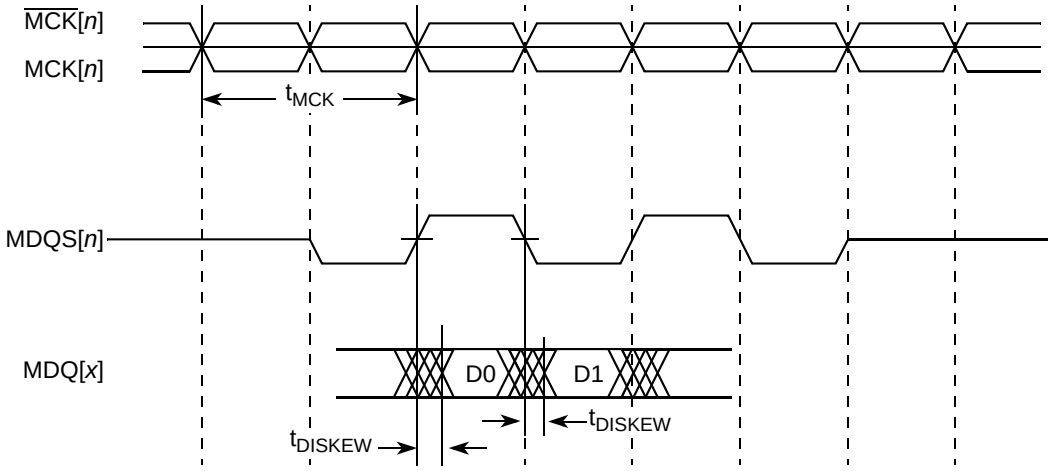


Figure 4. DDR Input Timing Diagram

8.2.1.4 RMII Receive AC Timing Specifications

This table provides the RMII receive AC timing specifications.

Table 29. RMII Receive AC Timing Specifications

At recommended operating conditions with NV_{DD} of 3.3 V ± 0.3 V.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This table provides the AC test load.

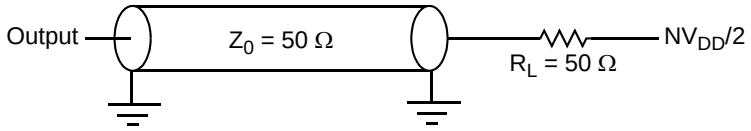


Figure 12. AC Test Load

This table shows the RMII receive AC timing diagram.

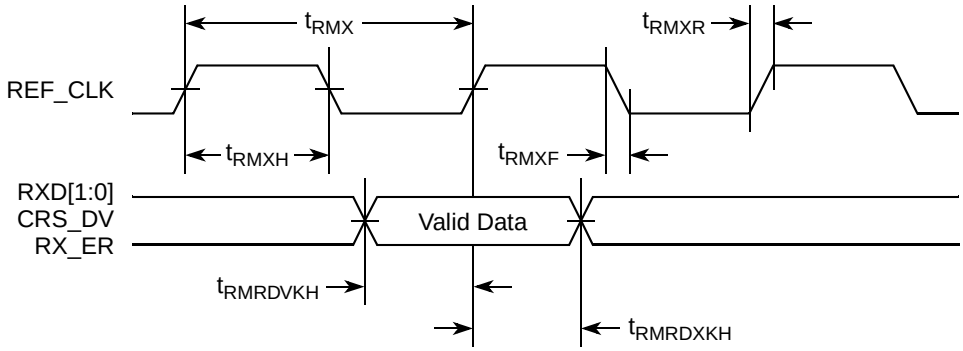


Figure 13. RMII Receive AC Timing Diagram

8.2.2 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 30. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{DDB} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–0.5	—	0.5	ns
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.6	ns
Clock cycle duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Note:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the RTBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is $LV_{DDA}/2$ or $LV_{DDB}/2$.
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
7. The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm

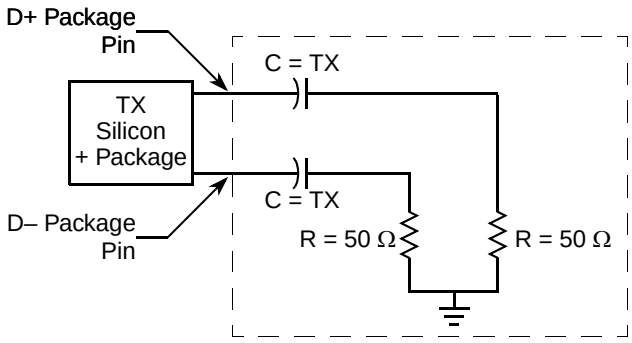
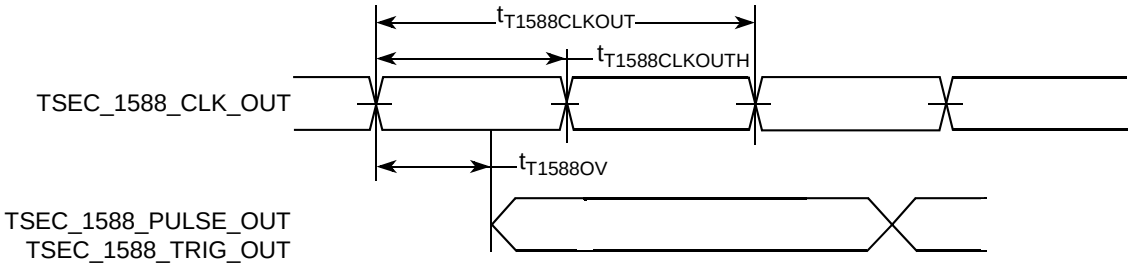


Figure 18. SGMII AC Test/Measurement Load

8.4 eTSEC IEEE 1588 AC Specifications

This figure provides the data and command output timing diagram.



Note: The output delay is count starting rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is count starting falling edge.

Figure 19. eTSEC IEEE 1588 Output AC Timing

This figure provides the data and command input timing diagram.

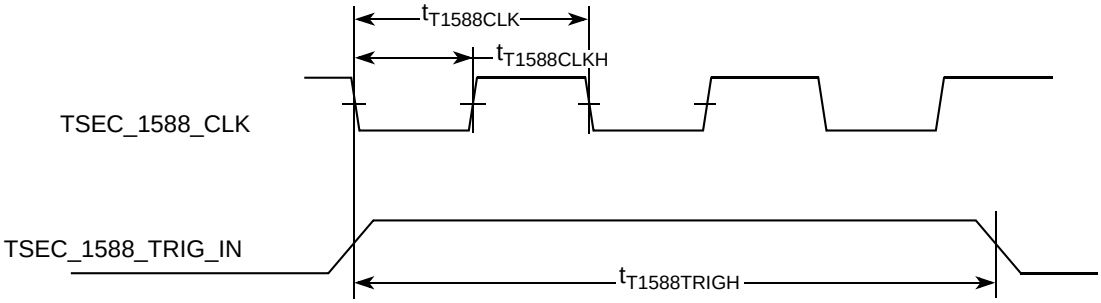


Figure 20. eTSEC IEEE 1588 Input AC Timing

This table lists the IEEE 1588 AC timing specifications.

Table 36. eTSEC IEEE 1588 AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.8	—	$T_{RX\_CLK} \times 9$	ns	1, 3
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	

Table 37. MII Management DC Electrical Characteristics When Powered at 3.3 V (continued)

Note:
1. Note that the symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

8.5.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 38. MII Management AC Timing Specifications

At recommended operating conditions with NV_{DD} is 3.3 V ± 0.3V

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO delay	t_{MDKHDX}	10	—	170	ns	
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	
MDC fall time	t_{MDHF}	—	—	10	ns	

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)

This figure shows the MII management AC timing diagram.

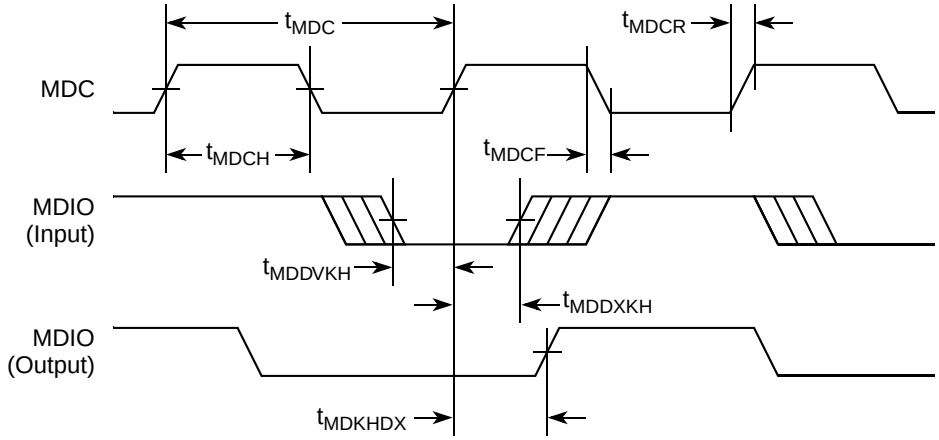


Figure 21. MII Management Interface Timing Diagram

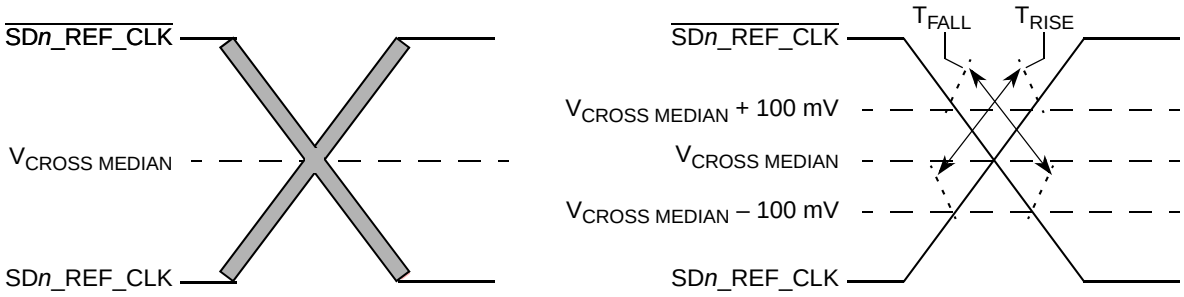


Figure 32. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. Refer to the following section for detailed information:

- Section 8.3.2, "AC Requirements for SGMII SD_REF_CLK and SD_REF_CLK"

9.2.4.1 Spread Spectrum Clock

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

9.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for the SerDes data lane's transmitter and receiver.

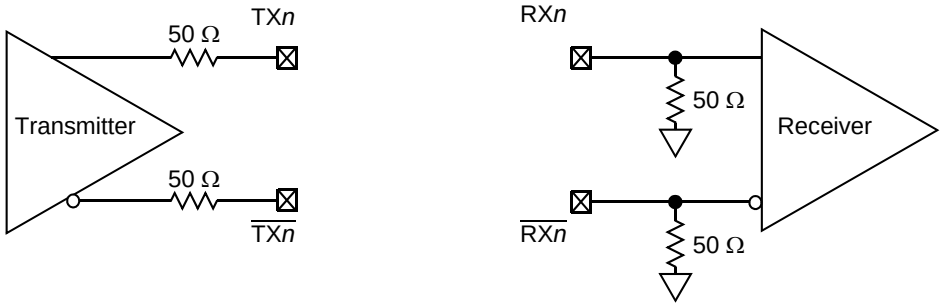


Figure 33. SerDes Transmitter and Receiver Reference Circuits

The SerDes data lane's DC and AC specifications are defined in the interface protocol section listed below (SGMII) based on the application usage:

- Section 8.3, "SGMII Interface Electrical Characteristics"

Please note that a external AC-coupling capacitor is required for the above serial transmission protocol with the capacitor value defined in the specifications of the protocol section.

17 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

17.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins.

Table 58. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

17.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 59. IPIC Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Note:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

18 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8313E.

18.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the MPC8313E SPI.

Table 60. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

19.3 Pinout Listings

This table provides the pin-out listing for the MPC8313E, TEPBGAII package.

Table 62. MPC8313E TEPBGAII Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Note
DDR Memory Controller Interface				
MEMC_MDQ0	A8	I/O	GV_{DD}	—
MEMC_MDQ1	A9	I/O	GV_{DD}	—
MEMC_MDQ2	C10	I/O	GV_{DD}	—
MEMC_MDQ3	C9	I/O	GV_{DD}	—
MEMC_MDQ4	E9	I/O	GV_{DD}	—
MEMC_MDQ5	E11	I/O	GV_{DD}	—
MEMC_MDQ6	E10	I/O	GV_{DD}	—
MEMC_MDQ7	C8	I/O	GV_{DD}	—
MEMC_MDQ8	E8	I/O	GV_{DD}	—
MEMC_MDQ9	A6	I/O	GV_{DD}	—
MEMC_MDQ10	B6	I/O	GV_{DD}	—
MEMC_MDQ11	C6	I/O	GV_{DD}	—
MEMC_MDQ12	C7	I/O	GV_{DD}	—
MEMC_MDQ13	D7	I/O	GV_{DD}	—
MEMC_MDQ14	D6	I/O	GV_{DD}	—
MEMC_MDQ15	A5	I/O	GV_{DD}	—
MEMC_MDQ16	A19	I/O	GV_{DD}	—
MEMC_MDQ17	D18	I/O	GV_{DD}	—
MEMC_MDQ18	A17	I/O	GV_{DD}	—
MEMC_MDQ19	E17	I/O	GV_{DD}	—
MEMC_MDQ20	E16	I/O	GV_{DD}	—
MEMC_MDQ21	C18	I/O	GV_{DD}	—
MEMC_MDQ22	D19	I/O	GV_{DD}	—
MEMC_MDQ23	C19	I/O	GV_{DD}	—
MEMC_MDQ24	E19	I/O	GV_{DD}	—
MEMC_MDQ25	A22	I/O	GV_{DD}	—
MEMC_MDQ26	C21	I/O	GV_{DD}	—
MEMC_MDQ27	C20	I/O	GV_{DD}	—
MEMC_MDQ28	A21	I/O	GV_{DD}	—

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MEMC_MDQ29	A20	I/O	GV_{DD}	—
MEMC_MDQ30	C22	I/O	GV_{DD}	—
MEMC_MDQ31	B22	I/O	GV_{DD}	—
MEMC_MDM0	B7	O	GV_{DD}	—
MEMC_MDM1	E6	O	GV_{DD}	—
MEMC_MDM2	E18	O	GV_{DD}	—
MEMC_MDM3	E20	O	GV_{DD}	—
MEMC_MDQS0	A7	I/O	GV_{DD}	—
MEMC_MDQS1	E7	I/O	GV_{DD}	—
MEMC_MDQS2	B19	I/O	GV_{DD}	—
MEMC_MDQS3	A23	I/O	GV_{DD}	—
MEMC_MBA0	D15	O	GV_{DD}	—
MEMC_MBA1	A18	O	GV_{DD}	—
MEMC_MBA2	A15	O	GV_{DD}	—
MEMC_MA0	E12	O	GV_{DD}	—
MEMC_MA1	D11	O	GV_{DD}	—
MEMC_MA2	B11	O	GV_{DD}	—
MEMC_MA3	A11	O	GV_{DD}	—
MEMC_MA4	A12	O	GV_{DD}	—
MEMC_MA5	E13	O	GV_{DD}	—
MEMC_MA6	C12	O	GV_{DD}	—
MEMC_MA7	E14	O	GV_{DD}	—
MEMC_MA8	B15	O	GV_{DD}	—
MEMC_MA9	C17	O	GV_{DD}	—
MEMC_MA10	C13	O	GV_{DD}	—
MEMC_MA11	A16	O	GV_{DD}	—
MEMC_MA12	C15	O	GV_{DD}	—
MEMC_MA13	C16	O	GV_{DD}	—
MEMC_MA14	E15	O	GV_{DD}	—
$\overline{\text{MEMC\_MWE}}$	B18	O	GV_{DD}	—
$\overline{\text{MEMC\_MRAS}}$	C11	O	GV_{DD}	—
$\overline{\text{MEMC\_MCAS}}$	B10	O	GV_{DD}	—

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TMS	E4	I	NV_{DD}	4
$\overline{\text{TRST}}$	E5	I	NV_{DD}	4
TEST				
TEST_MODE	F4	I	NV_{DD}	6
DEBUG				
$\overline{\text{QUIESCE}}$	F5	O	NV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	F2	I/O	NV_{DD}	1
$\overline{\text{PORESET}}$	F3	I	NV_{DD}	—
$\overline{\text{SRESET}}$	F1	I	NV_{DD}	—
Clocks				
SYS_CR_CLK_IN	U26	I	NV_{DD}	—
SYS_CR_CLK_OUT	U25	O	NV_{DD}	—
SYS_CLK_IN	U23	I	NV_{DD}	—
USB_CR_CLK_IN	T26	I	NV_{DD}	—
USB_CR_CLK_OUT	R26	O	NV_{DD}	—
USB_CLK_IN	T22	I	NV_{DD}	—
PCI_SYNC_OUT	U24	O	NV_{DD}	3
RTC_PIT_CLOCK	R22	I	NV_{DD}	—
PCI_SYNC_IN	T24	I	NV_{DD}	—
MISC				
THERM0	N1	I	NV_{DD}	7
THERM1	N3	I	NV_{DD}	7
PCI				
$\overline{\text{PCI\_INTA}}$	AF7	O	NV_{DD}	—
$\overline{\text{PCI\_RESET\_OUT}}$	AB11	O	NV_{DD}	—
PCI_AD0	AB20	I/O	NV_{DD}	—
PCI_AD1	AF23	I/O	NV_{DD}	—
PCI_AD2	AF22	I/O	NV_{DD}	—
PCI_AD3	AB19	I/O	NV_{DD}	—
PCI_AD4	AE22	I/O	NV_{DD}	—
PCI_AD5	AF21	I/O	NV_{DD}	—

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_AD6	AD19	I/O	NV_{DD}	—
PCI_AD7	AD20	I/O	NV_{DD}	—
PCI_AD8	AC18	I/O	NV_{DD}	—
PCI_AD9	AD18	I/O	NV_{DD}	—
PCI_AD10	AB18	I/O	NV_{DD}	—
PCI_AD11	AE19	I/O	NV_{DD}	—
PCI_AD12	AB17	I/O	NV_{DD}	—
PCI_AD13	AE18	I/O	NV_{DD}	—
PCI_AD14	AD17	I/O	NV_{DD}	—
PCI_AD15	AF19	I/O	NV_{DD}	—
PCI_AD16	AB14	I/O	NV_{DD}	—
PCI_AD17	AF15	I/O	NV_{DD}	—
PCI_AD18	AD14	I/O	NV_{DD}	—
PCI_AD19	AE14	I/O	NV_{DD}	—
PCI_AD20	AF12	I/O	NV_{DD}	—
PCI_AD21	AE11	I/O	NV_{DD}	—
PCI_AD22	AD12	I/O	NV_{DD}	—
PCI_AD23	AB13	I/O	NV_{DD}	—
PCI_AD24	AF9	I/O	NV_{DD}	—
PCI_AD25	AD11	I/O	NV_{DD}	—
PCI_AD26	AE10	I/O	NV_{DD}	—
PCI_AD27	AB12	I/O	NV_{DD}	—
PCI_AD28	AD10	I/O	NV_{DD}	—
PCI_AD29	AC10	I/O	NV_{DD}	—
PCI_AD30	AF10	I/O	NV_{DD}	—
PCI_AD31	AF8	I/O	NV_{DD}	—
PCI_C/$\overline{BE0}$	AC19	I/O	NV_{DD}	—
PCI_C/$\overline{BE1}$	AB15	I/O	NV_{DD}	—
PCI_C/$\overline{BE2}$	AF14	I/O	NV_{DD}	—
PCI_C/$\overline{BE3}$	AF11	I/O	NV_{DD}	—
PCI_PAR	AD16	I/O	NV_{DD}	—
$\overline{PCI\_FRAME}$	AF16	I/O	NV_{DD}	5

20.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in this table should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider. The VCO divider, which is determined by RCWLR[COREPLL], must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

Table 67. e300 Core PLL Configuration

RCWL[COREPLL]			***core_clk* : *csb_clk* Ratio**[1]	**VCO Divider (VCOD)**[3]
0–1	**2–5**	**6**		
nn	**0000**	0	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
11	***nnnn***	n	n/a	n/a
00	**0001**	0	1:1	2
01	**0001**	0	1:1	4
10	**0001**	0	1:1	8
00	**0001**	1	1.5:1	2
01	**0001**	1	1.5:1	4
10	**0001**	1	1.5:1	8
00	**0010**	0	2:1	2
01	**0010**	0	2:1	4
10	**0010**	0	2:1	8
00	**0010**	1	2.5:1	2
01	**0010**	1	2.5:1	4
10	**0010**	1	2.5:1	8
00	**0011**	0	3:1	2
01	**0011**	0	3:1	4
10	**0011**	0	3:1	8

Note:

1. For *core_clk:csb_clk* ratios of 2.5:1 and 3:1, the *core_clk* must not exceed its maximum operating frequency of 333 MHz.
2. Core VCO frequency = core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 400–800 MHz.

20.3 Example Clock Frequency Combinations

This table shows several possible frequency combinations that can be selected based on the indicated input reference frequencies, with RCWLR[LBCM] = 0 and RCWLR[DDRCM] =1, such that the LBC operates with a frequency equal to the frequency of *csb_clk* and the DDR controller operates at twice the frequency of *csb_clk*.

Table 68. System Clock Frequencies

						LBC(lbc_clk)				e300 Core(core_clk)				
SYS_ CLK_IN/ PCI_CLK	SPMF[1]	VCOD[2]	VCO[3]	CSB (*csb_clk*)[4]	DDR (ddr_clk)	/2	/4	/8	USB ref[5]	× 1	× 1.5	× 2	× 2.5	× 3
25.0	6	2	600.0	150.0	300.0	—	37.5	18.8	Note[6]	150.0	225	300	375	—
25.0	5	2	500.0	125.0	250.0	62.5	31.25	15.6	Note 6	125.0	188	250	313	375
33.3	5	2	666.0	166.5	333.0	—	41.63	20.8	Note 6	166.5	250	333	—	—
33.3	4	2	532.8	133.2	266.4	66.6	33.3	16.7	Note 6	133.2	200	266	333	400
48.0	3	2	576.0	144.0	288.0	—	36	18.0	48.0	144.0	216	288	360	—
66.7	2	2	533.4	133.3	266.7	66.7	33.34	16.7	Note 6	133.3	200	267	333	400

Note:

1. System PLL multiplication factor.
2. System PLL VCO divider.
3. When considering operating frequencies, the valid core VCO operating range of 400–800 MHz must not be violated.
4. Due to erratum eTSEC40, *csb_clk* frequencies of less than 133 MHz do not support gigabit Ethernet data rates. The core frequency must be 333 MHz for gigabit Ethernet operation. This erratum will be fixed in revision 2 silicon.
5. Frequency of USB PLL input reference.
6. USB reference clock must be supplied from a separate source as it must be 24 or 48 MHz, the USB reference must be supplied from a separate external source using USB_CLK_IN.

21 Thermal

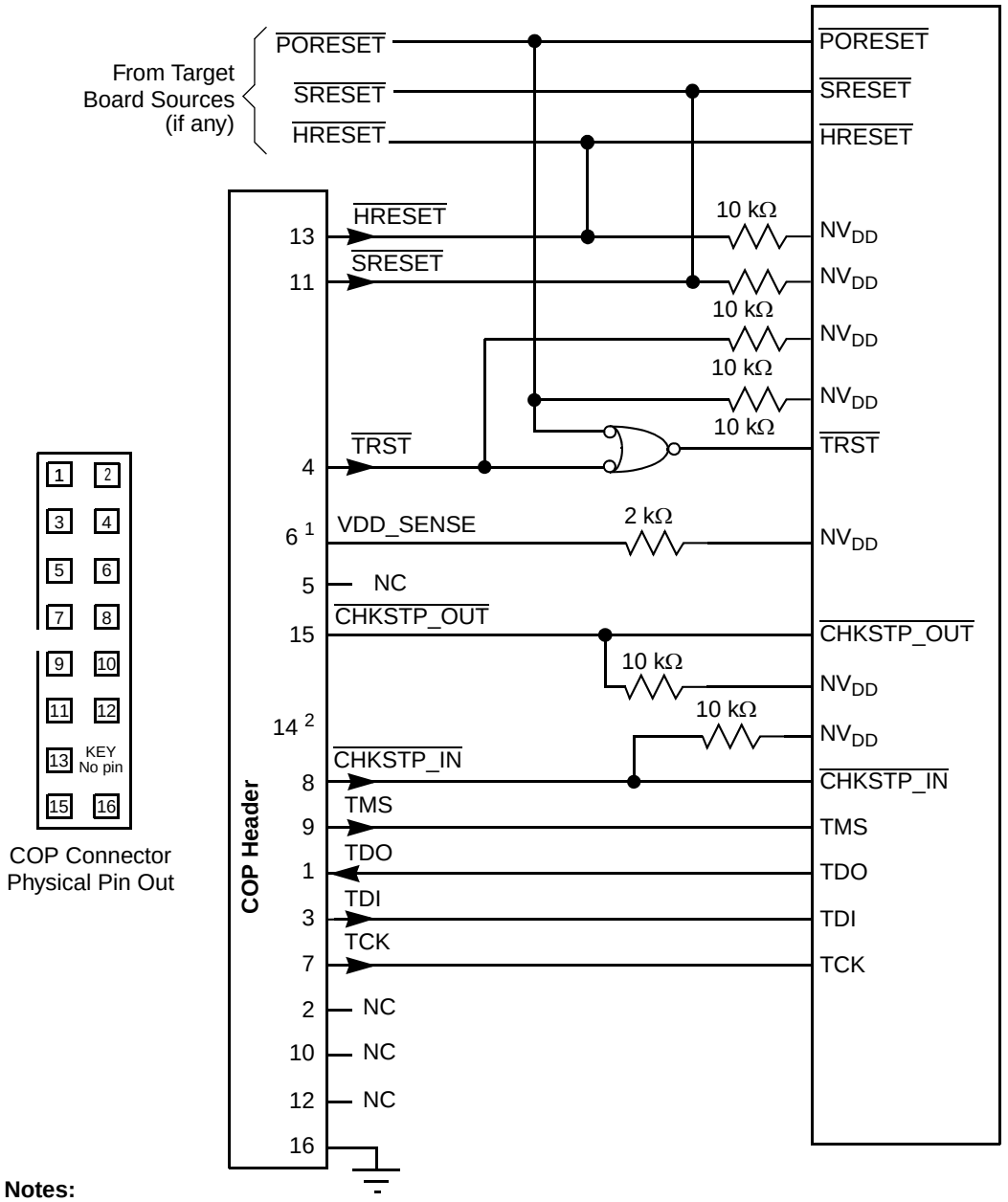
This section describes the thermal specifications of the MPC8313E.

21.1 Thermal Characteristics

This table provides the package thermal characteristics for the 516, 27 × 27 mm TEPBGAII.

Table 69. Package Thermal Characteristics for TEPBGAII

Characteristic	Board Type	Symbol	TEPBGA II	Unit	Note
Junction-to-ambient natural convection	Single layer board (1s)	$R_{\theta JA}$	25	°C/W	1, 2
Junction-to-ambient natural convection	Four layer board (2s2p)	$R_{\theta JA}$	18	°C/W	1, 2, 3
Junction-to-ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	20	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	15	°C/W	1, 3
Junction-to-board	—	$R_{\theta JB}$	10	°C/W	4



Notes:
1. Some systems require power to be fed from the application board into the debugger repeater card via the COP header. In this case the resistor value for VDD_SENSE should be around 20 Ω.
2. Key location; pin 14 is not physically present on the COP header.

Figure 61. JTAG Interface Connection

23 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 23.1, “Part Numbers Fully Addressed by this Document.”

Table 73. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
2	10/2008	• Added Note “The information in this document is accurate for revision 1.0, and 2.x and later. See Section 24.1, “Part Numbers Fully Addressed by this Document,” before Section 1, “Overview.” • Added part numbering details for all the silicon revisions in Table 74. • Changed V_{IH} from 2.7 V to 2.4 V in Table 7. • Added a row for V_{IH} level for Rev 2.x or later in Table 45. • Added a column for maximum power dissipation in low power mode for Rev 2.x or later silicon in Table 6. • Added a column for Power Nos for Rev 2.x or later silicon and added a row for 400 MHz in Table 4. • Removed footnote, “These are preliminary estimates.” from Table 4. • Added Table 21 for DDR AC Specs on Rev 2.x or later silicon. • Added Section 9, “High-Speed Serial Interfaces (HSSI).” • Added $\overline{\text{LFWE}}$, LFCLE, LFALE, $\overline{\text{LOE}}$, $\overline{\text{LFRE}}$, $\overline{\text{LFWP}}$, $\overline{\text{LGTA}}$, LUPWAIT, and $\overline{\text{LFRB}}$ in Table 63. • In Table 39, added note 2: “This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)” • Removed mentions of SGMII (SGMII has separate specs) from Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics.” • Corrected Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics,” to state that RGMII/RTBI interfaces only operate at 2.5 V, not 3.3 V. • Added ZQ package to ordering information In Table 74 and Section 19.1, “Package Parameters for the MPC8313E TEPBGAII” (applicable to both silicon rev. 1.0 and 2.1) • Removed footnotes 5 and 6 from Table 1 (left over when the PCI undershoot/overshoot voltages and maximum AC waveforms were removed from Section 2.1.2, “Power Supply Voltage Specification”). • Removed SD_PLL_TPD (T2) and SD_PLL_TPA_ANA (R4) from Table 63. • Added Section 8.3, “SGMII Interface Electrical Characteristics.” Removed Section 8.5.3 SGMII DC Electrical Characteristics. • Removed “HRESET negation to SRESET negation (output)” spec and changed “HRESET/SRESET assertion (output)” spec to “HRESET assertion (output)” in Table 10. • Clarified POR configuration signal specs to “Time for the device to turn off POR configuration signal drivers with respect to the assertion of HRESET” and “Time for the device to turn on POR configuration signal drivers with respect to the negation of HRESET” in Table 10. • Added Section 24.2, “Part Marking,” and Figure 62.

Table 73. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
1	3/2008	• Replaced OVDD with NV_{DD} everywhere • Added XCOREVDD and XPADVDD to Table 1 • Moved VDD and VDDC to the top of the table before SerDes supplies in Table 2 • In Table 2 split DDR row into two from total current requirement of 425 mA. One for DDR1 (131 mA) and other for DDR2 (140 mA). • In Table 2 corrected current requirement numbers for NV_{DD} from 27 mA to 74 mA, LV_{DD} from 60 mA to 16 mA, LV_{DDA} from 85 mA to 22 mA and LV_{DDB} from 85 mA to 44 mA. • In Table 2 corrected Vdd and Vddc current requirements from 560 mA and 454 mA to 469 and 377 mA, respectively. Corrected Avdd1 and Avdd2 current requirements from 10 mA to 2–3 mA, and XCOREVDD from 100 mA to 170 mA. • In Table 2, added row stating junction temperature range of 0 to 105°C. Added footnote 2 stating GPIO pins may operate from 2.5-V supply as well when configured for different functionality. • In Section 2.1.2, “Power Supply Voltage Specification,” added a note describing the purpose of Table 2. • In Section 3, “Power Characteristics,” added a note describing the purpose of Table 5. • Rewrote Section 2.2, “Power Sequencing,” and added Figure 3. • In Table 4, added “but do include core, USB PLL, and a portion of SerDes digital power...” to Note 1. • In Table 4 corrected “Typical power” to “Maximum power” in note 2 and added a note for Typical Power. • In Table 4 removed 266-MHz row as 266-MHz core parts are not offered. • In Table 5, moved Local bus typical power dissipation under LVdd. • Added Table 6 to show the low power mode power dissipation for D3warm mode. • In Table 8 corrected SYS_CLK_IN frequency range from 25–66 MHz to 24–66.67 MHz. • Added Section 8.4, “eTSEC IEEE 1588 AC Specifications” • In Table 42 changed minimum value of USB input hold t_{USIXKH} from 0 to 1ns • Added Table 43 and Table 44 showing USB clock in specifications • In Table 46, added rows for $t_{LALEHOV}$, $t_{LALETOT1}$, $t_{LALETOT2}$, and $t_{LALETOT3}$ parameters. Added Figure 40. • In Table 50, removed row for rise time (t_{I2CR}). Removed minimum value of t_{I2CF}. Added note 5 stating that the device does not follow the I2C-BUS Specifications version 2.1 regarding the t_{I2CF} AC parameter. • In Table 56, added a note stating: “This specification only applies to GPIO pins that are operating from a 3.3-V supply. See Table 63 for the power supply listed for the individual GPIO signal.” [• Added Table 57 to show DC characteristics for GPIO pins supplied by a 2.5-V supply. Same as eTSEC DC characteristics when operating at 2.5 V. • In Section 20, “Clocking,” corrected the sentence “When the device is configured as a PCI agent device, PCI_SYNC_IN is the primary input clock.” to state “When the device is configured as a PCI agent device, PCI_CLK is the primary input clock.” • Added “Value is decided by RCWLR[COREPLL]” to note 1 of Figure 57 • Added paragraph and Figure 59 to Section 22.2, “PLL Power Supply Filtering.” • Added Section 22.4, “SerDes Block Power Supply Decoupling Recommendations • Removed the two figures on PCI undershoot/overshoot voltages and maximum AC waveforms from Section 2.1.2, “Power Supply Voltage Specification,”