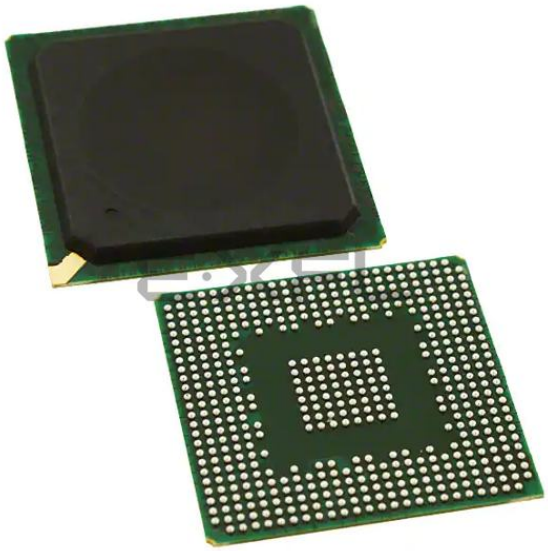

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8313ezqaffb

1.2 Serial Interfaces

The following interfaces are supported in the MPC8313E: dual UART, dual I^2C, and an SPI interface.

1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE Std 802.11i®, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are as follows:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-224, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

1.4 DDR Memory Controller

The MPC8313E DDR1/DDR2 memory controller includes the following features:

- Single 16- or 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 333 MHz
- Support for two physical banks (chip selects), each bank independently addressable
- 64-Mbit to 2-Gbit (for DDR1) and to 4-Gbit (for DDR2) devices with x8/x16/x32 data ports (no direct x4 support)
- Support for one 16-bit device or two 8-bit devices on a 16-bit bus, or one 32-bit device or two 16-bit devices on a 32-bit bus
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

1.5 PCI Controller

The MPC8313E PCI controller includes the following features:

- PCI specification revision 2.3 compatible
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

1.10 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the MPC8313E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

1.11 DMA Controller, Dual I^2C, DUART, Local Bus Controller, and Timers

The MPC8313E provides an integrated four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Supports misaligned transfers

There are two I^2C controllers. These synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. The 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8313E local bus controller (LBC) port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The three user programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM or UPM controller. The FCM provides a glueless interface to parallel-bus NAND Flash E2PROM devices. The FCM contains three basic configuration register groups—BR*n*, OR*n*, and FMR. Both may exist in the same system. The local bus can operate at up to 66 MHz.

The MPC8313E system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8313E. The MPC8313E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

Table 5. MPC8313E Typical I/O Power Dissipation (continued)

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	NV_{DD} (3.3 V)	LV_{DDA}/ LV_{DDB} (3.3 V)	LV_{DDA}/ LV_{DDB} (2.5 V)	LV_{DD} (3.3 V)	Unit	Comments
USBDR controller load = 20 pF	60 MHz	—	—	—	0.078	—	—	W	—
Other I/O	—	—	—	0.015	—	—	—	W	—

This table shows the estimated core power dissipation of the MPC8313E while transitioning into the D3 warm low-power state.

Table 6. MPC8313E Low-Power Modes Power Dissipation[1]

333-MHz Core, 167-MHz CSB[2]	Rev. 1.0[3]	Rev. 2.x or Later[3]	Unit
D3 warm	400	425	mW

Note:

1. All interfaces are enabled. For further power savings, disable the clocks to unused blocks.
2. The interfaces are run at the following frequencies: DDR: 333 MHz, eLBC 83 MHz, PCI 33 MHz, eTSEC1 and TSEC2: 167 MHz, SEC: 167 MHz, USB: 167 MHz. See the SCCR register for more information.
3. This is maximum power in D3 Warm based on a voltage of 1.05 V and a junction temperature of 105°C.

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8313E.

4.1 DC Electrical Characteristics

This table provides the system clock input (SYS_CLK_IN/PCI_SYNC_IN) DC timing specifications for the MPC8313E.

Table 7. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	NV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
SYS_CLK_IN input current	$0 V \le V_{IN} \le NV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0 V \le V_{IN} \le 0.5 V$ or $NV_{DD} – 0.5 V \le V_{IN} \le NV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0.5 V \le V_{IN} \le NV_{DD} – 0.5 V$	I_{IN}	—	±50	μA

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Note
Output leakage current	I_{OZ}	–9.9	–9.9	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Note:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 16. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM when GV_{DD}(typ) = 1.8 V.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	—

This table provides the input AC timing specifications for the DDR SDRAM when GV_{DD}(typ) = 2.5 V.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	—

This table provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions. with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ	t_{CISKEW}	—	—	ps	1, 2
333 MHz	—	–750	750	—	—
266 MHz	—	–750	750	—	—

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[*n*] and any corresponding bit that is captured with MDQS[*n*]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

This figure illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

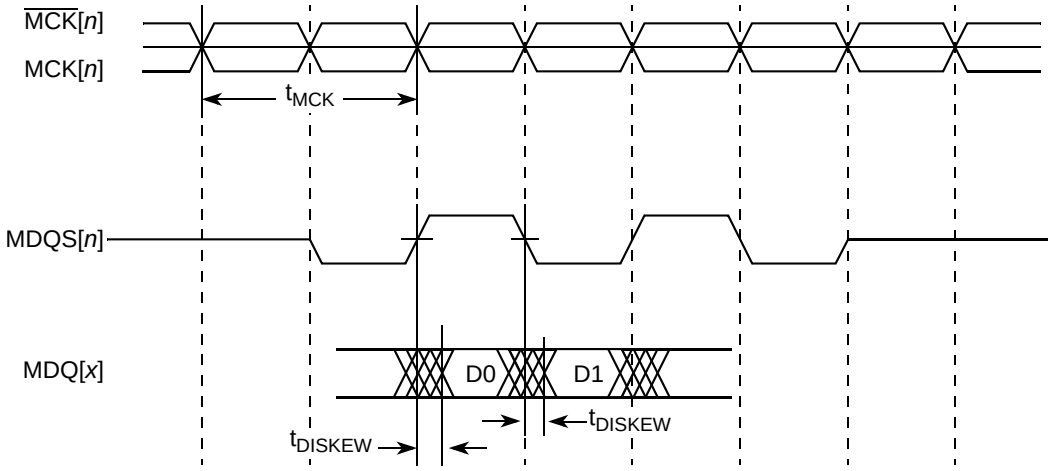


Figure 4. DDR Input Timing Diagram

This figure shows the MII transmit AC timing diagram.

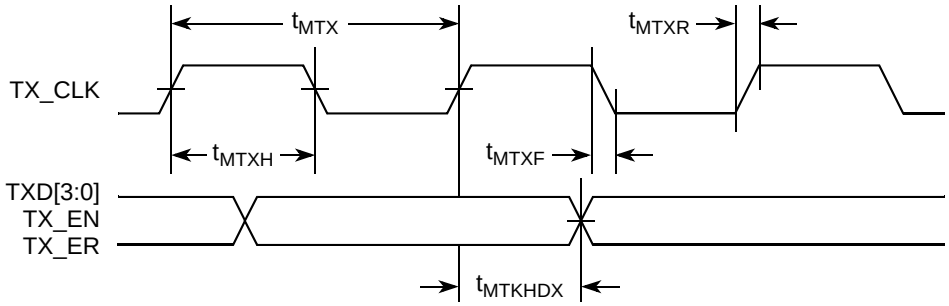


Figure 8. MII Transmit AC Timing Diagram

8.2.1.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 27. MII Receive AC Timing Specifications

At recommended operating conditions with $LV_{DDA}/LV_{DDB}/NV_{DD}$ of 3.3 V ± 0.3 V.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm

This figure provides the AC test load for TSEC.

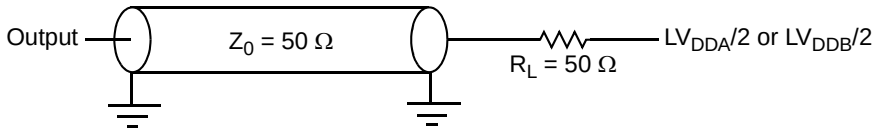


Figure 9. TSEC AC Test Load

Table 35. SGMII Receive AC Timing Specifications (continued)

At recommended operating conditions with $XCOREV_{DD}$ = 1.0 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Total jitter tolerance	JT	0.65	—	—	UI p-p	1
Bit error ratio	BER	—	—	10^{-12}		
Unit interval	UI	799.92	800	800.08	ps	2
AC coupling capacitor	C_{TX}	5	—	200	nF	3

Notes:
1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.

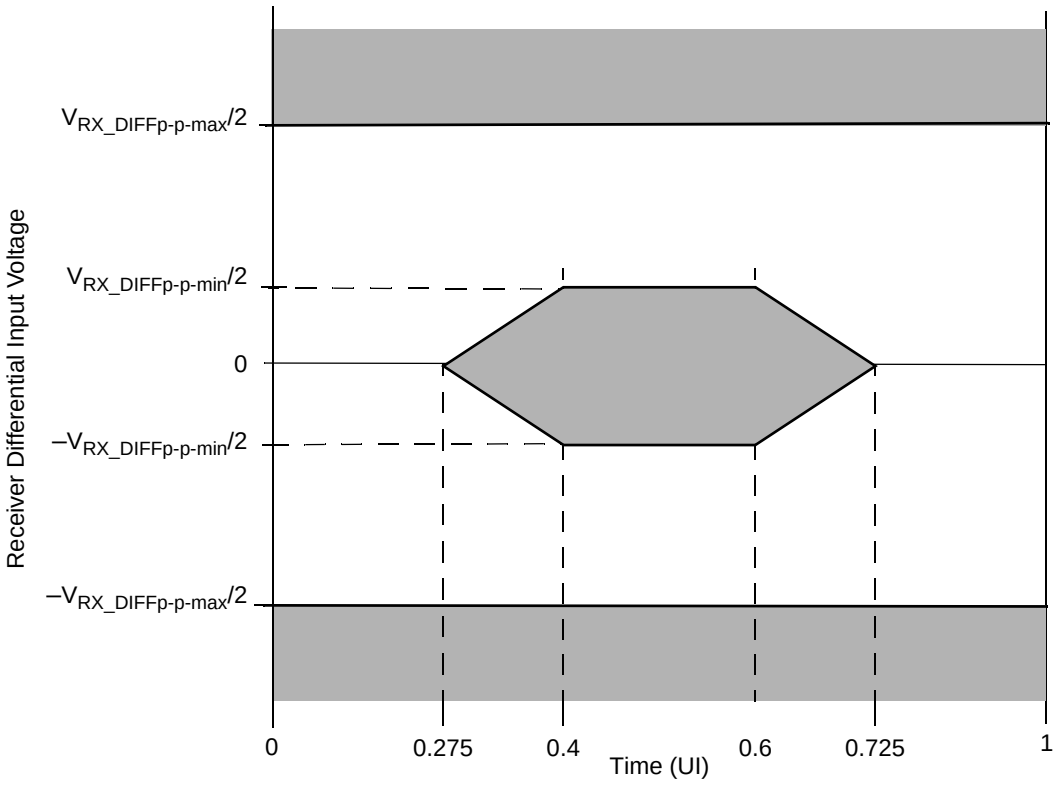


Figure 17. SGMII Receiver Input Compliance Mask

9.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low-phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters for SGMII protocol.

Table 39. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD_SRDS1} or XV_{DD_SRDS2} = 1.0 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
Rising edge rate	Rise edge rate	1.0	4.0	V/ns	2, 3
Falling edge rate	Fall edge rate	1.0	4.0	V/ns	2, 3
Differential input high voltage	V_{IH}	+200	—	mV	2
Differential input low voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn\_REF\_CLK}}$) matching	Rise-fall matching	—	20	%	1, 4

Notes:
1. Measurement taken from single-ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 31.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point, where SD*n*_REF_CLK rising meets $\overline{\text{SD}n\text{\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK should be compared to the fall edge rate of $\overline{\text{SD}n\text{\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 32.

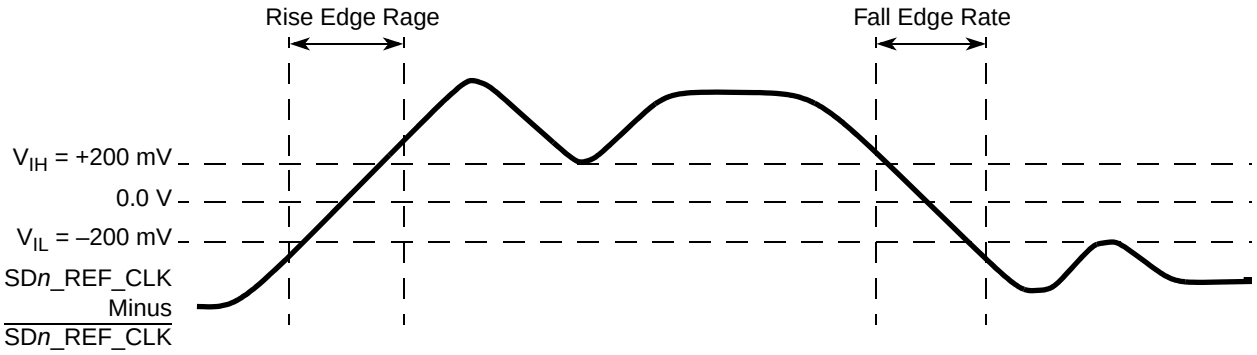


Figure 31. Differential Measurement Points for Rise and Fall Time

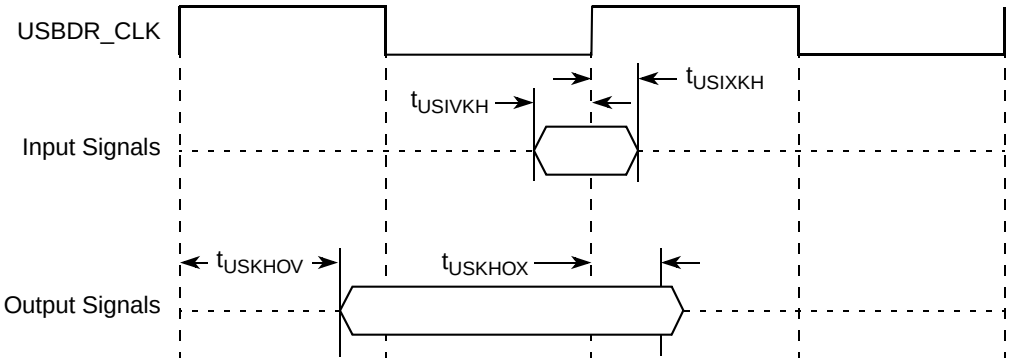


Figure 35. USB Signals

10.2 On-Chip USB PHY

This section describes the DC and AC electrical specifications for the on-chip USB PHY of the MPC8313E. See Chapter 7 in the *USB Specifications Rev. 2*, for more information.

This table provides the USB clock input (USB_CLK_IN) DC timing specifications.

Table 42. USB_CLK_IN DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2.7	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	–0.3	0.4	V

This table provides the USB clock input (USB_CLK_IN) AC timing specifications.

Table 43. USB_CLK_IN AC Timing Specifications

Parameter/Condition	Conditions	Symbol	Min	Typ	Max	Unit
Frequency range	—	$f_{USB\_CLK\_IN}$	—	24	48	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	–0.005	0	0.005	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/time interval error	Peak-to-peak value measured with a second order high-pass filter of 500 kHz bandwidth	t_{CLK_PJ}	—	—	200	ps

Table 47. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Note
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 34). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

This figure provides the AC test load for TDO and the boundary-scan outputs.

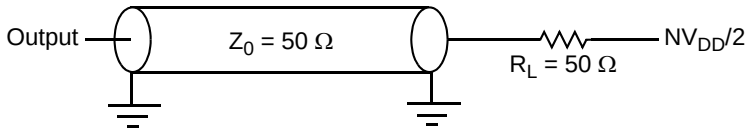


Figure 41. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

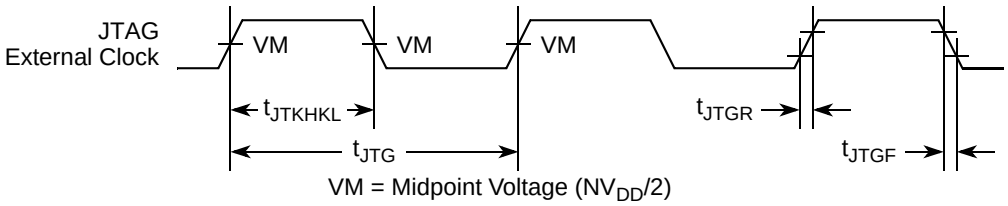


Figure 42. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

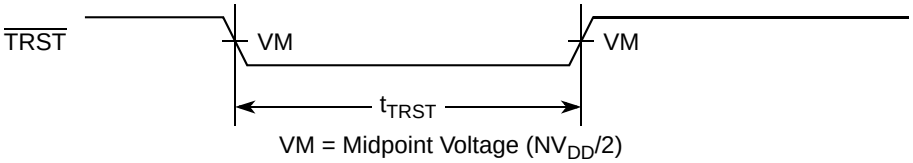


Figure 43. $\overline{\text{TRST}}$ Timing Diagram

This figure provides the boundary-scan timing diagram.

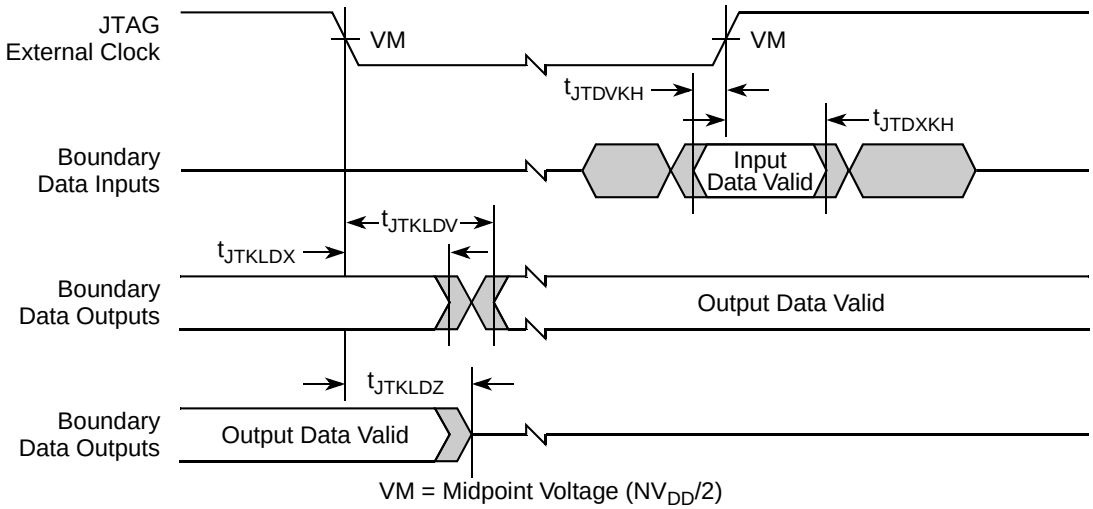


Figure 44. Boundary-Scan Timing Diagram

This figure provides the test access port timing diagram.

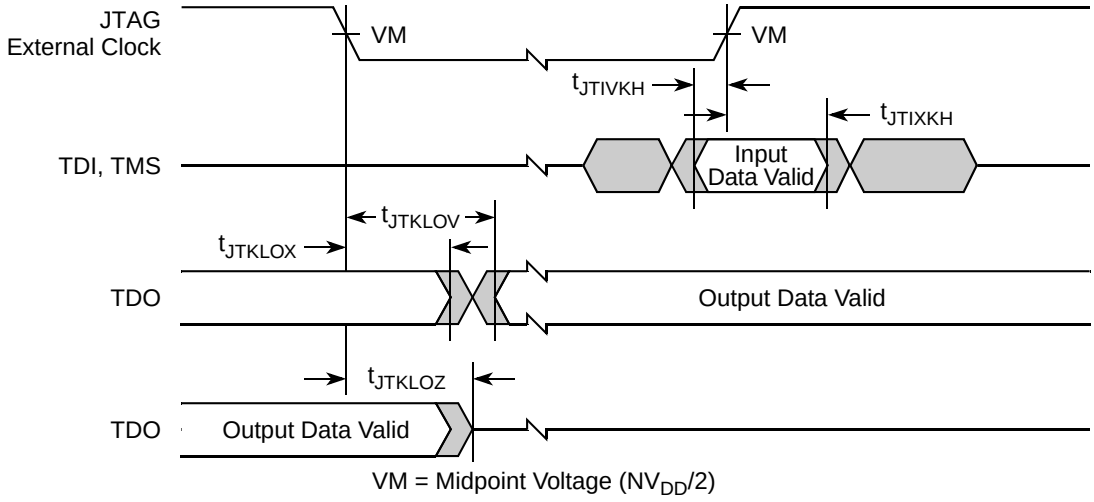


Figure 45. Test Access Port Timing Diagram

Table 49. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 48).

Parameter	Symbol[1]	Min	Max	Unit
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0[2]	 — 0.9[3]	µs
Fall time of both SDA and SCL signals[5]	t_{I2CF}	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times NV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times NV_{DD}$	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The MPC8313E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5. The MPC8313E does not follow the *I²C-BUS Specifications, Version 2.1,* regarding the t_{I2CF} AC parameter.

This figure provides the AC test load for the I²C.

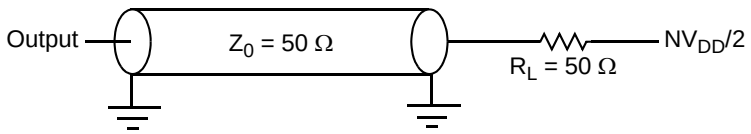


Figure 46. I²C AC Test Load

17 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

17.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins.

Table 58. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

17.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 59. IPIC Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Note:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

18 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8313E.

18.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the MPC8313E SPI.

Table 60. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MEMC_MDQ29	A20	I/O	GV_{DD}	—
MEMC_MDQ30	C22	I/O	GV_{DD}	—
MEMC_MDQ31	B22	I/O	GV_{DD}	—
MEMC_MDM0	B7	O	GV_{DD}	—
MEMC_MDM1	E6	O	GV_{DD}	—
MEMC_MDM2	E18	O	GV_{DD}	—
MEMC_MDM3	E20	O	GV_{DD}	—
MEMC_MDQS0	A7	I/O	GV_{DD}	—
MEMC_MDQS1	E7	I/O	GV_{DD}	—
MEMC_MDQS2	B19	I/O	GV_{DD}	—
MEMC_MDQS3	A23	I/O	GV_{DD}	—
MEMC_MBA0	D15	O	GV_{DD}	—
MEMC_MBA1	A18	O	GV_{DD}	—
MEMC_MBA2	A15	O	GV_{DD}	—
MEMC_MA0	E12	O	GV_{DD}	—
MEMC_MA1	D11	O	GV_{DD}	—
MEMC_MA2	B11	O	GV_{DD}	—
MEMC_MA3	A11	O	GV_{DD}	—
MEMC_MA4	A12	O	GV_{DD}	—
MEMC_MA5	E13	O	GV_{DD}	—
MEMC_MA6	C12	O	GV_{DD}	—
MEMC_MA7	E14	O	GV_{DD}	—
MEMC_MA8	B15	O	GV_{DD}	—
MEMC_MA9	C17	O	GV_{DD}	—
MEMC_MA10	C13	O	GV_{DD}	—
MEMC_MA11	A16	O	GV_{DD}	—
MEMC_MA12	C15	O	GV_{DD}	—
MEMC_MA13	C16	O	GV_{DD}	—
MEMC_MA14	E15	O	GV_{DD}	—
$\overline{\text{MEMC\_MWE}}$	B18	O	GV_{DD}	—
$\overline{\text{MEMC\_MRAS}}$	C11	O	GV_{DD}	—
$\overline{\text{MEMC\_MCAS}}$	B10	O	GV_{DD}	—

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LA14/TSEC_1588_TRIG1	L24	O	LV_{DD}	8
LA15/TSEC_1588_ALARM2	K26	O	LV_{DD}	8
DUART				
UART_SOUT1/MSRCID0	N2	O	NV_{DD}	—
UART_SIN1/MSRCID1	M5	I/O	NV_{DD}	—
$\overline{\text{UART\_CTS1}}$/GPIO8/MSRCID2	M1	I/O	NV_{DD}	—
$\overline{\text{UART\_RTS1}}$/GPIO9/MSRCID3	K1	I/O	NV_{DD}	—
UART_SOUT2/MSRCID4/TSEC_1588_CLK	M3	O	NV_{DD}	8
UART_SIN2/MDVAL/TSEC_1588_GCLK	L1	I/O	NV_{DD}	8
$\overline{\text{UART\_CTS2}}$/TSEC_1588_PP1	L5	I/O	NV_{DD}	8
$\overline{\text{UART\_RTS2}}$/TSEC_1588_PP2	L3	I/O	NV_{DD}	8
I^2C interface				
IIC1_SDA/$\overline{\text{CKSTOP\_OUT}}$/TSEC_1588_TRIG1	J4	I/O	NV_{DD}	2, 8
IIC1_SCL/$\overline{\text{CKSTOP\_IN}}$/TSEC_1588_ALARM2	J2	I/O	NV_{DD}	2, 8
IIC2_SDA/PMC_PWR_OK/GPIO10	J3	I/O	NV_{DD}	2
IIC2_SCL/GPIO11	H5	I/O	NV_{DD}	2
Interrupts				
$\overline{\text{MCP\_OUT}}$	G5	O	NV_{DD}	2
$\overline{\text{IRQ0}}$/$\overline{\text{MCP\_IN}}$	K5	I	NV_{DD}	—
$\overline{\text{IRQ1}}$	K4	I	NV_{DD}	—
$\overline{\text{IRQ2}}$	K2	I	NV_{DD}	—
$\overline{\text{IRQ3}}$/$\overline{\text{CKSTOP\_OUT}}$	K3	I/O	NV_{DD}	—
$\overline{\text{IRQ4}}$/$\overline{\text{CKSTOP\_IN}}$/GPIO12	J1	I/O	NV_{DD}	—
Configuration				
$\overline{\text{CFG\_CLKIN\_DIV}}$	D5	I	NV_{DD}	—
EXT_PWR_CTRL	J5	O	NV_{DD}	—
CFG_LBIU_MUX_EN	R24	I	NV_{DD}	—
JTAG				
TCK	E1	I	NV_{DD}	—
TDI	E2	I	NV_{DD}	4
TDO	E3	O	NV_{DD}	3

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal NV_{DD}, 105°C.

Table 71. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (Not Including PCI Output Clocks)	PCI Output Clocks (Including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
R_P	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
Differential	NA	NA	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_J = 105 °C.

22.7 Configuration Pin Muxing

The MPC8313E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{PORESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

22.8 Pull-Up Resistor Requirements

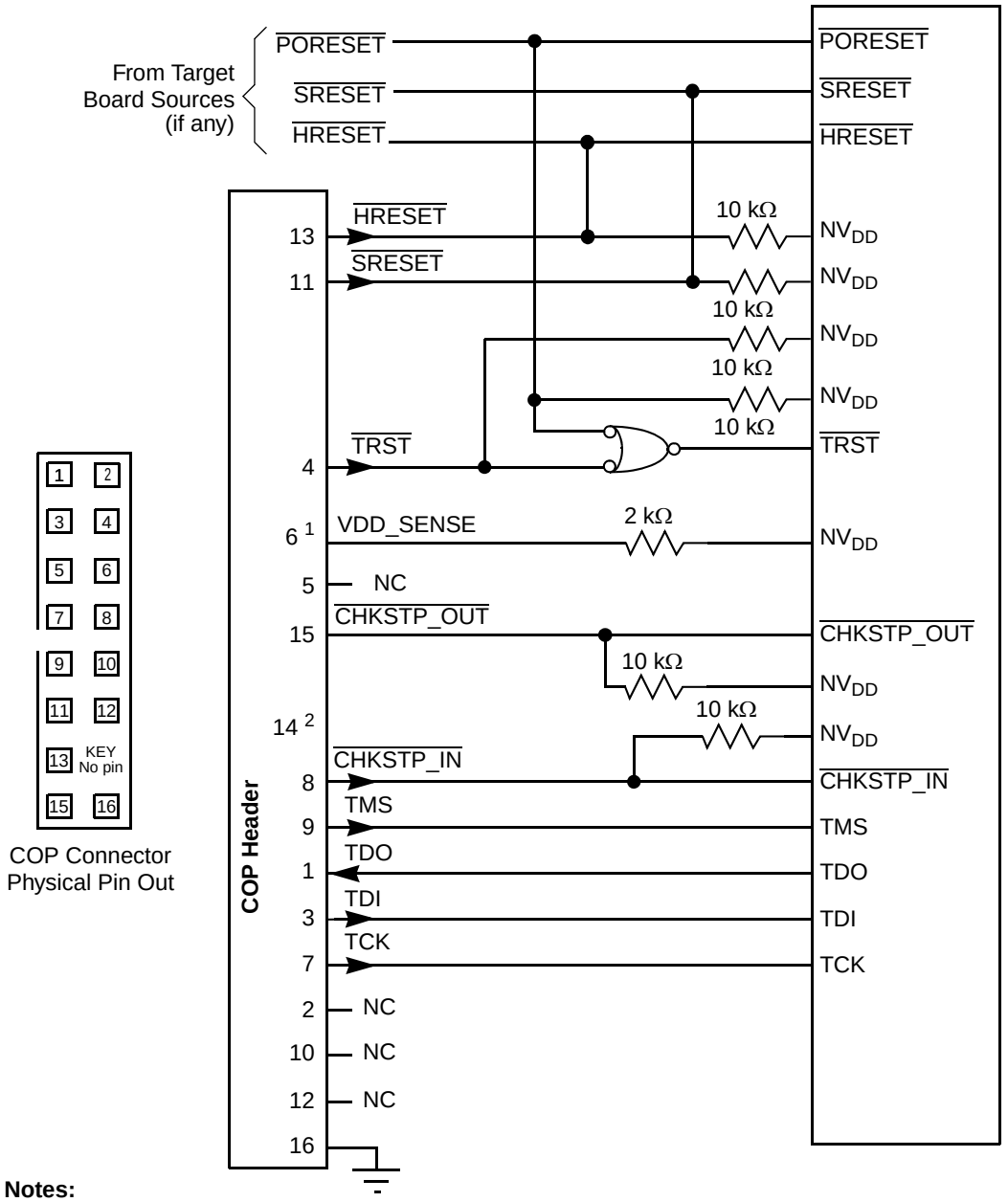
The MPC8313E requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C, and IPIC (integrated programmable interrupt controller).

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 61. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions because most have asynchronous behavior and spurious assertion, which give unpredictable results.

Refer to the *PCI 2.2 Specification*, for all pull-ups required for PCI.

22.9 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in IEEE 1149.1, but is provided on any Freescale devices that are built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, systems generally assert $\overline{\text{TRST}}$ during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ is not practical.



Notes:
1. Some systems require power to be fed from the application board into the debugger repeater card via the COP header. In this case the resistor value for VDD_SENSE should be around 20 Ω.
2. Key location; pin 14 is not physically present on the COP header.

Figure 61. JTAG Interface Connection

23 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 23.1, “Part Numbers Fully Addressed by this Document.”

24 Revision History

This table summarizes a revision history for this document.

Table 73. Document Revision History

Rev. Number	Date	Substantive Change(s)
4	11/2011	• In Table 2, added following notes: – Note 3: Min temperature is specified with T_A; Max temperature is specified with T_J – Note 4: All Power rails must be connected and power applied to the MPC8313 even if the IP interfaces are not used. – Note 5: All I/O pins should be interfaced with peripherals operating at same voltage level. – Note 6: This voltage is the input to the filter discussed in Section 22.2, “PLL Power Supply Filtering.” and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter • Decoupled PCI_CLK and SYS_CLK_IN rise and fall times in Table 8. Relaxed maximum rise/fall time of SYS_CLK_IN to 4ns. • Added a note in Table 27 stating “The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm." • In Table 30: – Changed max value of t_{skrgt} in “Data to clock input skew (at receiver)” row from 2.8 to 2.6. – Added Note 7, stating that, “The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm.” • Added a note stating “eTSEC should be interfaced with peripheral operating at same voltage level” in Section 8.1.1, “TSEC DC Electrical Characteristics.” • TSEC1_MDC and TSEC_MDIO are powered at 3.3V by NVDD. Replaced LVDDA/LVDDB with NVDD and removed instances of 2.5V at several places in Section 8.5, “Ethernet Management Interface Electrical Characteristics.” • In Table 43, changed min/max values of t_{CLK_TOL} from 0.05 to 0.005. • In Table 62: – Added Note 2 for LGPL4 in showing LGPL4 as open-drain. – Removed Note 2 from TSEC1_MDIO. – Added Note 10: This pin has an internal pull-up. – Added Note 11: This pin has an internal pull-down. – Added Note 12: “In MII mode, GTX_CLK should be pulled down by 300 Ω to V_{SS}” to TSEC1_GTX_CLK and TSEC2_GTX_CLK. • In Section 19.1, “Package Parameters for the MPC8313E TEPBGAII,” replaced "5.5 Sn/0.5 Cu/4 Ag" with "Sn/3.5 Ag." • Added foot note 3 in Table 65 stating “The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.” • In Table 72: – Added AD = 266 and D = 266. – Added “C = 2.2” in “Revision level” column. – Added Note 4. • Changed resitor from 1.0 Ω to 10 Ω in Figure 58. • Replaced LCCR with LCRR throughout. • Added high-speed to USB Phy description.
3	01/2009	• Table 72, in column aa, changed to AG = 400 MHz.
2.2	12/2008	• Made cross-references active for sections, figures, and tables.
2.1	12/2008	• Added Figure 2, after Table 2 and renumbered the following figures.

Table 73. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
2	10/2008	• Added Note “The information in this document is accurate for revision 1.0, and 2.x and later. See Section 24.1, “Part Numbers Fully Addressed by this Document,” before Section 1, “Overview.” • Added part numbering details for all the silicon revisions in Table 74. • Changed V_{IH} from 2.7 V to 2.4 V in Table 7. • Added a row for V_{IH} level for Rev 2.x or later in Table 45. • Added a column for maximum power dissipation in low power mode for Rev 2.x or later silicon in Table 6. • Added a column for Power Nos for Rev 2.x or later silicon and added a row for 400 MHz in Table 4. • Removed footnote, “These are preliminary estimates.” from Table 4. • Added Table 21 for DDR AC Specs on Rev 2.x or later silicon. • Added Section 9, “High-Speed Serial Interfaces (HSSI).” • Added $\overline{\text{LFWE}}$, LFCLE, LFALE, $\overline{\text{LOE}}$, $\overline{\text{LFRE}}$, $\overline{\text{LFWP}}$, $\overline{\text{LGTA}}$, LUPWAIT, and $\overline{\text{LFRB}}$ in Table 63. • In Table 39, added note 2: “This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)” • Removed mentions of SGMII (SGMII has separate specs) from Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics.” • Corrected Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics,” to state that RGMII/RTBI interfaces only operate at 2.5 V, not 3.3 V. • Added ZQ package to ordering information In Table 74 and Section 19.1, “Package Parameters for the MPC8313E TEPBGAII” (applicable to both silicon rev. 1.0 and 2.1) • Removed footnotes 5 and 6 from Table 1 (left over when the PCI undershoot/overshoot voltages and maximum AC waveforms were removed from Section 2.1.2, “Power Supply Voltage Specification”). • Removed SD_PLL_TPD (T2) and SD_PLL_TPA_ANA (R4) from Table 63. • Added Section 8.3, “SGMII Interface Electrical Characteristics.” Removed Section 8.5.3 SGMII DC Electrical Characteristics. • Removed “HRESET negation to SRESET negation (output)” spec and changed “HRESET/SRESET assertion (output)” spec to “HRESET assertion (output)” in Table 10. • Clarified POR configuration signal specs to “Time for the device to turn off POR configuration signal drivers with respect to the assertion of HRESET” and “Time for the device to turn on POR configuration signal drivers with respect to the negation of HRESET” in Table 10. • Added Section 24.2, “Part Marking,” and Figure 62.

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