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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8313vragdb

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2.1 **Overall DC Electrical Characteristics**

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table	1. Absolute	Maximum	Ratings ¹
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	Characteristic	Symbol	Max Value	Unit	Note
Core supply volta	age	V _{DD}	-0.3 to 1.26	V	
PLL supply voltage		AV _{DD} -0.3 to 1.26		V	—
Core power supp	ly for SerDes transceivers	XCOREV _{DD}	-0.3 to 1.26	V	—
Pad power supply	y for SerDes transceivers	XPADV _{DD}	-0.3 to 1.26	V	—
DDR and DDR2 DRAM I/O voltage		GV _{DD}	-0.3 to 2.75 -0.3 to 1.98	V	_
PCI, local bus, DUART, system control and power management, I^2C , and JTAG I/O voltage		NV _{DD} /LV _{DD}	-0.3 to 3.6	V	—
eTSEC, USB		LV _{DDA} /LV _{DDB}	-0.3 to 3.6	V	
Input voltage	DDR DRAM signals	MV _{IN}	–0.3 to (GV _{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV _{REF}	–0.3 to (GV _{DD} + 0.3)	V	2, 5
	Enhanced three-speed Ethernet signals	LV _{IN}	-0.3 to (LV _{DDA} + 0.3) or -0.3 to (LV _{DDB} + 0.3)	V	4, 5
	Local bus, DUART, SYS_CLK_IN, system control, and power management, I ² C, and JTAG signals	NV _{IN}	–0.3 to (NV _{DD} + 0.3)	V	3, 5
PCI		NV _{IN}	–0.3 to (NV _{DD} + 0.3)	V	6
Storage temperature range		T _{STG}	–55 to 150	°C	

Notes:

- 1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 3. **Caution:** NV_{IN} must not exceed NV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution: LV_{IN} must not exceed LV_{DDA}/LV_{DDB} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the MPC8313E. Note that the values in this table are the recommended and tested operating conditions. If a particular block is given a voltage falling within the range in the Recommended Value column, the MPC8313E is capable of delivering the amount of current listed in the Current Requirement column; this is the maximum current possible. Proper device operation outside of these conditions is not guaranteed.



Table 2. Recommended Operating Conditions (continued)

|--|

Note:

- 1. GV_{DD}, NV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
- 2. Some GPIO pins may operate from a 2.5-V supply when configured for other functions.
- 3. Min temperature is specified with T_A ; Max temperature is specified with T_J
- 4. All Power rails must be connected and power applied to the MPC8313 even if the IP interfaces are not used.
- 5. All I/O pins should be interfaced with peripherals operating at same voltage level.
- This voltage is the input to the filter discussed in Section 22.2, "PLL Power Supply Filtering" and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter.

This figure shows the undershoot and overshoot voltages at the interfaces of the MPC8313E.



Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/NV_{DD}/LV_{DD}

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	NV _{DD} = 3.3 V
PCI signals	25	
DDR signal	18	GV _{DD} = 2.5 V



Driver Type	Output Impedance (Ω)	Supply Voltage
DDR2 signal	18	GV _{DD} = 1.8 V
DUART, system control, I ² C, JTAG, SPI	42	NV _{DD} = 3.3 V
GPIO signals	42	NV _{DD} = 3.3 V
eTSEC signals	42	LV_{DDA} , LV_{DDB} = 2.5/3.3 V
USB signals	42	LV _{DDB} = 2.5/3.3 V

Table 3. Output Drive Capability (continued)

2.2 Power Sequencing

The MPC8313E does not require the core supply voltage (V_{DD} and V_{DDC}) and I/O supply voltages (GV_{DD} , LV_{DD} , and NV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD} and V_{DDC}) before the I/O voltage (GV_{DD} , LV_{DD} , and NV_{DD}) and assert PORESET before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating PORESET.

Note that there is no specific power down sequence requirement for the MPC8313E. I/O voltage supplies $(GV_{DD}, LV_{DD}, and NV_{DD})$ do not have any ordering requirements with respect to one another.



Figure 3. Power-Up Sequencing Example





This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

8.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-coupled serial link from the dedicated SerDes interface of MPC8313E as shown in Figure 15, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features a 50- Ω output impedance. Each input of the SerDes receiver differential pair features 50- Ω on-die termination to XCOREVSS. The reference circuit of the SerDes transmitter and receiver is shown in Figure 33.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in Section 22.5, "Connection Recommendations," as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the TSEC_GTX_CLK125 clock is not required for this port. Instead, the SerDes reference clock is required on SD_REF_CLK and SD_REF_CLK pins.

8.3.1 DC Requirements for SGMII SD_REF_CLK and SD_REF_CLK

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 9, "High-Speed Serial Interfaces (HSSI)."



 Table 33. SGMII DC Receiver Electrical Characteristics (continued)

Parameter	Symbol	Min	Тур	Мах	Unit	Note
Common mode input voltage	V _{CM}	_	V _{xcorevss}	—	V	4

Notes:

1. Input must be externally AC-coupled.

2. $V_{RX_DIFFp-p}$ is also referred to as peak to peak input differential voltage

3. V_{CM_ACp-p} is also referred to as peak to peak AC common mode voltage.

4. On-chip termination to XCOREV_{SS}.

8.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs $(TX[n] \text{ and } \overline{TX}[n])$ or at the receiver inputs $(RX[n] \text{ and } \overline{RX}[n])$ as depicted in Figure 18, respectively.

8.3.4.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 34. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XCOREV_{DD} = 1.0 V \pm 5%.

Parameter	Symbol	Min	Тур	Мах	Unit	Note
Deterministic jitter	JD	—	—	0.17	UI p-p	
Total jitter	JT	—	—	0.35	UI p-p	
Unit interval	UI	799.92	800	800.08	ps	1
V _{OD} fall time (80%–20%)	tfall	50	—	120	ps	
V _{OD} rise time (20%–80%)	t _{rise}	50	—	120	ps	

Note:

1. Each UI is 800 ps \pm 100 ppm.

8.3.4.2 SGMII Receive AC Timing Specifications

This table provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 17 shows the SGMII receiver input compliance mask eye diagram.

Table 35. SGMII Receive AC Timing Specifications

At recommended operating conditions with XCOREV_{DD} = 1.0 V \pm 5%.

Parameter	Symbol	Min	Тур	Max	Unit	Note
Deterministic jitter tolerance	JD	0.37	—	_	UI p-p	1
Combined deterministic and random jitter tolerance	JDR	0.55	_	_	UI p-p	1
Sinusoidal jitter tolerance	JSIN	0.1	—		UI p-p	1



Table 36. eTSEC IEEE 1588 AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5%.

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Note
TSEC_1588_CLK peak-to-peak jitter	t _{T1588} CLKINJ	—	_	250	ps	
Rise time eTSEC_1588_CLK (20%-80%)	t _{T1588} CLKINR	1.0	_	2.0	ns	
Fall time eTSEC_1588_CLK (80%–20%)	t _{T1588} CLKINF	1.0	_	2.0	ns	
TSEC_1588_CLK_OUT clock period	t _{T1588} CLKOUT	$2 \times t_{T1588CLK}$	_	_	ns	
TSEC_1588_CLK_OUT duty cycle	^t t1588CLKOTH /t _{T1588} CLKOUT	30	50	70	%	
TSEC_1588_PULSE_OUT	t _{T1588OV}	0.5	_	3.0	ns	
TSEC_1588_TRIG_IN pulse width	t _{T1588} TRIGH	$2 \times t_{T1588CLK_MAX}$	_	—	ns	2

Notes:

1. T_{RX_CLK} is the max clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for a description of TMR_CTRL registers.

2. It need to be at least two times of clock period of clock selected by TMR_CTRL[CKSEL]. See the MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual, for a description of TMR_CTRL registers.

The maximum value of t_{T1588CLK} is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of t_{T1588CLK} is 3600, 280, and 56 ns, respectively.

8.5 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, RMII, RGMII, SGMII, and RTBI are specified in Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics."

8.5.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. Table 37 provide the DC electrical characteristics for MDIO and MDC.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (3.3 V)	NV _{DD}		_		3.63	V
Output high voltage	V _{OH}	I _{OH} = -1.0 mA	NV _{DD} = Min	2.10	NV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$NV_{DD} = Min$	V _{SS}	0.50	V
Input high voltage	V _{IH}	_		2.0	_	V
Input low voltage	V _{IL}		-		0.80	V
Input high current	I _{IH}	NV _{DD} = Max	$V_{IN}^{1} = 2.1 V$	—	40	μΑ
Input low current	Ι _{IL}	NV _{DD} = Max	V _{IN} = 0.5 V	-600	—	μΑ

 Table 37. MII Management DC Electrical Characteristics When Powered at 3.3 V



This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8313E SerDes reference clock input's DC requirement.



Figure 27. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8313E SerDes reference clock input's allowed range (100 to 400 mV), the AC-coupled connection scheme must be used. It assumes the LVDS output driver features a 50- Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.



Figure 28. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the MPC8313E SerDes reference clock input's DC requirement, AC coupling has to be used. Figure 29



assumes that the LVPECL clock driver's output impedance is 50 Ω . R1 is used to DC-bias the LVPECL outputs prior to AC coupling. Its value could be ranged from 140 to 240 Ω depending on the clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50- Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8313E SerDes3 reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω . Consult with the clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.



Figure 29. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the MPC8313E SerDes reference clock input's DC requirement.



Figure 30. Single-Ended Connection (Reference Only)



11 Enhanced Local Bus

This section describes the DC and AC electrical specifications for the local bus interface.

11.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface.

Table 44. Local Bus DC Electrical Chara	cteristics at 3.3 V
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Parameter	Symbol	Min	Мах	Unit
High-level input voltage for Rev 1.0	V _{IH}	2.0	LV _{DD} + 0.3	V
High-level input voltage for Rev 2.x or later	V _{IH}	2.1	LV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current, $(V_{IN}^{1} = 0 V \text{ or } V_{IN} = LV_{DD})$	I _{IN}	—	±5	μA
High-level output voltage, (LV _{DD} = min, $I_{OH} = -2$ mA)	V _{OH}	LV _{DD} - 0.2	—	V
Low-level output voltage, (LV _{DD} = min, I _{OH} = 2 mA)	V _{OL}	—	0.2	V

Note: The parameters stated in above table are valid for all revisions unless explicitly mentioned.

11.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface.

Table 45. Local Bus General Timing Parameters

Parameter	Symbol ¹	Min	Мах	Unit	Note
Local bus cycle time	t _{LBK}	15	_	ns	2
Input setup to local bus clock	t _{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t _{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT1}	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT2}	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT3}	2.5	—	ns	7
LALE output rise to LCLK negative edge	t _{LALEHOV}	—	3.0	ns	
LALE output fall to LCLK negative edge	t _{LALETOT1}	-1.5	—	ns	5
LALE output fall to LCLK negative edge	t _{LALETOT2}	-5.0	—	ns	6
LALE output fall to LCLK negative edge	t _{LALETOT3}	-4.5	—	ns	7
Local bus clock to output valid	t _{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD	t _{LBKHOZ}	—	4	ns	8



Table 45. Local Bus General Timing Parameters (continued)

	Parameter	Symbol ¹	Min	Max	Unit	Note
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Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1).
 </sub>
- 2. All timings are in reference to falling edge of LCLK0 (for all outputs and for LGTA and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
- 3. All signals are measured from NV_{DD}/2 of the rising/falling edge of LCLK0 to $0.4 \times NV_{DD}$ of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. t_{LBOTOT1} and t_{LALETOT1} should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- 6. t_{LBOTOT2} and t_{LALETOT2} should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- 7. t_{LBOTOT3} and t_{LALETOT3} should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.
- 8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This figure provides the AC test load for the local bus.



Figure 36. Local Bus AC Test Load



13 I²C

This section describes the DC and AC electrical characteristics for the I²C interface.

13.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interface.

Table 48. I²C DC Electrical Characteristics

At recommended operating conditions with NV_{DD} of 3.3 V \pm 0.3 V.

Parameter	Symbol	Min	Мах	Unit	Note
Input high voltage level	V _{IH}	$0.7 imes NV_{DD}$	NV _{DD} + 0.3	V	
Input low voltage level	V _{IL}	-0.3	$0.3\times \text{NV}_{\text{DD}}$	V	
Low level output voltage	V _{OL}	0	$0.2\times \text{NV}_{\text{DD}}$	V	1
Output fall time from $V_{IH}(min)$ to $V_{IL}(max)$ with a bus capacitance from 10 to 400 pF	^t I2KLKV	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t _{i2KHKL}	0	50	ns	3
Capacitance for each I/O pin	CI	—	10	pF	
Input current, (0 V \leq V _{IN} \leq NV _{DD})	I _{IN}		± 5	μA	4

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

- 2. C_B = capacitance of one bus line in pF.
- 3. Refer to the MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual, for information on the digital filter used.
- 4. I/O pins obstruct the SDA and SCL lines if $\mathsf{NV}_{\mathsf{DD}}$ is switched off.

13.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I^2C interface.

Table 49. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 48).

Parameter	Symbol ¹	Min	Мах	Unit
SCL clock frequency	f _{I2C}	0	400	kHz
Low period of the SCL clock	t _{I2CL}	1.3	—	μS
High period of the SCL clock	t _{I2CH}	0.6	—	μS
Setup time for a repeated START condition	t _{I2SVKH}	0.6	—	μS
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	—	μs
Data setup time	t _{I2DVKH}	100	_	ns



Parameter	Symbol ¹	Min	Мах	Unit	Note
Clock to output high impedance	t _{PCKHOZ}	_	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t _{PCIXKH}	0	—	ns	2, 4

Table 51. PCI AC Timing Specifications at 66 MHz (continued)

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
</sub>

2. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.

- 3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.

This table shows the PCI AC timing specifications at 33 MHz.

Table 52. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Мах	Unit	Note
Clock to output valid	^t PCKHOV	—	11	ns	2
Output hold from clock	t _{PCKHOX}	2	—	ns	2
Clock to output high impedance	t _{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	^t PCIVKH	3.0	—	ns	2, 4
Input hold from clock	t _{PCIXKH}	0	—	ns	2, 4

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
</sub>

- 2. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.
- 3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.

This figure provides the AC test load for PCI.



Figure 48. PCI AC Test Load



This figure shows the PCI input AC timing conditions.



Figure 49. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.



15 Timers

This section describes the DC and AC electrical specifications for the timers.

15.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the MPC8313E timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V
Input high voltage	V _{IH}	_	2.1	NV _{DD} + 0.3	V
Input low voltage	V _{IL}	_	-0.3	0.8	V
Input current	I _{IN}	$0~V \leq V_{IN} \leq NV_{DD}$	_	±5	μA

Table 53. Timers DC Electrical Characteristics



Table 62. MPC8313E TEPBGAII Pi	inout Listing (continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Note
MEMC_MCS0	D10	0	GV _{DD}	_
MEMC_MCS1	A10	0	GV _{DD}	_
MEMC_MCKE	B14	0	GV _{DD}	3
MEMC_MCK	A13	0	GV _{DD}	_
MEMC_MCK	A14	0	GV _{DD}	_
MEMC_MODT0	B23	0	GV _{DD}	_
MEMC_MODT1	C23	0	GV _{DD}	_
Local Bus	Controller Interface			
LAD0	K25	I/O	LV _{DD}	11
LAD1	K24	I/O	LV _{DD}	11
LAD2	K23	I/O	LV _{DD}	11
LAD3	K22	I/O	LV _{DD}	11
LAD4	J25	I/O	LV _{DD}	11
LAD5	J24	I/O	LV _{DD}	11
LAD6	J23	I/O	LV _{DD}	11
LAD7	J22	I/O	LV _{DD}	11
LAD8	H24	I/O	LV _{DD}	11
LAD9	F26	I/O	LV _{DD}	11
LAD10	G24	I/O	LV _{DD}	11
LAD11	F25	I/O	LV _{DD}	11
LAD12	E25	I/O	LV _{DD}	11
LAD13	F24	I/O	LV _{DD}	11
LAD14	G22	I/O	LV _{DD}	11
LAD15	F23	I/O	LV _{DD}	11
LA16	AC25	0	LV _{DD}	11
LA17	AC26	0	LV _{DD}	11
LA18	AB22	0	LV _{DD}	11
LA19	AB23	0	LV _{DD}	11
LA20	AB24	0	LV _{DD}	11
LA21	AB25	0	LV _{DD}	11
LA22	AB26	0	LV _{DD}	11
LA23	E22	0	LV _{DD}	11



20 Clocking

This figure shows the internal distribution of clocks within the MPC8313E.



² Multiplication factor L = 2, 3, 4, 5, and 6. Value is decided by RCWLR[SPMF].





RCWL[SPMF]	System PLL Multiplication Factor
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

Table 65. System PLL Multiplication Factors (continued)

Note:

1. If RCWL[DDRCM] and RCWL[LBCM] are both cleared, the system PLL VCO frequency = (CSB frequency) × (System PLL VCO Divider).

2. If either RCWL[DDRCM] or RCWL[LBCM] are set, the system PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO Divider).

3. The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz

As described in Section 20, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (SYS_CLK_IN or PCI_SYNC_IN) and the internal coherent system bus clock (*csb_clk*). This table shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN/PCI_SYNC_IN ratios.

			Inp	out Clock Fre	equency (MH	lz) ²
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> :Input Clock Ratio ²	24	25	33.33	66.67
			csb_clk Frequency (MHz)
High	0010	2:1				133
High	0011	3:1			100	
High	0100	4:1		100	133	
High	0101	5:1	120	125	167	
High	0110	6:1	144	150		
Low	0010	2:1				133
Low	0011	3:1			100	
Low	0100	4:11		100	133	
Low	0101	5:1	120	125	167	
Low	0110	6:1	144	150		

Table 66. CSB Frequency Options

¹ CFG_CLKIN_DIV select the ratio between SYS_CLK_IN and PCI_SYNC_OUT.

² SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.



Table 69. Package Thermal Characteristics for TEPBGAII (continued)

Characteristic	Board Type	Symbol	TEPBGA II	Unit	Note
Junction-to-case	_	$R_{ ext{ heta}JC}$	8	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	7	°C/W	6

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

- 3. Per JEDEC JESD51-6 with the board horizontal.
- 4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- 6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

21.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

21.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 T_J = junction temperature (°C) T_A = ambient temperature for the package (°C) $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W) P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_I - T_A$) are possible.

21.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter



 $R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Heat Sink Assuming Thermal Grease	Airflow	Thermal Resistance (°C/W)
Wakefield 53 \times 53 \times 2.5 mm pin fin	Natural convection	13.0
	0.5 m/s	10.6
	1 m/s	9.7
	2 m/s	9.2
	4 m/s	8.9
Aavid 35 $\times~$ 31 \times 23 mm pin fin	Natural convection	14.4
	0.5 m/s	11.3
	1 m/s	10.5
	2 m/s	9.9
	4 m/s	9.4
Aavid $30 \times 30 \times 9.4$ mm pin fin	Natural convection	16.5
	0.5 m/s	13.5
	1 m/s	12.1
	2 m/s	10.9
	4 m/s	10.0
Aavid 43 \times 41 \times 16.5 mm pin fin	Natural convection	14.5
	0.5 m/s	11.7
	1 m/s	10.5
	2 m/s	9.7
	4 m/s	9.2

Table 70. Thermal Resistance for TEPBGAII with Heat Sink in Open Flow

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in Table 70. More detailed thermal models can be made available on request.



22.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1} , AV_{DD2} , and $SDAV_{DD}$, respectively). The AV_{DD} level should always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 58, one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

This figure shows the PLL power supply filter circuits.



Low ESL Surface Mount Capacitors

Figure 58. PLL Power Supply Filter Circuit

The SDAV_{DD} signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit like the one shown in Figure 59. For maximum effectiveness, the filter circuit should be placed as closely as possible to the SDAV_{DD} ball to ensure it filters out as much noise as possible. The ground connection should be near the SDAV_{DD} ball. The 0.003- μ F capacitor is closest to the ball, followed by the two 2.2- μ F capacitors, and finally the 1- Ω resistor to the board supply plane. The capacitors are connected from traces from SDAV_{DD} to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 59. SerDes PLL Power Supply Filter Circuit

Note the following:

• SDAV_{DD} should be a filtered version of XCOREV_{DD}.



- Output signals on the SerDes interface are fed from the XPADV_{DD} power plane. Input signals and sensitive transceiver analog circuits are on the XCOREV_{DD} supply.
- Power: XPADV_{DD} consumes less than 300 mW; XCOREV_{DD} + SDAV_{DD} consumes less than 750 mW.

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8313E system, and the MPC8313E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , NV_{DD} , GV_{DD} , LV_{DD} , LV_{DDA} , and LV_{DDB} pin of the device. These decoupling capacitors should receive their power from separate V_{DD} , NV_{DD} , GV_{DD} , LV_{DDA} , LV_{DDB} , and VSS power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , NV_{DD} , GV_{DD} , LV_{DD} , LV_{DDA} , and LV_{DDB} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100 to 330 μ F (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (XCOREV_{DD} and XPADV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor from each SerDes supply (XCOREV_{DD} and XPADV_{DD}) to the board ground plane on each side of the device. This should be done for all SerDes supplies.