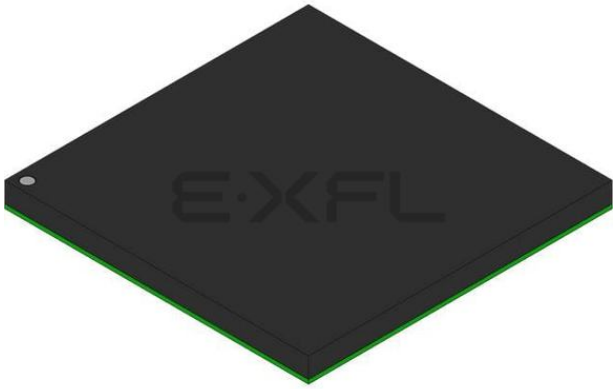

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300c3 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 267MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | USB 2.0 + PHY (1) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 516-BBGA Exposed Pad |
| Supplier Device Package | 516-TEPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8313cvraddb |

- Full and half-duplex Ethernet support (1000 Mbps supports only full-duplex):
  - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE 802.1 virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision
  - CRC generation and verification of inbound/outbound packets
  - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
  - Exact match on primary and virtual 48-bit unicast addresses
    - VRRP and HSRP support for seamless router fail-over
  - Up to 16 exact-match MAC addresses supported
  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status

## 1.8 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model supports 5 external and 34 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

## 1.9 Power Management Controller (PMC)

The MPC8313E power management controller includes the following features:

- Provides power management when the device is used in both host and agent modes
- Supports PCI power management 1.2 D0, D1, D2, D3hot, and D3cold states
- On-chip split power supply controlled through external power switch for minimum standby power
- Support for PME generation in PCI agent mode, PME detection in PCI host mode
- Supports wake-up from Ethernet (Magic Packet), USB, GPIO, and PCI (PME input as host)

## Table 2. Recommended Operating Conditions

| Characteristic | Symbol | Recommended Value[1] | Unit | Current Requirement |
|---|---|---|---|---|
| Core supply voltage | $V_{DD}$ | 1.0 V ± 50 mV | V | 469 mA |
| Internal core logic constant power | $V_{DDC}$ | 1.0 V ± 50 mV | V | 377 mA |
| SerDes internal digital power | $XCOREV_{DD}$ | 1.0 | V | 170 mA |
| SerDes internal digital ground | $XCOREV_{SS}$ | 0.0 | V | — |
| SerDes I/O digital power | $XPADV_{DD}$ | 1.0 | V | 10 mA |
| SerDes I/O digital ground | $XPADV_{SS}$ | 0.0 | V | — |
| SerDes analog power for PLL | $SDAV_{DD}$ | 1.0 V ± 50 mV | V | 10 mA |
| SerDes analog ground for PLL | $SDAV_{SS}$ | 0.0 | V | — |
| Dedicated 3.3 V analog power for USB PLL | USB_PLL_PWR3 | 3.3 V ± 300 mV | V | 2–3 mA |
| Dedicated 1.0 V analog power for USB PLL | USB_PLL_PWR1 | 1.0 V ± 50 mV | V | 2–3 mA |
| Dedicated analog ground for USB PLL | USB_PLL_GND | 0.0 | V | — |
| Dedicated USB power for USB bias circuit | USB_VDDA_BIAS | 3.3 V ± 300 mV | V | 4–5 mA |
| Dedicated USB ground for USB bias circuit | USB_VSSA_BIAS | 0.0 | V | — |
| Dedicated power for USB transceiver | USB_VDDA | 3.3 V ± 300 mV | V | 75 mA |
| Dedicated ground for USB transceiver | USB_VSSA | 0.0 | V | — |
| Analog power for e300 core APLL | $AV_{DD1}$ [6] | 1.0 V ± 50 mV | V | 2–3 mA |
| Analog power for system APLL | $AV_{DD2}$ [6] | 1.0 V ± 50 mV | V | 2–3 mA |
| DDR1 DRAM I/O voltage (333 MHz, 32-bit operation) | $GV_{DD}$ | 2.5 V ± 125 mV | V | 131 mA |
| DDR2 DRAM I/O voltage (333 MHz, 32-bit operation) | $GV_{DD}$ | 1.8 V ± 80 mV | V | 140 mA |
| Differential reference voltage for DDR controller | $MV_{REF}$ | 1/2 DDR supply ($0.49 \times GV_{DD}$ to $0.51 \times GV_{DD}$) | V | — |
| Standard I/O voltage | $NV_{DD}$ | 3.3 V ± 300 mV[2] | V | 74 mA |
| eTSEC2 I/O supply | $LV_{DDA}$ | 2.5 V ± 125 mV/ 3.3 V ± 300 mV | V | 22 mA |
| eTSEC1/USB DR I/O supply | $LV_{DDB}$ | 2.5 V ± 125 mV/ 3.3 V ± 300 mV | V | 44 mA |
| Supply for eLBC IOs | $LV_{DD}$ | 3.3 V ± 300 mV | V | 16 mA |
| Analog and digital ground | $V_{SS}$ | 0.0 | V | — |
| Junction temperature range | $T_A/T_J$ [3] | 0 to 105 | °C | |

# 3 Power Characteristics

The estimated typical power dissipation, not including I/O supply power, for this family of MPC8313E devices is shown in this table. Table 5 shows the estimated typical I/O power dissipation.

**Table 4. MPC8313E Power Dissipation[1]**

| Core Frequency (MHz) | CSB Frequency (MHz) | Typical[2] | Maximum for Rev. 1.0 Silicon[3] | Maximum for Rev. 2.x or Later Silicon[3] | Unit |
|---|---|---|---|---|---|
| 333 | 167 | 820 | 1020 | 1200 | mW |
| 400 | 133 | 820 | 1020 | 1200 | mW |

**Note:**

1. The values do not include I/O supply power or $AV_{DD}$, but do include core, USB PLL, and a portion of SerDes digital power (not including $XCOREV_{DD}$, $XPADV_{DD}$, or $SDAV_{DD}$, which all have dedicated power supplies for the SerDes PHY).
2. Typical power is based on a voltage of $V_{DD}$ = 1.05 V and an artificial smoker test running at room temperature.
3. Maximum power is based on a voltage of $V_{DD}$ = 1.05 V, a junction temperature of $T_J$ = 105°C, and an artificial smoker test.

This table describes a typical scenario where blocks with the stated percentage of utilization and impedances consume the amount of power described.

**Table 5. MPC8313E Typical I/O Power Dissipation**

| Interface | Parameter | $GV_{DD}$ (1.8 V) | $GV_{DD}$ (2.5 V) | $NV_{DD}$ (3.3 V) | $LV_{DDA}$/ $LV_{DDB}$ (3.3 V) | $LV_{DDA}$/ $LV_{DDB}$ (2.5 V) | $LV_{DD}$ (3.3 V) | Unit | Comments |
|---|---|---|---|---|---|---|---|---|---|
| DDR 1, 60% utilization, 50% read/write $R_s$ = 22 Ω $R_t$ = 50 Ω single pair of clock capacitive load: data = 8 pF, control address = 8 pF, clock = 8 pF | 333 MHz, 32 bits | — | 0.355 | — | — | — | — | W | — |
| | 266 MHz, 32 bits | — | 0.323 | — | — | — | — | W | — |
| DDR 2, 60% utilization, 50% read/write $R_s$ = 22 Ω $R_t$ = 75 Ω single pair of clock capacitive load: data = 8 pF, control address = 8 pF, clock = 8 pF | 333 MHz, 32 bits | 0.266 | — | — | — | — | — | W | — |
| | 266 MHz, 32 bits | 0.246 | — | — | — | — | — | W | — |
| PCI I/O load = 50 pF | 33 MHz | — | — | 0.120 | — | — | — | W | — |
| | 66 MHz | — | — | 0.249 | — | — | — | W | — |
| Local bus I/O load = 20 pF | 66 MHz | — | — | — | — | — | 0.056 | W | — |
| | 50 MHz | — | — | — | — | — | 0.040 | W | — |
| TSEC I/O load = 20 pF | MII, 25 MHz | — | — | — | 0.008 | — | — | W | Multiple by number of interface used |
| | RGMII, 125 MHz | — | — | — | 0.078 | 0.044 | — | W | |

## 4.2 AC Electrical Characteristics

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the system clock input (SYS_CLK_IN/PCI_CLK) AC timing specifications for the MPC8313E.

**Table 8. SYS_CLK_IN AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| SYS_CLK_IN/PCI_CLK frequency | $f_{SYS\_CLK\_IN}$ | 24 | — | 66.67 | MHz | 1 |
| SYS_CLK_IN/PCI_CLK cycle time | $t_{SYS\_CLK\_IN}$ | 15 | — | — | ns | — |
| SYS_CLK_IN rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | 0.8 | 4 | ns | 2 |
| PCI_CLK rise and fall time | $t_{PCH}$, $t_{PCL}$ | 0.6 | 0.8 | 1.2 | ns | 2 |
| SYS_CLK_IN/PCI_CLK duty cycle | $t_{KHK}/t_{SYS\_CLK\_IN}$ | 40 | — | 60 | % | 3 |
| SYS_CLK_IN/PCI_CLK jitter | — | — | — | ±150 | ps | 4, 5 |

**Notes:**
1. **Caution:** The system, core, security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN/PCI_CLK are measured at 0.4 and 2.4 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.

# 5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8313E.

## 5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins.

**Table 9. RESET Pins DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 2.1 | $NV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le NV_{DD}$ | — | ±5 | μA |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |

This figure provides the AC test load for the DDR bus.

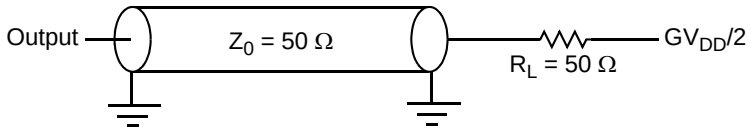


**Figure 7. DDR AC Test Load**

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

## 7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

**Table 22. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2.0 | $NV_{DD}$ + 0.3 | V |
| Low-level input voltage $NV_{DD}$ | $V_{IL}$ | –0.3 | 0.8 | V |
| High-level output voltage, $I_{OH}$ = –100 μA | $V_{OH}$ | $NV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 μA | $V_{OL}$ | — | 0.2 | V |
| Input current (0 V ≤$V_{IN}$ ≤ $NV_{DD}$) | $I_{IN}$ | — | ±5 | μA |

## 7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

**Table 23. DUART AC Timing Specifications**

| Parameter | Value | Unit | Note |
|---|---|---|---|
| Minimum baud rate | 256 | baud | — |
| Maximum baud rate | > 1,000,000 | baud | 1 |
| Oversample rate | 16 | — | 2 |

**Notes:**
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8$^{th}$ sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16$^{th}$ sample.

# 8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

## 8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all the media independent interface (MII), reduced gigabit media independent interface (RGMII), serial gigabit media independent interface (SGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the MII interface can be operated at 3.3 V. The RMII and SGMII interfaces can be operated at either 3.3 or 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for *Gigabit Ethernet Physical Layer Device Specification Version 1.2*a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.5, "Ethernet Management Interface Electrical Characteristics."

### 8.1.1 TSEC DC Electrical Characteristics

All RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

**NOTE**

eTSEC should be interfaced with peripheral operating at same voltage level.

**Table 24. MII DC Electrical Characteristics**

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage 3.3 V | $LV_{DDA}/LV_{DDB}$ | — | | 2.97 | 3.63 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –4.0 mA | $LV_{DDA}$ or $LV_{DDB}$ = Min | 2.40 | $LV_{DDA}$ + 0.3 or $LV_{DDB}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 4.0 mA | $LV_{DDA}$ or $LV_{DDB}$ = Min | $V_{SS}$ | 0.50 | V |
| Input high voltage | $V_{IH}$ | — | — | 2.0 | $LV_{DDA}$ + 0.3 or $LV_{DDB}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | — | –0.3 | 0.90 | V |
| Input high current | $I_{IH}$ | $V_{IN}$[1] = $LV_{DDA}$ or $LV_{DDB}$ | | — | 40 | μA |
| Input low current | $I_{IL}$ | $V_{IN}$[1] = VSS | | –600 | — | μA |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ symbol referenced in Table 1 and Table 2.

**Table 25. RGMII/RTBI DC Electrical Characteristics**

| Parameters | Symbol | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage 2.5 V | $LV_{DDA}/LV_{DDB}$ | — | 2.37 | 2.63 | V |

### 8.3.2 AC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

This table lists the SGMII SerDes reference clock AC requirements. Note that SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

**Table 31. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements**

| Symbol | Parameter Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{REF}$ | REFCLK cycle time | — | 8 | — | ns |
| $t_{REFCJ}$ | REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles | — | — | 100 | ps |
| $t_{REFPJ}$ | Phase jitter. Deviation in edge location with respect to mean edge location | –50 | — | 50 | ps |

### 8.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 32 and Table 33 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX[*n*] and $\overline{\text{SD\_TX}}$[*n*]) as depicted in Figure 16.

**Table 32. SGMII DC Transmitter Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage | $XCOREV_{DD}$ | 0.95 | 1.0 | 1.05 | V | |
| Output high voltage | $V_{OH}$ | — | — | $XCOREV_{DD\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-max}}/2$ | mV | 1 |
| Output low voltage | $V_{OL}$ | $XCOREV_{DD\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-max}}/2$ | — | — | mV | 1 |
| Output ringing | $V_{RING}$ | — | — | 10 | % | |
| Output differential voltage[2, 3] | $\lvert V_{OD}\rvert$ | 323 | 500 | 725 | mV | Equalization setting: 1.0x |
| Output offset voltage | $V_{OS}$ | 425 | 500 | 575 | mV | 1, 4 |
| Output impedance (single-ended) | $R_O$ | 40 | — | 60 | Ω | |
| Mismatch in a pair | $\Delta R_O$ | — | — | 10 | % | |
| Change in $V_{OD}$ between 0 and 1 | $\Delta\lvert V_{OD}\rvert$ | — | — | 25 | mV | |
| Change in $V_{OS}$ between 0 and 1 | $\Delta V_{OS}$ | — | — | 25 | mV | |
| Output current on short to GND | $I_{SA}$, $I_{SB}$ | — | — | 40 | mA | |

**Notes:**

1. This will not align to DC-coupled SGMII. $XCOREV_{DD\text{-}Typ}$ = 1.0 V.
2. $\lvert V_{OD}\rvert = \lvert V_{TXn} - V_{\overline{TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $XCOREV_{DD\text{-}Typ}$ = 1.0 V, no common mode offset variation ($V_{OS}$ = 500 mV), SerDes transmitter is terminated with 100-Ω differential load between TX[*n*] and $\overline{\text{TX}}$[*n*].
4. $V_{OS}$ is also referred to as output common mode voltage.

of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

— For external DC-coupled connection, as described in Section 9.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 24 shows the SerDes reference clock input requirement for the DC-coupled connection scheme.

— For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to $XCOREV_{SS}$. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage ($XCOREV_{SS}$). Figure 25 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- Single-ended mode

— The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-to-peak (from $V_{min}$ to $V_{max}$) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.

— The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 26 shows the SerDes reference clock input requirement for the single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC coupled externally. For the best noise performance, the reference of the clock could be DC or AC coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

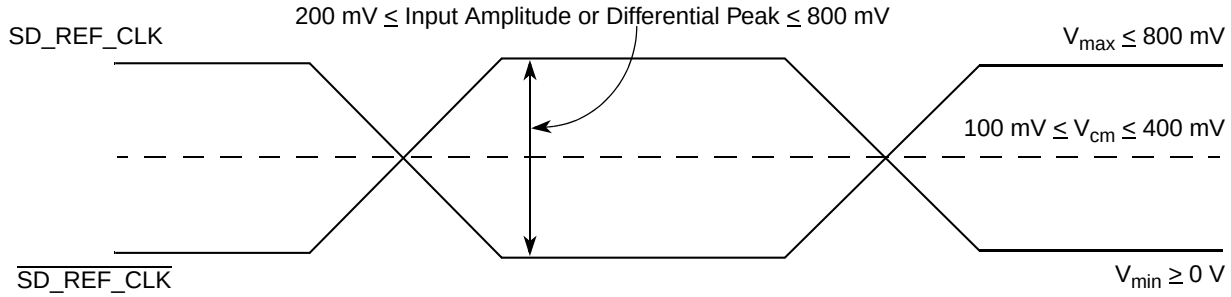


**Figure 24. Differential Reference Clock Input DC Requirements (External DC-Coupled)**

### 9.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low-phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters for SGMII protocol.

**Table 39. SerDes Reference Clock Common AC Parameters**

At recommended operating conditions with $XV_{DD\_SRDS1}$ or $XV_{DD\_SRDS2}$ = 1.0 V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Rising edge rate | Rise edge rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Falling edge rate | Fall edge rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Differential input high voltage | $V_{IH}$ | +200 | — | mV | 2 |
| Differential input low voltage | $V_{IL}$ | — | –200 | mV | 2 |
| Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn\_REF\_CLK}}$) matching | Rise-fall matching | — | 20 | % | 1, 4 |

**Notes:**
1. Measurement taken from single-ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 31.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point, where SD*n*_REF_CLK rising meets $\overline{\text{SD}n\text{\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK should be compared to the fall edge rate of $\overline{\text{SD}n\text{\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 32.

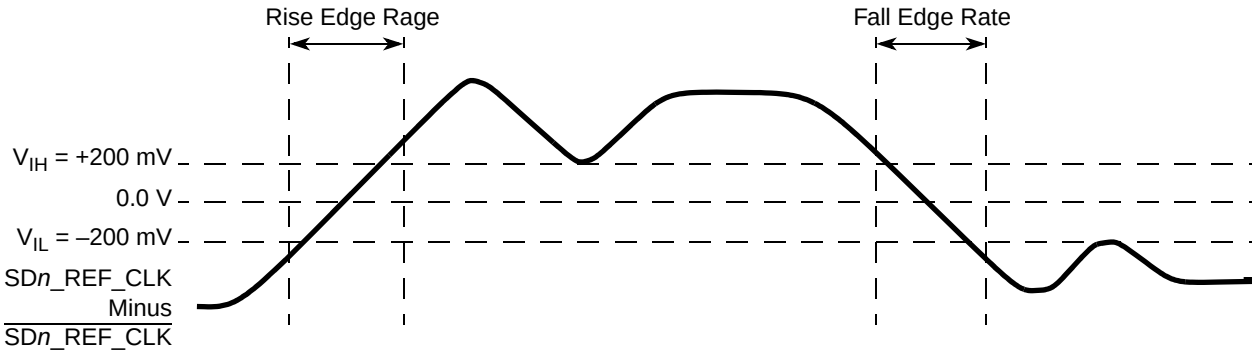


**Figure 31. Differential Measurement Points for Rise and Fall Time**

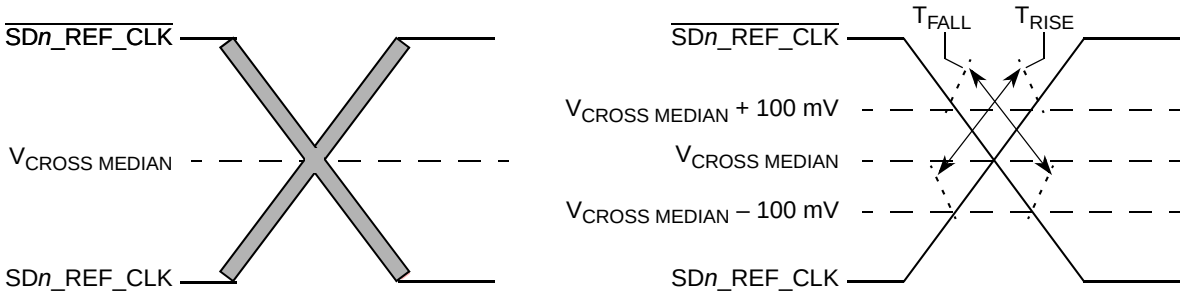


**Figure 32. Single-Ended Measurement Points for Rise and Fall Time Matching**

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. Refer to the following section for detailed information:

- Section 8.3.2, "AC Requirements for SGMII SD_REF_CLK and SD_REF_CLK"

#### 9.2.4.1 Spread Spectrum Clock

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

## 9.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for the SerDes data lane's transmitter and receiver.

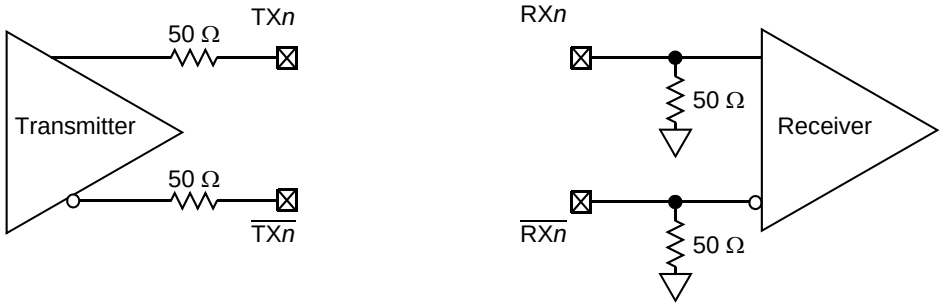


**Figure 33. SerDes Transmitter and Receiver Reference Circuits**

The SerDes data lane's DC and AC specifications are defined in the interface protocol section listed below (SGMII) based on the application usage:

- Section 8.3, "SGMII Interface Electrical Characteristics"

Please note that a external AC-coupling capacitor is required for the above serial transmission protocol with the capacitor value defined in the specifications of the protocol section.

# 12 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

## 12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE Std 1149.1 (JTAG) interface.

**Table 46. JTAG Interface DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 2.1 | $NV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | — | ±5 | μA |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |

## 12.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std 1149.1 (JTAG) interface. This table provides the JTAG AC timing specifications as defined in Figure 41 through Figure 45.

**Table 47. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)[1]**

At recommended operating conditions (see Table 2).

| Parameter | Symbol[2] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | |
| JTAG external clock pulse width measured at 1.4 V | $t_{JTKHKL}$ | 15 | — | ns | |
| JTAG external clock rise and fall times | $t_{JTGR}$ & $t_{JTGF}$ | 0 | 2 | ns | |
| $\overline{TRST}$ assert time | $t_{TRST}$ | 25 | — | ns | 3 |
| Input setup times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDVKH}$<br>$t_{JTIVKH}$ | <br>4<br>4 | <br>—<br>— | ns | 4 |
| Input hold times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDXKH}$<br>$t_{JTIXKH}$ | <br>10<br>10 | <br>—<br>— | ns | 4 |
| Valid times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDV}$<br>$t_{JTKLOV}$ | <br>2<br>2 | <br>11<br>11 | ns | 5 |
| Output hold times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | <br>2<br>2 | <br>—<br>— | ns | 5 |

This figure shows the AC timing diagram for the $I^2C$ bus.

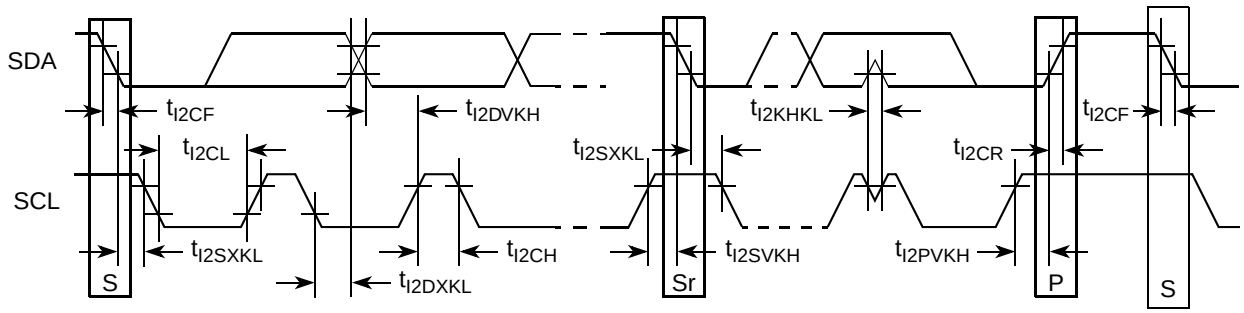


**Figure 47. $I^2C$ Bus AC Timing Diagram**

# 14 PCI

This section describes the DC and AC electrical specifications for the PCI bus.

## 14.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface.

**Table 50. PCI DC Electrical Characteristics[1]**

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | $V_{OUT} \geq V_{OH}$ (min) or | 0.5 × $NV_{DD}$ | $NV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | $V_{OUT} \leq V_{OL}$ (max) | –0.5 | 0.3 × $NV_{DD}$ | V |
| High-level output voltage | $V_{OH}$ | $NV_{DD}$ = min, $I_{OH}$ = –100 µA | 0.9 × $NV_{DD}$ | — | V |
| Low-level output voltage | $V_{OL}$ | $NV_{DD}$ = min, $I_{OL}$ = 100 µA | — | 0.1 × $NV_{DD}$ | V |
| Input current | $I_{IN}$ | 0 V ≤ $V_{IN}$ ≤ $NV_{DD}$ | — | ±5 | µA |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $NV_{IN}$ symbol referenced in Table 1 and Table 2.

## 14.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8313E is configured as a host or agent device.

This table shows the PCI AC timing specifications at 66 MHz.

**Table 51. PCI AC Timing Specifications at 66 MHz**

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Clock to output valid | $t_{PCKHOV}$ | — | 6.0 | ns | 2 |
| Output hold from clock | $t_{PCKHOX}$ | 1 | — | ns | 2 |

**Table 62. MPC8313E TEPBGAII Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| $\overline{\text{MEMC\_MCS0}}$ | D10 | O | $GV_{DD}$ | — |
| $\overline{\text{MEMC\_MCS1}}$ | A10 | O | $GV_{DD}$ | — |
| MEMC_MCKE | B14 | O | $GV_{DD}$ | 3 |
| MEMC_MCK | A13 | O | $GV_{DD}$ | — |
| $\overline{\text{MEMC\_MCK}}$ | A14 | O | $GV_{DD}$ | — |
| MEMC_MODT0 | B23 | O | $GV_{DD}$ | — |
| MEMC_MODT1 | C23 | O | $GV_{DD}$ | — |
| **Local Bus Controller Interface** | | | | |
| LAD0 | K25 | I/O | $LV_{DD}$ | 11 |
| LAD1 | K24 | I/O | $LV_{DD}$ | 11 |
| LAD2 | K23 | I/O | $LV_{DD}$ | 11 |
| LAD3 | K22 | I/O | $LV_{DD}$ | 11 |
| LAD4 | J25 | I/O | $LV_{DD}$ | 11 |
| LAD5 | J24 | I/O | $LV_{DD}$ | 11 |
| LAD6 | J23 | I/O | $LV_{DD}$ | 11 |
| LAD7 | J22 | I/O | $LV_{DD}$ | 11 |
| LAD8 | H24 | I/O | $LV_{DD}$ | 11 |
| LAD9 | F26 | I/O | $LV_{DD}$ | 11 |
| LAD10 | G24 | I/O | $LV_{DD}$ | 11 |
| LAD11 | F25 | I/O | $LV_{DD}$ | 11 |
| LAD12 | E25 | I/O | $LV_{DD}$ | 11 |
| LAD13 | F24 | I/O | $LV_{DD}$ | 11 |
| LAD14 | G22 | I/O | $LV_{DD}$ | 11 |
| LAD15 | F23 | I/O | $LV_{DD}$ | 11 |
| LA16 | AC25 | O | $LV_{DD}$ | 11 |
| LA17 | AC26 | O | $LV_{DD}$ | 11 |
| LA18 | AB22 | O | $LV_{DD}$ | 11 |
| LA19 | AB23 | O | $LV_{DD}$ | 11 |
| LA20 | AB24 | O | $LV_{DD}$ | 11 |
| LA21 | AB25 | O | $LV_{DD}$ | 11 |
| LA22 | AB26 | O | $LV_{DD}$ | 11 |
| LA23 | E22 | O | $LV_{DD}$ | 11 |

**Table 62. MPC8313E TEPBGAII Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| LA14/TSEC_1588_TRIG1 | L24 | O | $LV_{DD}$ | 8 |
| LA15/TSEC_1588_ALARM2 | K26 | O | $LV_{DD}$ | 8 |
| **DUART** | | | | |
| UART_SOUT1/MSRCID0 | N2 | O | $NV_{DD}$ | — |
| UART_SIN1/MSRCID1 | M5 | I/O | $NV_{DD}$ | — |
| $\overline{\text{UART\_CTS1}}$/GPIO8/MSRCID2 | M1 | I/O | $NV_{DD}$ | — |
| $\overline{\text{UART\_RTS1}}$/GPIO9/MSRCID3 | K1 | I/O | $NV_{DD}$ | — |
| UART_SOUT2/MSRCID4/TSEC_1588_CLK | M3 | O | $NV_{DD}$ | 8 |
| UART_SIN2/MDVAL/TSEC_1588_GCLK | L1 | I/O | $NV_{DD}$ | 8 |
| $\overline{\text{UART\_CTS2}}$/TSEC_1588_PP1 | L5 | I/O | $NV_{DD}$ | 8 |
| $\overline{\text{UART\_RTS2}}$/TSEC_1588_PP2 | L3 | I/O | $NV_{DD}$ | 8 |
| **$I^2C$ interface** | | | | |
| IIC1_SDA/$\overline{\text{CKSTOP\_OUT}}$/TSEC_1588_TRIG1 | J4 | I/O | $NV_{DD}$ | 2, 8 |
| IIC1_SCL/$\overline{\text{CKSTOP\_IN}}$/TSEC_1588_ALARM2 | J2 | I/O | $NV_{DD}$ | 2, 8 |
| IIC2_SDA/PMC_PWR_OK/GPIO10 | J3 | I/O | $NV_{DD}$ | 2 |
| IIC2_SCL/GPIO11 | H5 | I/O | $NV_{DD}$ | 2 |
| **Interrupts** | | | | |
| $\overline{\text{MCP\_OUT}}$ | G5 | O | $NV_{DD}$ | 2 |
| $\overline{\text{IRQ0}}$/$\overline{\text{MCP\_IN}}$ | K5 | I | $NV_{DD}$ | — |
| $\overline{\text{IRQ1}}$ | K4 | I | $NV_{DD}$ | — |
| $\overline{\text{IRQ2}}$ | K2 | I | $NV_{DD}$ | — |
| $\overline{\text{IRQ3}}$/$\overline{\text{CKSTOP\_OUT}}$ | K3 | I/O | $NV_{DD}$ | — |
| $\overline{\text{IRQ4}}$/$\overline{\text{CKSTOP\_IN}}$/GPIO12 | J1 | I/O | $NV_{DD}$ | — |
| **Configuration** | | | | |
| $\overline{\text{CFG\_CLKIN\_DIV}}$ | D5 | I | $NV_{DD}$ | — |
| EXT_PWR_CTRL | J5 | O | $NV_{DD}$ | — |
| CFG_LBIU_MUX_EN | R24 | I | $NV_{DD}$ | — |
| **JTAG** | | | | |
| TCK | E1 | I | $NV_{DD}$ | — |
| TDI | E2 | I | $NV_{DD}$ | 4 |
| TDO | E3 | O | $NV_{DD}$ | 3 |

**Table 62. MPC8313E TEPBGAII Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| TSEC1_TXD1/TSEC_1588_PP2 | AD6 | O | $LV_{DDB}$ | — |
| TSEC1_TXD0/USBDR_STP/TSEC_1588_PP3 | AD5 | O | $LV_{DDB}$ | — |
| TSEC1_TX_EN/TSEC_1588_ALARM1 | AB7 | O | $LV_{DDB}$ | — |
| TSEC1_TX_ER/TSEC_1588_ALARM2 | AB8 | O | $LV_{DDB}$ | — |
| TSEC1_GTX_CLK125 | AE1 | I | $LV_{DDB}$ | — |
| TSEC1_MDC/LB_POR_CFG_BOOT_ECC_DIS | AF6 | O | $NV_{DD}$ | 9, 11 |
| TSEC1_MDIO | AB9 | I/O | $NV_{DD}$ | — |
| **ETSEC2** | | | | |
| TSEC2_COL/GTM1_TIN4/GTM2_TIN3/GPIO15 | AB4 | I/O | $LV_{DDA}$ | — |
| TSEC2_CRS/$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$/GPIO16 | AB3 | I/O | $LV_{DDA}$ | — |
| TSEC2_GTX_CLK/$\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$/GPIO17 | AC1 | I/O | $LV_{DDA}$ | 12 |
| TSEC2_RX_CLK/GTM1_TIN2/GTM2_TIN1/GPIO18 | AC2 | I/O | $LV_{DDA}$ | — |
| TSCE2_RX_DV/$\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$/GPIO19 | AA3 | I/O | $LV_{DDA}$ | — |
| TSEC2_RXD3/GPIO20 | Y5 | I/O | $LV_{DDA}$ | — |
| TSEC2_RXD2/GPIO21 | AA4 | I/O | $LV_{DDA}$ | — |
| TSEC2_RXD1/GPIO22 | AB2 | I/O | $LV_{DDA}$ | — |
| TSEC2_RXD0/GPIO23 | AA5 | I/O | $LV_{DDA}$ | — |
| TSEC2_RX_ER/$\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$/GPIO24 | AA2 | I/O | $LV_{DDA}$ | — |
| TSEC2_TX_CLK/GPIO25 | AB1 | I/O | $LV_{DDA}$ | — |
| TSEC2_TXD3/CFG_RESET_SOURCE0 | W3 | I/O | $LV_{DDA}$ | — |
| TSEC2_TXD2/CFG_RESET_SOURCE1 | Y1 | I/O | $LV_{DDA}$ | — |
| TSEC2_TXD1/CFG_RESET_SOURCE2 | W5 | I/O | $LV_{DDA}$ | — |
| TSEC2_TXD0/CFG_RESET_SOURCE3 | Y3 | I/O | $LV_{DDA}$ | — |
| TSEC2_TX_EN/GPIO26 | AA1 | I/O | $LV_{DDA}$ | — |
| TSEC2_TX_ER/GPIO27 | W1 | I/O | $LV_{DDA}$ | — |
| **SGMII PHY** | | | | |
| TXA | U3 | O | | — |
| $\overline{\text{TXA}}$ | V3 | O | | — |
| RXA | U1 | I | | — |
| $\overline{\text{RXA}}$ | V1 | I | | — |
| TXB | P4 | O | | — |
| $\overline{\text{TXB}}$ | N4 | O | | — |

**Table 62. MPC8313E TEPBGAII Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| $V_{SS}$ | B1,B2,B8,B9,B16,B17,C1, C2,C3,C4,C5,C24,C25, C26,D3,D4,D12,D13,D20, D21,F8,F11,F13,F16,F17, F21,G2,G25,H2,H6,H21, H25,L4,L6,L11,L12,L13, L14,L15,L16,L21,L23,M4, M11,M12,M13,M14,M15, M16,M23,N6,N11,N12, N13,N14,N15,N16, N21,N23,P11,P12,P13, P14,P15,P16,P23,P25, R11,R12,R13,R14,R15, R16,R25,T6,T11,T12,T13, T14,T15,T16,T21,T25,U5, U6,U21,W4,W23,Y4,Y23, AA8,AA11,AA13,AA16, AA17,AA21,AC4,AC5, AC12,AC13,AC20,AC21, AD1,AE2,AE8,AE9,AE16, AE17,AF2 | — | — | — |
| $XCOREV_{DD}$ | T1,U2,V2 | Core power for SerDes transceivers (1.0 V) | — | — |
| $XCOREV_{SS}$ | P2,R2,T3 | — | — | — |
| $XPADV_{DD}$ | P5,U4 | Pad power for SerDes transceivers (1.0 V) | — | — |
| $XPADV_{SS}$ | P3,V4 | — | — | — |

**Notes:**
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to $NV_{DD}$.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to $NV_{DD}$.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. This pin must always be tied to $V_{SS}$.
7. Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.
8. 1588 signals are available on these pins only in MPC8313 Rev 2.x or later.
9. LB_POR_CFG_BOOT_ECC_DIS is available only in MPC8313 Rev 2.x or later.
10. This pin has an internal pull-up.
11. This pin has an internal pull-down.
12. In MII mode, GTX_CLK should be pulled down by 300Ω to $V_{SS}$.

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$T_J$ = junction temperature (°C)
$T_B$ = board temperature at the package perimeter (°C)
$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51–8
$P_D$ = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

### 21.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$T_J$ = junction temperature (°C)
$T_T$ = thermocouple temperature on top of package (°C)
$\Psi_{JT}$ = thermal characterization parameter (°C/W)
$P_D$ = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

### 21.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to- ambient thermal resistance (°C/W)

Heat sink Vendors include the following list:

| | |
|---|---|
| Aavid Thermalloy<br>80 Commercial St.<br>Concord, NH 03301<br>Internet: www.aavidthermalloy.com | 603-224-9988 |
| Alpha Novatech<br>473 Sapena Ct. #12<br>Santa Clara, CA 95054<br>Internet: www.alphanovatech.com | 408-749-7601 |
| International Electronic Research Corporation (IERC)<br>413 North Moss St.<br>Burbank, CA 91502<br>Internet: www.ctscorp.com | 818-842-7277 |
| Millennium Electronics (MEI)<br>Loroco Sites<br>671 East Brokaw Road<br>San Jose, CA 95112<br>Internet: www.mei-thermal.com | 408-436-8770 |
| Tyco Electronics<br>Chip Coolers™<br>P.O. Box 3668<br>Harrisburg, PA 17105<br>Internet: www.chipcoolers.com | 800-522-6752 |
| Wakefield Engineering<br>33 Bridge St.<br>Pelham, NH 03076<br>Internet: www.wakefield.com | 603-635-2800 |

Interface material vendors include the following:

| | |
|---|---|
| Chomerics, Inc.<br>77 Dragon Ct.<br>Woburn, MA 01801<br>Internet: www.chomerics.com | 781-935-4850 |
| Dow-Corning Corporation<br>Corporate Center<br>PO BOX 994<br>Midland, MI 48686-0994<br>Internet: www.dowcorning.com | 800-248-2481 |
| Shin-Etsu MicroSi, Inc.<br>10028 S. 51st St.<br>Phoenix, AZ 85044<br>Internet: www.microsi.com | 888-642-7674 |
| The Bergquist Company<br>18930 West 78th St.<br>Chanhassen, MN 55317<br>Internet: www.bergquistcompany.com | 800-347-4572 |

**Table 73. Document Revision History (continued)**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 1 | 3/2008 | • In Table 63, added LBC_PM_REF_10 & LSRCID3 as muxed with USBDR_PCTL1<br>• In Table 63, added LSRCID2 as muxed with USBDR_PCTL0<br>• In Table 63, added LSRCID1 as muxed with USBDR_PWRFAULT<br>• In Table 63, added LSRCID0 as muxed with USBDR_DRIVE_VBUS<br>• In Table 63, moved T1, U2,& V2 from $V_{DD}$ to XCOREVDD.<br>• In Table 63, moved P2, R2, & T3 from $V_{SS}$ to XCOREVSS.<br>• In Table 63, moved P5, & U4 from $V_{DD}$ to XPADVDD.<br>• In Table 63, moved P3, & V4 from $V_{SS}$ to XPADVSS.<br>• In Table 63, removed “Double with pad” for $AV_{DD1}$ and $AV_{DD2}$ and moved $AV_{DD1}$ and $AV_{DD2}$ to Power and Ground Supplies section<br>• In Table 63, added impedance control requirements for SD_IMP_CAL_TX (100 ohms to GND) and SD_IMP_CAL_RX (200 ohms to GND).<br>• In Table 63, updated muxing in pinout to show new options for selecting IEEE 1588 functionality. Added footnote 8<br>• In Table 63, updated muxing in pinout to show new LBC ECC boot enable control muxed with eTSEC1_MDC<br>• Added pin type information for power supplies.<br>• Removed N1 and N3 from Vss section of Table 63. Added Therm0 and Therm1 (N1 and N3, respectively). Added note 7 to state: “Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.”<br>• In Table 65 corrected maximum frequency of Local Bus Frequency from “33–66” to 66 MHz<br>• In Table 65 corrected maximum frequency of PCI from “24–66” to 66 MHz<br>• Added “which is determined by RCWLR[COREPLL],” to the note in Section 20.2, “Core PLL Configuration” about the VCO divider.<br>• Added “(VCOD)” next to VCO divider column in Table 68. Added footnote stating that core_clk frequency must not exceed its maximum, so 2.5:1 and 3:1 *core_clk:csb_clk* ratios are invalid for certain *csb_clk* values.<br>• In Table 69, notes were confusing. Added note 3 for VCO column, note 4 for CSB (*csb_clk*) column, note 5 for USB ref column, and note 6 to replace “Note 1”. Clarified note 4 to explain erratum eTSEC40.<br>• In Table 69, updated note 6 to specify USB reference clock frequencies limited to 24 and 48 for rev. 2 silicon.<br>• Replaced Table 71 “Thermal Resistance for TEPBGAII with Heat Sink in Open Flow”.<br>• Removed last row of Table 19.<br>• Removed 200 MHz rows from Table 21 and Table 5.<br>• Changed VIH minimum spec from 2.0 to 2.1 for clock, PIC, JTAG, SPI, and reset pins in Table 9, Table 47, Table 54, Table 59, and Table 61.<br>• Added Figure 4 showing the DDR input timing diagram.<br>• In Table 19, removed “MDM” from the “MDQS-MDQ/MECC/MDM” text under the Parameter column for the tCISKEW parameter. MDM is an output signal and should be removed from the input AC timing spec table (tCISKEW).<br>• Added “and power” to rows 2 and 3 in Table 10<br>• Added the sentence “Once both the power supplies...” and PORESET to Section 2.2, “Power Sequencing,” and Figure 3.<br>• In Figure 35, corrected “USB0_CLK/USB1_CLK/DR_CLK” with “USBDR_CLK”<br>• In Table 42, clarified that AC specs are for ULPI only. |
| 0 | 6/2007 | Initial release. |

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