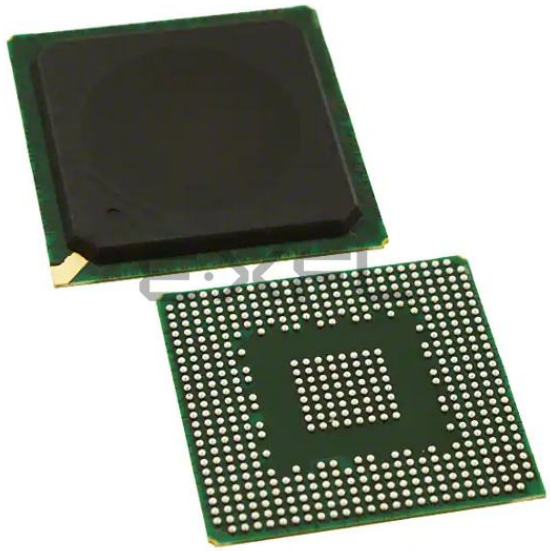


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8313cvragdb

3 Power Characteristics

The estimated typical power dissipation, not including I/O supply power, for this family of MPC8313E devices is shown in this table. Table 5 shows the estimated typical I/O power dissipation.

Table 4. MPC8313E Power Dissipation[1]

Core Frequency (MHz)	CSB Frequency (MHz)	Typical[2]	Maximum for Rev. 1.0 Silicon[3]	Maximum for Rev. 2.x or Later Silicon[3]	Unit
333	167	820	1020	1200	mW
400	133	820	1020	1200	mW

Note:

1. The values do not include I/O supply power or AV_{DD}, but do include core, USB PLL, and a portion of SerDes digital power (not including $XCOREV_{DD}$, $XPADV_{DD}$, or $SDAV_{DD}$, which all have dedicated power supplies for the SerDes PHY).
2. Typical power is based on a voltage of V_{DD} = 1.05 V and an artificial smoker test running at room temperature.
3. Maximum power is based on a voltage of V_{DD} = 1.05 V, a junction temperature of T_J = 105°C, and an artificial smoker test.

This table describes a typical scenario where blocks with the stated percentage of utilization and impedances consume the amount of power described.

Table 5. MPC8313E Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	NV_{DD} (3.3 V)	LV_{DDA}/ LV_{DDB} (3.3 V)	LV_{DDA}/ LV_{DDB} (2.5 V)	LV_{DD} (3.3 V)	Unit	Comments
DDR 1, 60% utilization, 50% read/write R_s = 22 Ω R_t = 50 Ω single pair of clock capacitive load: data = 8 pF, control address = 8 pF, clock = 8 pF	333 MHz, 32 bits	—	0.355	—	—	—	—	W	—
	266 MHz, 32 bits	—	0.323	—	—	—	—	W	—
DDR 2, 60% utilization, 50% read/write R_s = 22 Ω R_t = 75 Ω single pair of clock capacitive load: data = 8 pF, control address = 8 pF, clock = 8 pF	333 MHz, 32 bits	0.266	—	—	—	—	—	W	—
	266 MHz, 32 bits	0.246	—	—	—	—	—	W	—
PCI I/O load = 50 pF	33 MHz	—	—	0.120	—	—	—	W	—
	66 MHz	—	—	0.249	—	—	—	W	—
Local bus I/O load = 20 pF	66 MHz	—	—	—	—	—	0.056	W	—
	50 MHz	—	—	—	—	—	0.040	W	—
TSEC I/O load = 20 pF	MII, 25 MHz	—	—	—	0.008	—	—	W	Multiple by number of interface used
	RGMII, 125 MHz	—	—	—	0.078	0.044	—	W	

NOTE

For the ADDR/CMD setup and hold specifications in Table 21, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

This figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

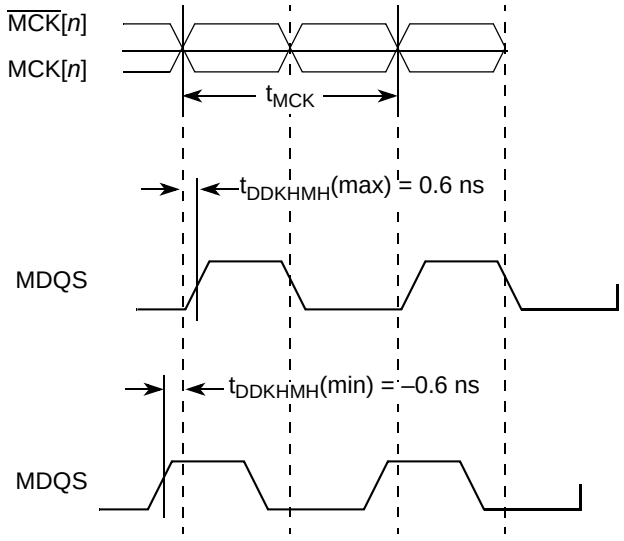


Figure 5. Timing Diagram for t_{DDKHMH}

This figure shows the DDR and DDR2 SDRAM output timing diagram.

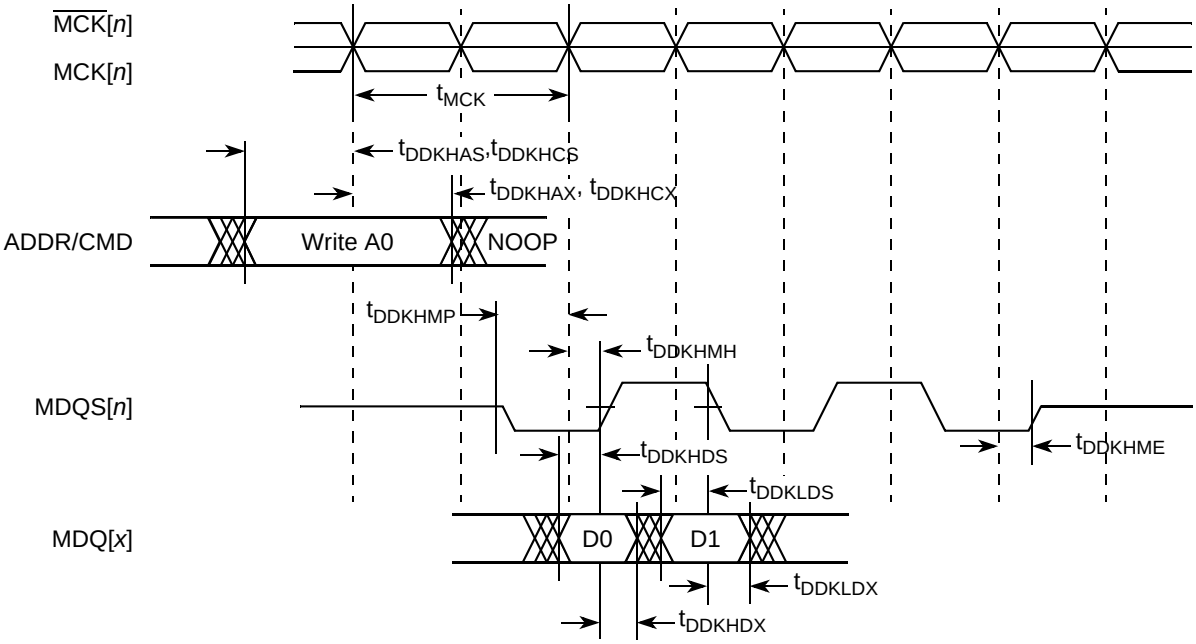


Figure 6. DDR and DDR2 SDRAM Output Timing Diagram

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all the media independent interface (MII), reduced gigabit media independent interface (RGMII), serial gigabit media independent interface (SGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the MII interface can be operated at 3.3 V. The RMII and SGMII interfaces can be operated at either 3.3 or 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for *Gigabit Ethernet Physical Layer Device Specification Version 1.2*a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.5, "Ethernet Management Interface Electrical Characteristics."

8.1.1 TSEC DC Electrical Characteristics

All RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

NOTE

eTSEC should be interfaced with peripheral operating at same voltage level.

Table 24. MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DDA}/LV_{DDB}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LV_{DDA} or LV_{DDB} = Min	2.40	LV_{DDA} + 0.3 or LV_{DDB} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LV_{DDA} or LV_{DDB} = Min	V_{SS}	0.50	V
Input high voltage	V_{IH}	—	—	2.0	LV_{DDA} + 0.3 or LV_{DDB} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DDA} or LV_{DDB}		—	40	μA
Input low current	I_{IL}	V_{IN}[1] = VSS		–600	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 25. RGMII/RTBI DC Electrical Characteristics

Parameters	Symbol	Conditions	Min	Max	Unit
Supply voltage 2.5 V	LV_{DDA}/LV_{DDB}	—	2.37	2.63	V

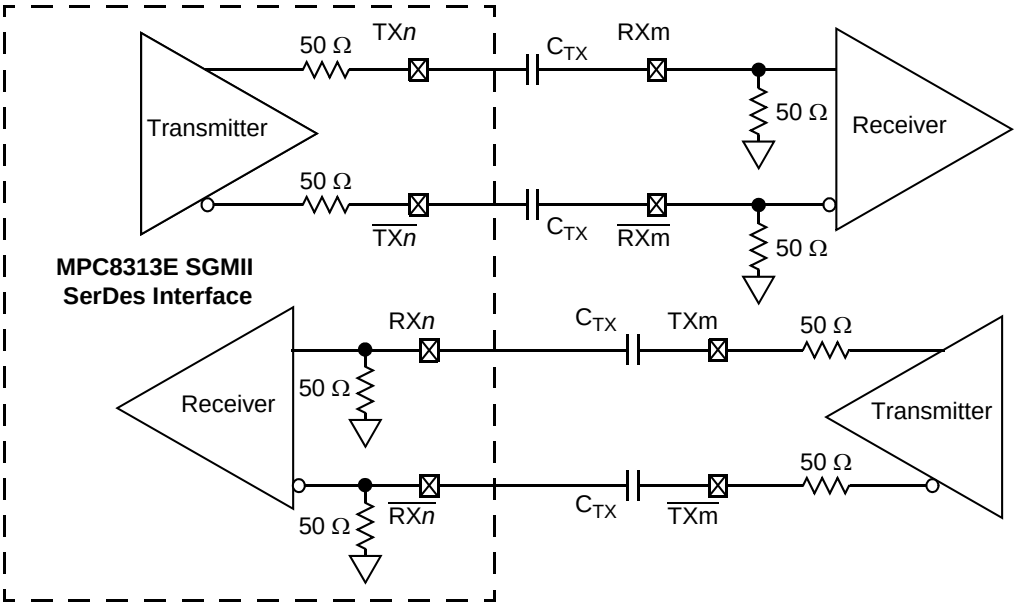


Figure 15. 4-Wire AC-Coupled SGMII Serial Link Connection Example

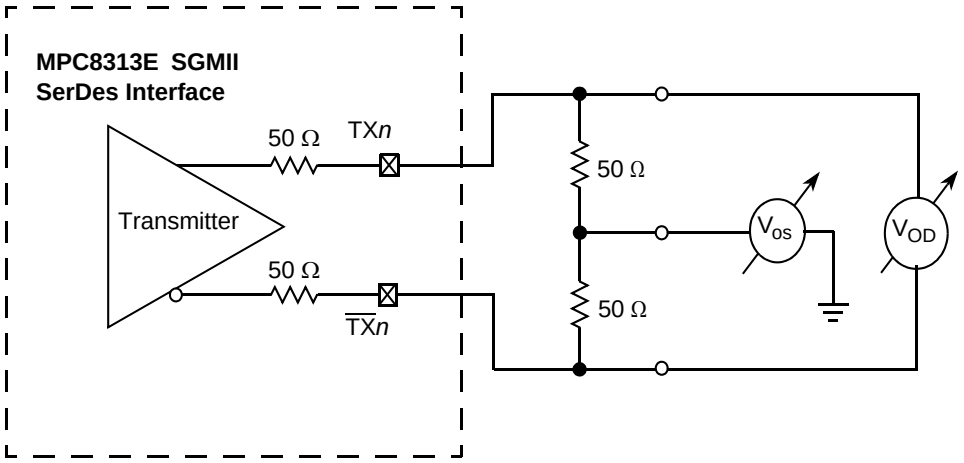


Figure 16. SGMII Transmitter DC Measurement Circuit

Table 33. SGMII DC Receiver Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$XCOREV_{DD}$	0.95	1.0	1.05	V	
DC Input voltage range			N/A			1
Input differential voltage	$V_{RX\_DIFFp\text{-}p}$	100	—	1200	mV	2
Loss of signal threshold	VL_{OS}	30	—	100	mV	
Input AC common mode voltage	$V_{CM\_ACp\text{-}p}$	—	—	100	mV	3
Receiver differential input impedance	Z_{RX_DIFF}	80	100	120	Ω	
Receiver common mode input impedance	Z_{RX_CM}	20	—	35	Ω	

Table 36. eTSEC IEEE 1588 AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	—	—	ns	2

Notes:
1. T_{RX_CLK} is the max clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for a description of TMR_CTRL registers.
2. It need to be at least two times of clock period of clock selected by TMR_CTRL[CKSEL]. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 3600, 280, and 56 ns, respectively.

8.5 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, RMII, RGMII, SGMII, and RTBI are specified in Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics."

8.5.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. Table 37 provide the DC electrical characteristics for MDIO and MDC.

Table 37. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	NV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	NV_{DD} = Min	2.10	NV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	NV_{DD} = Min	V_{SS}	0.50	V
Input high voltage	V_{IH}	—		2.0	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input high current	I_{IH}	NV_{DD} = Max	V_{IN}[1] = 2.1 V	—	40	μA
Input low current	I_{IL}	NV_{DD} = Max	V_{IN} = 0.5 V	–600	—	μA

This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8313E SerDes reference clock input's DC requirement.

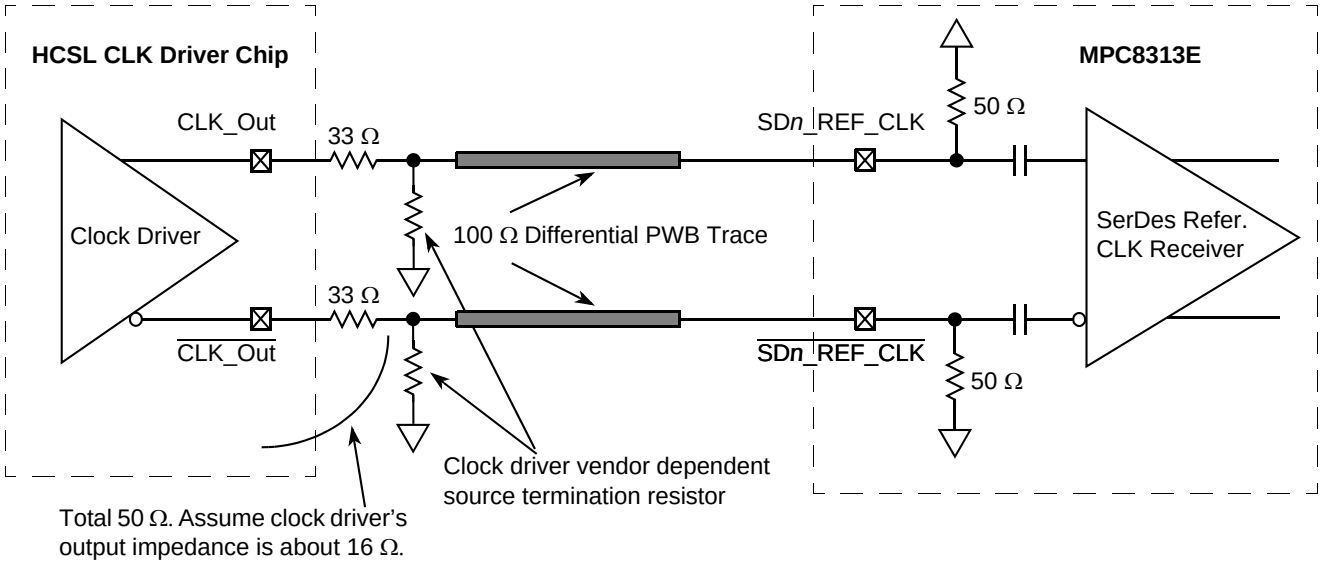


Figure 27. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8313E SerDes reference clock input's allowed range (100 to 400 mV), the AC-coupled connection scheme must be used. It assumes the LVDS output driver features a 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

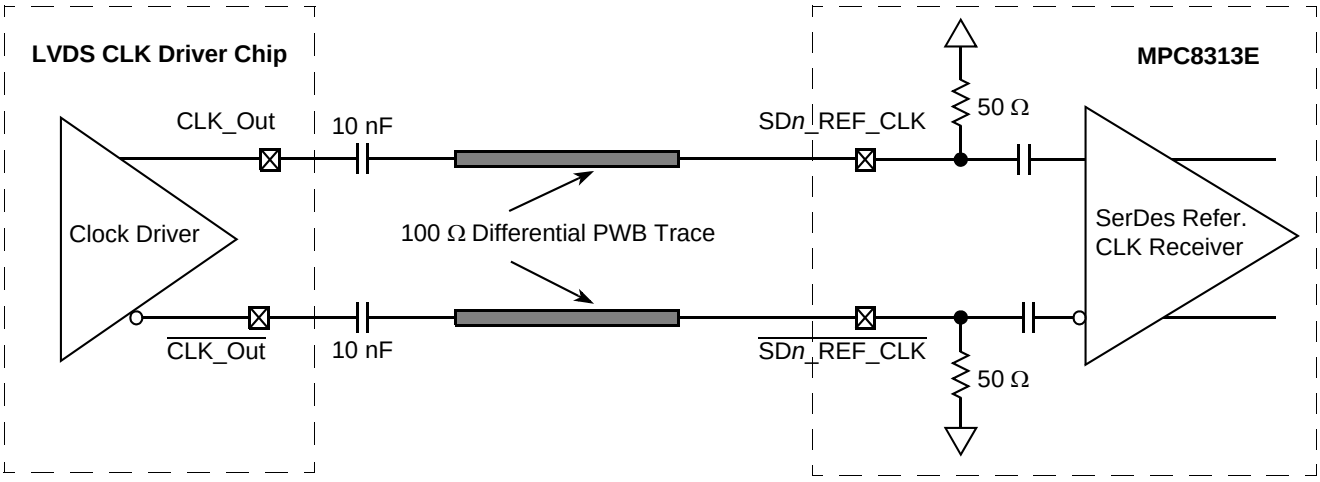


Figure 28. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the MPC8313E SerDes reference clock input's DC requirement, AC coupling has to be used. Figure 29

Figure 37 through Figure 40 show the local bus signals.

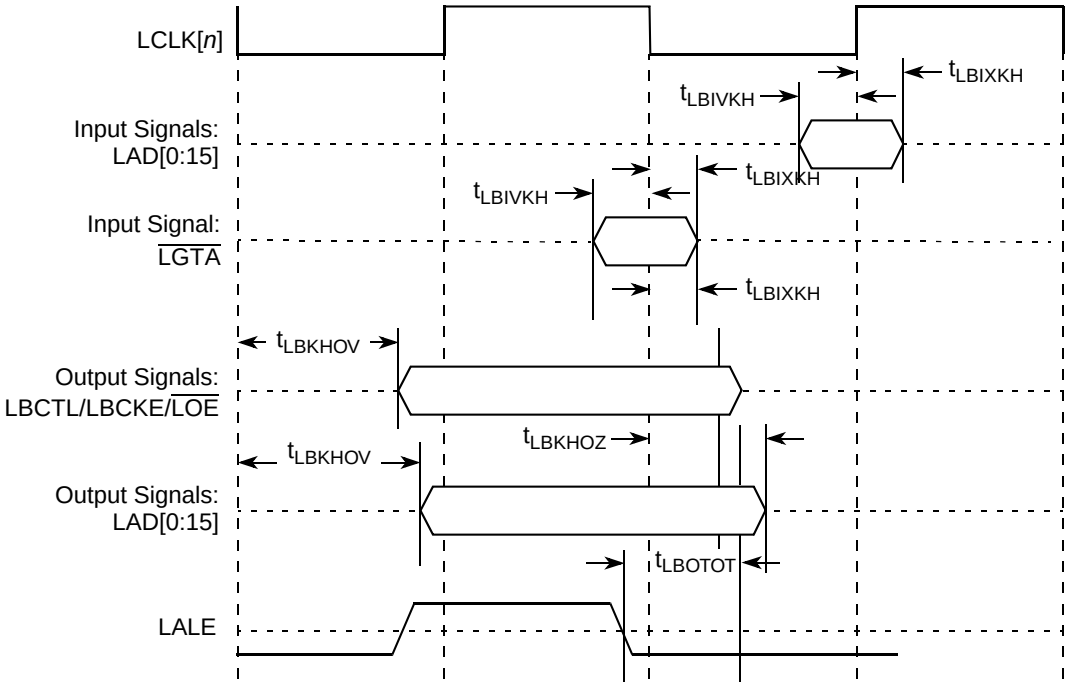


Figure 37. Local Bus Signals, Non-Special Signals Only

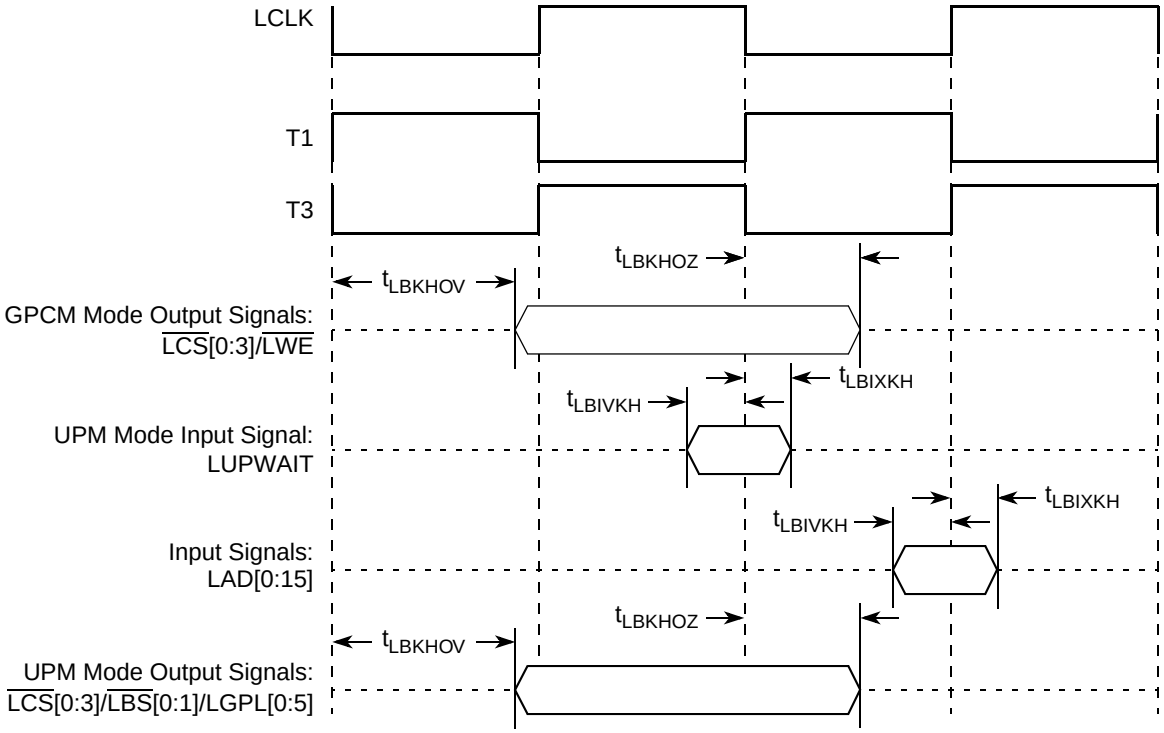


Figure 38. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2

13 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interface.

13.1 I^2C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interface.

Table 48. I^2C DC Electrical Characteristics

At recommended operating conditions with NV_{DD} of 3.3 V ± 0.3 V.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage level	V_{IH}	$0.7 \times NV_{DD}$	$NV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times NV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times NV_{DD}$	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	
Input current, ($0 V \le V_{IN} \le NV_{DD}$)	I_{IN}	—	± 5	μA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if NV_{DD} is switched off.

13.2 I^2C AC Electrical Specifications

This table provides the AC timing parameters for the I^2C interface.

Table 49. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 48).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns

Table 49. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 48).

Parameter	Symbol[1]	Min	Max	Unit
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0[2]	 — 0.9[3]	µs
Fall time of both SDA and SCL signals[5]	t_{I2CF}	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times NV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times NV_{DD}$	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The MPC8313E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5. The MPC8313E does not follow the *I²C-BUS Specifications, Version 2.1,* regarding the t_{I2CF} AC parameter.

This figure provides the AC test load for the I²C.

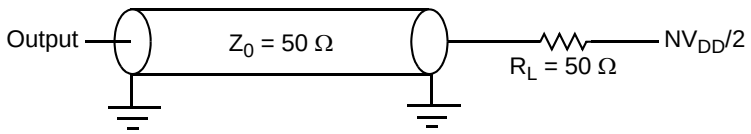


Figure 46. I²C AC Test Load

This figure shows the AC timing diagram for the I^2C bus.

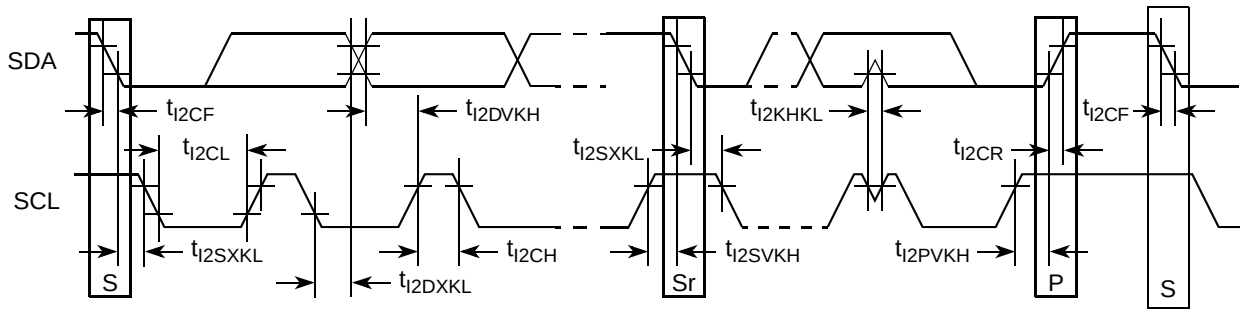


Figure 47. I^2C Bus AC Timing Diagram

14 PCI

This section describes the DC and AC electrical specifications for the PCI bus.

14.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface.

Table 50. PCI DC Electrical Characteristics[1]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	0.5 × NV_{DD}	NV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.5	0.3 × NV_{DD}	V
High-level output voltage	V_{OH}	NV_{DD} = min, I_{OH} = –100 µA	0.9 × NV_{DD}	—	V
Low-level output voltage	V_{OL}	NV_{DD} = min, I_{OL} = 100 µA	—	0.1 × NV_{DD}	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NV_{DD}	—	±5	µA

Note:
1. Note that the symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

14.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8313E is configured as a host or agent device.

This table shows the PCI AC timing specifications at 66 MHz.

Table 51. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2

This table provides the DC electrical characteristics for the GPIO when the GPIO pins are operating from a 2.5-V supply.

Table 56. GPIO (When Operating at 2.5 V) DC Electrical Characteristics[1]

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	NV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	NV_{DD} = min	2.00	NV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	NV_{DD} = min	V_{SS} – 0.3	0.40	V
Input high voltage	V_{IH}	—	NV_{DD} = min	1.7	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	NV_{DD} = min	–0.3	0.70	V
Input high current	I_{IH}	V_{IN} = NV_{DD}		—	10	μA
Input low current	I_{IL}	V_{IN} = V_{SS}		–15	—	μA

Note:

1. This specification only applies to GPIO pins that are operating from a 2.5-V supply. See Table 62 for the power supply listed for the individual GPIO signal

16.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 57. GPIO Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

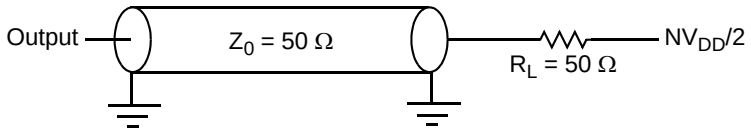


Figure 52. GPIO AC Test Load

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LA24	E23	O	LV_{DD}	11
LA25	D22	O	LV_{DD}	11
$\overline{\text{LCS0}}$	D23	O	LV_{DD}	10
$\overline{\text{LCS1}}$	J26	O	LV_{DD}	10
$\overline{\text{LCS2}}$	F22	O	LV_{DD}	10
$\overline{\text{LCS3}}$	D26	O	LV_{DD}	10
$\overline{\text{LWE0}}$/$\overline{\text{LFWE}}$	E24	O	LV_{DD}	10
$\overline{\text{LWE1}}$	H26	O	LV_{DD}	10
LBCTL	L22	O	LV_{DD}	10
LALE/M1LALE/M2LALE	E26	O	LV_{DD}	11
LGPL0/LFCLE	AA23	O	LV_{DD}	—
LGPL1/LFALE	AA24	O	LV_{DD}	—
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	AA25	O	LV_{DD}	10
LGPL3/$\overline{\text{LFWP}}$	AA26	O	LV_{DD}	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/$\overline{\text{LFRB}}$	Y22	I/O	LV_{DD}	2
LGPL5	E21	O	LV_{DD}	10
LCLK0	H22	O	LV_{DD}	11
LCLK1	G26	O	LV_{DD}	11
LA0/GPIO0/MSRCID0	AC24	I/O	LV_{DD}	—
LA1/GPIO1//MSRCID1	Y24	I/O	LV_{DD}	—
LA2/GPIO2//MSRCID2	Y26	I/O	LV_{DD}	—
LA3/GPIO3//MSRCID3	W22	I/O	LV_{DD}	—
LA4/GPIO4//MSRCID4	W24	I/O	LV_{DD}	—
LA5/GPIO5/MDVAL	W26	I/O	LV_{DD}	—
LA6/GPIO6	V22	I/O	LV_{DD}	—
LA7/GPIO7/TSEC_1588_TRIG2	V23	I/O	LV_{DD}	8
LA8/GPIO13/TSEC_1588_ALARM1	V24	I/O	LV_{DD}	8
LA9/GPIO14/TSEC_1588_PP3	V25	I/O	LV_{DD}	8
LA10/TSEC_1588_CLK	V26	O	LV_{DD}	8
LA11/TSEC_1588_GCLK	U22	O	LV_{DD}	8
LA12/TSEC_1588_PP1	AD24	O	LV_{DD}	8
LA13/TSEC_1588_PP2	L25	O	LV_{DD}	8

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_TRDY	AD13	I/O	NV_{DD}	5
PCI_IRDY	AC15	I/O	NV_{DD}	5
PCI_STOP	AF13	I/O	NV_{DD}	5
PCI_DEVSEL	AC14	I/O	NV_{DD}	5
PCI_IDSEL	AF20	I	NV_{DD}	—
PCI_SERR	AE15	I/O	NV_{DD}	5
PCI_PERR	AD15	I/O	NV_{DD}	5
PCI_REQ0	AB10	I/O	NV_{DD}	—
PCI_REQ1/CPCI_HS_ES	AD9	I	NV_{DD}	—
PCI_REQ2	AD8	I	NV_{DD}	—
PCI_GNT0	AC11	I/O	NV_{DD}	—
PCI_GNT1/CPCI_HS_LED	AE7	O	NV_{DD}	—
PCI_GNT2/CPCI_HS_ENUM	AD7	O	NV_{DD}	—
M66EN	AD21	I	NV_{DD}	—
PCI_CLK0	AF17	O	NV_{DD}	—
PCI_CLK1	AB16	O	NV_{DD}	—
PCI_CLK2	AF18	O	NV_{DD}	—
PCI_PME	AD22	I/O	NV_{DD}	5
ETSEC1/_USBULPI				
TSEC1_COL/USBDR_TXDRXD0	AD2	I/O	LV_{DDB}	—
TSEC1_CRS/USBDR_TXDRXD1	AC3	I/O	LV_{DDB}	—
TSEC1_GTX_CLK/USBDR_TXDRXD2	AF3	I/O	LV_{DDB}	3, 12
TSEC1_RX_CLK/USBDR_TXDRXD3	AE3	I/O	LV_{DDB}	—
TSEC1_RX_DV/USBDR_TXDRXD4	AD3	I/O	LV_{DDB}	—
TSEC1_RXD3/USBDR_TXDRXD5	AC6	I/O	LV_{DDB}	—
TSEC1_RXD2/USBDR_TXDRXD6	AF4	I/O	LV_{DDB}	—
TSEC1_RXD1/USBDR_TXDRXD7	AB6	I/O	LV_{DDB}	—
TSEC1_RXD0/USBDR_NXT/TSEC_1588_TRIG1	AB5	I	LV_{DDB}	—
TSEC1_RX_ER/USBDR_DIR/TSEC_1588_TRIG2	AD4	I	LV_{DDB}	—
TSEC1_TX_CLK/USBDR_CLK/TSEC_1588_CLK	AF5	I	LV_{DDB}	—
TSEC1_TXD3/TSEC_1588_GCLK	AE6	O	LV_{DDB}	—
TSEC1_TXD2/TSEC_1588_PP1	AC7	O	LV_{DDB}	—

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TSEC1_TXD1/TSEC_1588_PP2	AD6	O	LV_{DDB}	—
TSEC1_TXD0/USBDR_STP/TSEC_1588_PP3	AD5	O	LV_{DDB}	—
TSEC1_TX_EN/TSEC_1588_ALARM1	AB7	O	LV_{DDB}	—
TSEC1_TX_ER/TSEC_1588_ALARM2	AB8	O	LV_{DDB}	—
TSEC1_GTX_CLK125	AE1	I	LV_{DDB}	—
TSEC1_MDC/LB_POR_CFG_BOOT_ECC_DIS	AF6	O	NV_{DD}	9, 11
TSEC1_MDIO	AB9	I/O	NV_{DD}	—
ETSEC2				
TSEC2_COL/GTM1_TIN4/GTM2_TIN3/GPIO15	AB4	I/O	LV_{DDA}	—
TSEC2_CRS/$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$/GPIO16	AB3	I/O	LV_{DDA}	—
TSEC2_GTX_CLK/$\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$/GPIO17	AC1	I/O	LV_{DDA}	12
TSEC2_RX_CLK/GTM1_TIN2/GTM2_TIN1/GPIO18	AC2	I/O	LV_{DDA}	—
TSCE2_RX_DV/$\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$/GPIO19	AA3	I/O	LV_{DDA}	—
TSEC2_RXD3/GPIO20	Y5	I/O	LV_{DDA}	—
TSEC2_RXD2/GPIO21	AA4	I/O	LV_{DDA}	—
TSEC2_RXD1/GPIO22	AB2	I/O	LV_{DDA}	—
TSEC2_RXD0/GPIO23	AA5	I/O	LV_{DDA}	—
TSEC2_RX_ER/$\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$/GPIO24	AA2	I/O	LV_{DDA}	—
TSEC2_TX_CLK/GPIO25	AB1	I/O	LV_{DDA}	—
TSEC2_TXD3/CFG_RESET_SOURCE0	W3	I/O	LV_{DDA}	—
TSEC2_TXD2/CFG_RESET_SOURCE1	Y1	I/O	LV_{DDA}	—
TSEC2_TXD1/CFG_RESET_SOURCE2	W5	I/O	LV_{DDA}	—
TSEC2_TXD0/CFG_RESET_SOURCE3	Y3	I/O	LV_{DDA}	—
TSEC2_TX_EN/GPIO26	AA1	I/O	LV_{DDA}	—
TSEC2_TX_ER/GPIO27	W1	I/O	LV_{DDA}	—
SGMII PHY				
TXA	U3	O		—
$\overline{\text{TXA}}$	V3	O		—
RXA	U1	I		—
$\overline{\text{RXA}}$	V1	I		—
TXB	P4	O		—
$\overline{\text{TXB}}$	N4	O		—

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
V_{SS}	B1,B2,B8,B9,B16,B17,C1, C2,C3,C4,C5,C24,C25, C26,D3,D4,D12,D13,D20, D21,F8,F11,F13,F16,F17, F21,G2,G25,H2,H6,H21, H25,L4,L6,L11,L12,L13, L14,L15,L16,L21,L23,M4, M11,M12,M13,M14,M15, M16,M23,N6,N11,N12, N13,N14,N15,N16, N21,N23,P11,P12,P13, P14,P15,P16,P23,P25, R11,R12,R13,R14,R15, R16,R25,T6,T11,T12,T13, T14,T15,T16,T21,T25,U5, U6,U21,W4,W23,Y4,Y23, AA8,AA11,AA13,AA16, AA17,AA21,AC4,AC5, AC12,AC13,AC20,AC21, AD1,AE2,AE8,AE9,AE16, AE17,AF2	—	—	—
$XCOREV_{DD}$	T1,U2,V2	Core power for SerDes transceivers (1.0 V)	—	—
$XCOREV_{SS}$	P2,R2,T3	—	—	—
$XPADV_{DD}$	P5,U4	Pad power for SerDes transceivers (1.0 V)	—	—
$XPADV_{SS}$	P3,V4	—	—	—

Notes:
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NV_{DD}.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. This pin must always be tied to V_{SS}.
7. Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.
8. 1588 signals are available on these pins only in MPC8313 Rev 2.x or later.
9. LB_POR_CFG_BOOT_ECC_DIS is available only in MPC8313 Rev 2.x or later.
10. This pin has an internal pull-up.
11. This pin has an internal pull-down.
12. In MII mode, GTX_CLK should be pulled down by 300Ω to V_{SS}.

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICOE*n*] parameters select whether the PCI_SYNC_OUT is driven out on the PCI_CLK_OUT*n* signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the SYS_CLK_IN signal should be tied to VSS.

As shown in Figure 57, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbc_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{\text{PCI\_SYNC\_IN} \times (1 + \sim\overline{\text{CFG\_CLKIN\_DIV}})\} \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~$\overline{\text{CFG\_CLKIN\_DIV}}$) is the SYS_CLK_IN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*, for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + \text{RCWL[DDRCM]})$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbc_clk* frequency is determined by the following equation:

$$lbc\_clk = csb\_clk \times (1 + \text{RCWL[LBCM]})$$

Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the a LBC clock divider to create the external local bus clock outputs (LCLK[0:1]). The LBC clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 63 specifies which units have a configurable clock frequency.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal NV_{DD}, 105°C.

Table 71. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (Not Including PCI Output Clocks)	PCI Output Clocks (Including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
R_P	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
Differential	NA	NA	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_J = 105 °C.

22.7 Configuration Pin Muxing

The MPC8313E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{PORESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

22.8 Pull-Up Resistor Requirements

The MPC8313E requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C, and IPIC (integrated programmable interrupt controller).

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 61. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions because most have asynchronous behavior and spurious assertion, which give unpredictable results.

Refer to the *PCI 2.2 Specification*, for all pull-ups required for PCI.

22.9 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in IEEE 1149.1, but is provided on any Freescale devices that are built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, systems generally assert $\overline{\text{TRST}}$ during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ is not practical.

23.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the MPC8313E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 72. Part Numbering Nomenclature

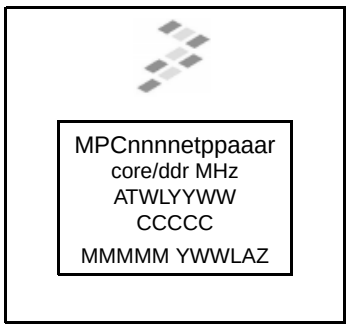
MPC	*nnnn*	*e*	*t*	*pp*	*aa*	*a*	*x*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range [3]**	**Package [1, 4]**	**e300 core Frequency [2]**	**DDR Frequency**	**Revision Level**
MPC	8313	Blank = Not included E = included	Blank = 0° to 105°C C= –40° to 105°C	ZQ = PB TEPBGAII VR = PB free TEPBGAII	AD = 266 MHz AF = 333 MHz AG = 400 MHz	D = 266 MHz F = 333 MHz	Blank = 1.0 A = 2.0 B = 2.1 C = 2.2

Note:

1. See Section 19, “Package and Pin Listings,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
3. Contact local Freescale office on availability of parts with °C temperature range.
4. ZQ package was available for Rev 1.0. For Rev 2.x, only VR package is available.

23.2 Part Marking

Parts are marked as shown in this figure.



TePBGA

Notes:
MPCnnnnetppaar is the orderable part number.
ATWLYYWW is the standard assembly, test, year, and work week codes.
CCCCC is the country code.
MMMMM is the mask number.

Figure 62. Part Marking for TEPBGAII Device

Table 73. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
1	3/2008	• In Table 63, added LBC_PM_REF_10 & LSRCID3 as muxed with USBDR_PCTL1 • In Table 63, added LSRCID2 as muxed with USBDR_PCTL0 • In Table 63, added LSRCID1 as muxed with USBDR_PWRFAULT • In Table 63, added LSRCID0 as muxed with USBDR_DRIVE_VBUS • In Table 63, moved T1, U2,& V2 from V_{DD} to XCOREVDD. • In Table 63, moved P2, R2, & T3 from V_{SS} to XCOREVSS. • In Table 63, moved P5, & U4 from V_{DD} to XPADVDD. • In Table 63, moved P3, & V4 from V_{SS} to XPADVSS. • In Table 63, removed “Double with pad” for AV_{DD1} and AV_{DD2} and moved AV_{DD1} and AV_{DD2} to Power and Ground Supplies section • In Table 63, added impedance control requirements for SD_IMP_CAL_TX (100 ohms to GND) and SD_IMP_CAL_RX (200 ohms to GND). • In Table 63, updated muxing in pinout to show new options for selecting IEEE 1588 functionality. Added footnote 8 • In Table 63, updated muxing in pinout to show new LBC ECC boot enable control muxed with eTSEC1_MDC • Added pin type information for power supplies. • Removed N1 and N3 from Vss section of Table 63. Added Therm0 and Therm1 (N1 and N3, respectively). Added note 7 to state: “Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.” • In Table 65 corrected maximum frequency of Local Bus Frequency from “33–66” to 66 MHz • In Table 65 corrected maximum frequency of PCI from “24–66” to 66 MHz • Added “which is determined by RCWLR[COREPLL],” to the note in Section 20.2, “Core PLL Configuration” about the VCO divider. • Added “(VCOD)” next to VCO divider column in Table 68. Added footnote stating that core_clk frequency must not exceed its maximum, so 2.5:1 and 3:1 *core_clk:csb_clk* ratios are invalid for certain *csb_clk* values. • In Table 69, notes were confusing. Added note 3 for VCO column, note 4 for CSB (*csb_clk*) column, note 5 for USB ref column, and note 6 to replace “Note 1”. Clarified note 4 to explain erratum eTSEC40. • In Table 69, updated note 6 to specify USB reference clock frequencies limited to 24 and 48 for rev. 2 silicon. • Replaced Table 71 “Thermal Resistance for TEPBGAII with Heat Sink in Open Flow”. • Removed last row of Table 19. • Removed 200 MHz rows from Table 21 and Table 5. • Changed VIH minimum spec from 2.0 to 2.1 for clock, PIC, JTAG, SPI, and reset pins in Table 9, Table 47, Table 54, Table 59, and Table 61. • Added Figure 4 showing the DDR input timing diagram. • In Table 19, removed “MDM” from the “MDQS-MDQ/MECC/MDM” text under the Parameter column for the tCISKEW parameter. MDM is an output signal and should be removed from the input AC timing spec table (tCISKEW). • Added “and power” to rows 2 and 3 in Table 10 • Added the sentence “Once both the power supplies...” and PORESET to Section 2.2, “Power Sequencing,” and Figure 3. • In Figure 35, corrected “USB0_CLK/USB1_CLK/DR_CLK” with “USBDR_CLK” • In Table 42, clarified that AC specs are for ULPI only.
0	6/2007	Initial release.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Document Number: MPC8313EEC
Rev. 4
11/2011