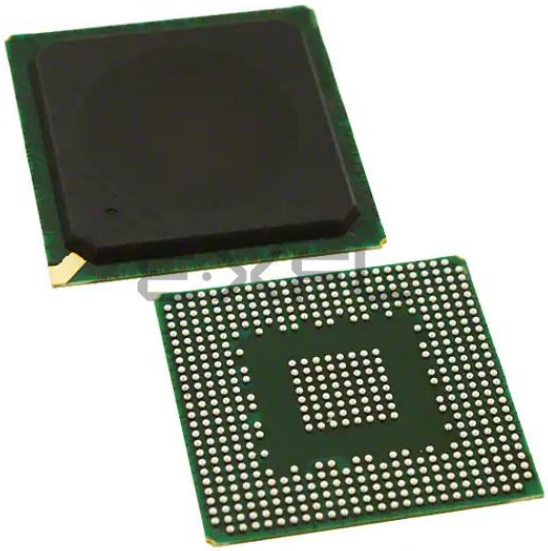


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	267MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8313czqaddb

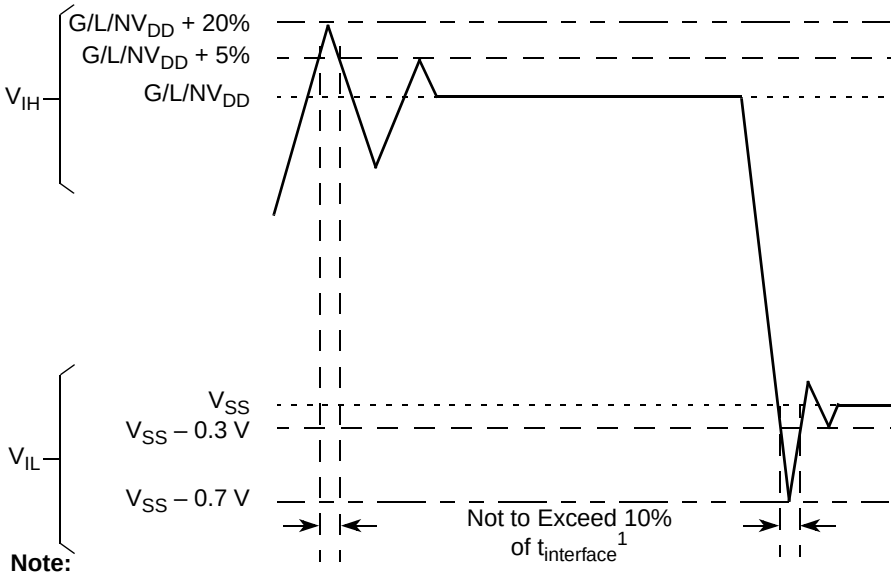
Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value[1]	Unit	Current Requirement

Note:

1. GV_{DD}, NV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. Some GPIO pins may operate from a 2.5-V supply when configured for other functions.
3. Min temperature is specified with T_A; Max temperature is specified with T_J.
4. All Power rails must be connected and power applied to the MPC8313 even if the IP interfaces are not used.
5. All I/O pins should be interfaced with peripherals operating at same voltage level.
6. This voltage is the input to the filter discussed in Section 22.2, "PLL Power Supply Filtering" and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter.

This figure shows the undershoot and overshoot voltages at the interfaces of the MPC8313E.



Note:

1. Note that $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/NV_{DD}/LV_{DD}

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	NV_{DD} = 3.3 V
PCI signals	25	
DDR signal	18	GV_{DD} = 2.5 V

3 Power Characteristics

The estimated typical power dissipation, not including I/O supply power, for this family of MPC8313E devices is shown in this table. Table 5 shows the estimated typical I/O power dissipation.

Table 4. MPC8313E Power Dissipation[1]

Core Frequency (MHz)	CSB Frequency (MHz)	Typical[2]	Maximum for Rev. 1.0 Silicon[3]	Maximum for Rev. 2.x or Later Silicon[3]	Unit
333	167	820	1020	1200	mW
400	133	820	1020	1200	mW

Note:

1. The values do not include I/O supply power or AV_{DD}, but do include core, USB PLL, and a portion of SerDes digital power (not including $XCOREV_{DD}$, $XPADV_{DD}$, or $SDAV_{DD}$, which all have dedicated power supplies for the SerDes PHY).
2. Typical power is based on a voltage of V_{DD} = 1.05 V and an artificial smoker test running at room temperature.
3. Maximum power is based on a voltage of V_{DD} = 1.05 V, a junction temperature of T_J = 105°C, and an artificial smoker test.

This table describes a typical scenario where blocks with the stated percentage of utilization and impedances consume the amount of power described.

Table 5. MPC8313E Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	NV_{DD} (3.3 V)	LV_{DDA}/ LV_{DDB} (3.3 V)	LV_{DDA}/ LV_{DDB} (2.5 V)	LV_{DD} (3.3 V)	Unit	Comments
DDR 1, 60% utilization, 50% read/write R_s = 22 Ω R_t = 50 Ω single pair of clock capacitive load: data = 8 pF, control address = 8 pF, clock = 8 pF	333 MHz, 32 bits	—	0.355	—	—	—	—	W	—
	266 MHz, 32 bits	—	0.323	—	—	—	—	W	—
DDR 2, 60% utilization, 50% read/write R_s = 22 Ω R_t = 75 Ω single pair of clock capacitive load: data = 8 pF, control address = 8 pF, clock = 8 pF	333 MHz, 32 bits	0.266	—	—	—	—	—	W	—
	266 MHz, 32 bits	0.246	—	—	—	—	—	W	—
PCI I/O load = 50 pF	33 MHz	—	—	0.120	—	—	—	W	—
	66 MHz	—	—	0.249	—	—	—	W	—
Local bus I/O load = 20 pF	66 MHz	—	—	—	—	—	0.056	W	—
	50 MHz	—	—	—	—	—	0.040	W	—
TSEC I/O load = 20 pF	MII, 25 MHz	—	—	—	0.008	—	—	W	Multiple by number of interface used
	RGMII, 125 MHz	—	—	—	0.078	0.044	—	W	

This table provides the input AC timing specifications for the DDR SDRAM when GV_{DD}(typ) = 2.5 V.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	—

This table provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions. with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ	t_{CISKEW}	—	—	ps	1, 2
333 MHz	—	–750	750	—	—
266 MHz	—	–750	750	—	—

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[*n*] and any corresponding bit that is captured with MDQS[*n*]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

This figure illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

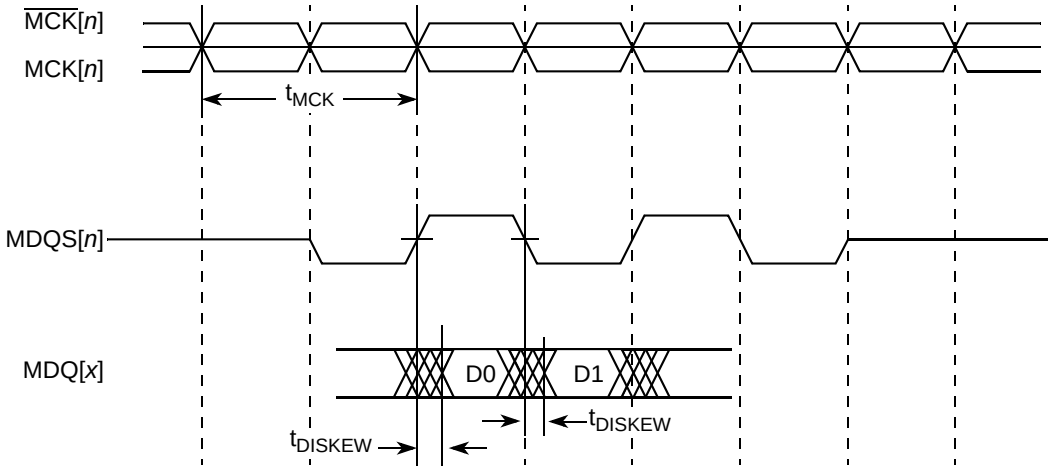


Figure 4. DDR Input Timing Diagram

8.3.2 AC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

This table lists the SGMII SerDes reference clock AC requirements. Note that SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Table 31. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit
t_{REF}	REFCLK cycle time	—	8	—	ns
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps

8.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 32 and Table 33 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX[*n*] and $\overline{\text{SD\_TX}}$[*n*]) as depicted in Figure 16.

Table 32. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$XCOREV_{DD}$	0.95	1.0	1.05	V	
Output high voltage	V_{OH}	—	—	$XCOREV_{DD\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-max}}/2$	mV	1
Output low voltage	V_{OL}	$XCOREV_{DD\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-max}}/2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	
Output differential voltage[2, 3]	$\lvert V_{OD}\rvert$	323	500	725	mV	Equalization setting: 1.0x
Output offset voltage	V_{OS}	425	500	575	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	
Mismatch in a pair	ΔR_O	—	—	10	%	
Change in V_{OD} between 0 and 1	$\Delta\lvert V_{OD}\rvert$	—	—	25	mV	
Change in V_{OS} between 0 and 1	ΔV_{OS}	—	—	25	mV	
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	

Notes:

1. This will not align to DC-coupled SGMII. $XCOREV_{DD\text{-}Typ}$ = 1.0 V.
2. $\lvert V_{OD}\rvert = \lvert V_{TXn} - V_{\overline{TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $XCOREV_{DD\text{-}Typ}$ = 1.0 V, no common mode offset variation (V_{OS} = 500 mV), SerDes transmitter is terminated with 100-Ω differential load between TX[*n*] and $\overline{\text{TX}}$[*n*].
4. V_{OS} is also referred to as output common mode voltage.

Table 33. SGMII DC Receiver Electrical Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Common mode input voltage	V_{CM}	—	$V_{xcorevss}$	—	V	4

Notes:
1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak to peak input differential voltage
3. $V_{CM\_ACp\text{-}p}$ is also referred to as peak to peak AC common mode voltage.
4. On-chip termination to $XCOREV_{SS}$.

8.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (TX[*n*] and $\overline{\text{TX}}$[*n*]) or at the receiver inputs (RX[*n*] and $\overline{\text{RX}}$[*n*]) as depicted in Figure 18, respectively.

8.3.4.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 34. SGMII Transmit AC Timing Specifications

At recommended operating conditions with $XCOREV_{DD}$ = 1.0 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter	JD	—	—	0.17	UI p-p	
Total jitter	JT	—	—	0.35	UI p-p	
Unit interval	UI	799.92	800	800.08	ps	1
V_{OD} fall time (80%–20%)	tfall	50	—	120	ps	
V_{OD} rise time (20%–80%)	t_{rise}	50	—	120	ps	

Note:
1. Each UI is 800 ps ± 100 ppm.

8.3.4.2 SGMII Receive AC Timing Specifications

This table provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 17 shows the SGMII receiver input compliance mask eye diagram.

Table 35. SGMII Receive AC Timing Specifications

At recommended operating conditions with $XCOREV_{DD}$ = 1.0 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter tolerance	JD	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal jitter tolerance	JSIN	0.1	—	—	UI p-p	1

The common mode voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, V_{cm_out} = (V_{TXn} + $V_{\overline{TXn}}$)/2 = (A + B)/2, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It's also referred as the DC offset in some occasion.

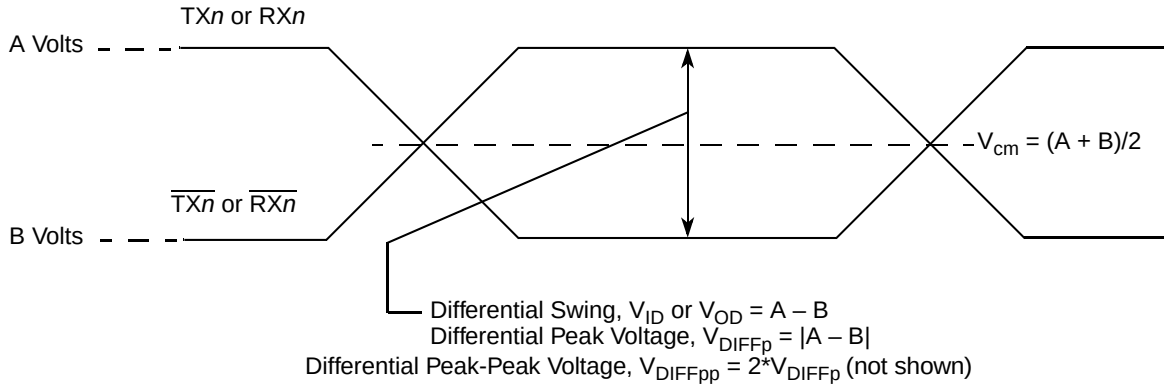


Figure 22. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

9.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks input is SD_REF_CLK and $\overline{SD\_REF\_CLK}$ for SGMII interface.

The following sections describe the SerDes reference clock requirements and some application information.

9.2.1 SerDes Reference Clock Receiver Characteristics

Figure 23 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $XCOREV_{DD}$ are specified in Table 1 and Table 2.
- SerDes reference clock receiver reference circuit structure:

9.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low-phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters for SGMII protocol.

Table 39. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD_SRDS1} or XV_{DD_SRDS2} = 1.0 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
Rising edge rate	Rise edge rate	1.0	4.0	V/ns	2, 3
Falling edge rate	Fall edge rate	1.0	4.0	V/ns	2, 3
Differential input high voltage	V_{IH}	+200	—	mV	2
Differential input low voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn\_REF\_CLK}}$) matching	Rise-fall matching	—	20	%	1, 4

Notes:
1. Measurement taken from single-ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 31.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point, where SD*n*_REF_CLK rising meets $\overline{\text{SD}n\text{\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK should be compared to the fall edge rate of $\overline{\text{SD}n\text{\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 32.

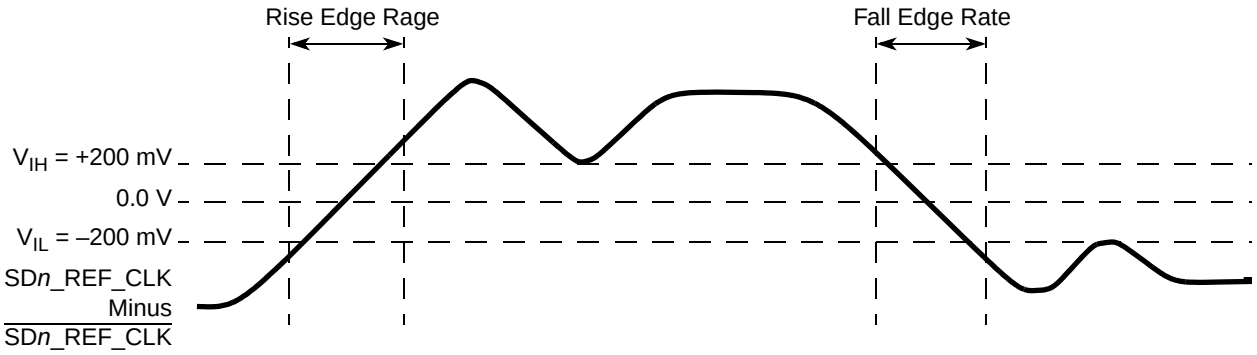


Figure 31. Differential Measurement Points for Rise and Fall Time

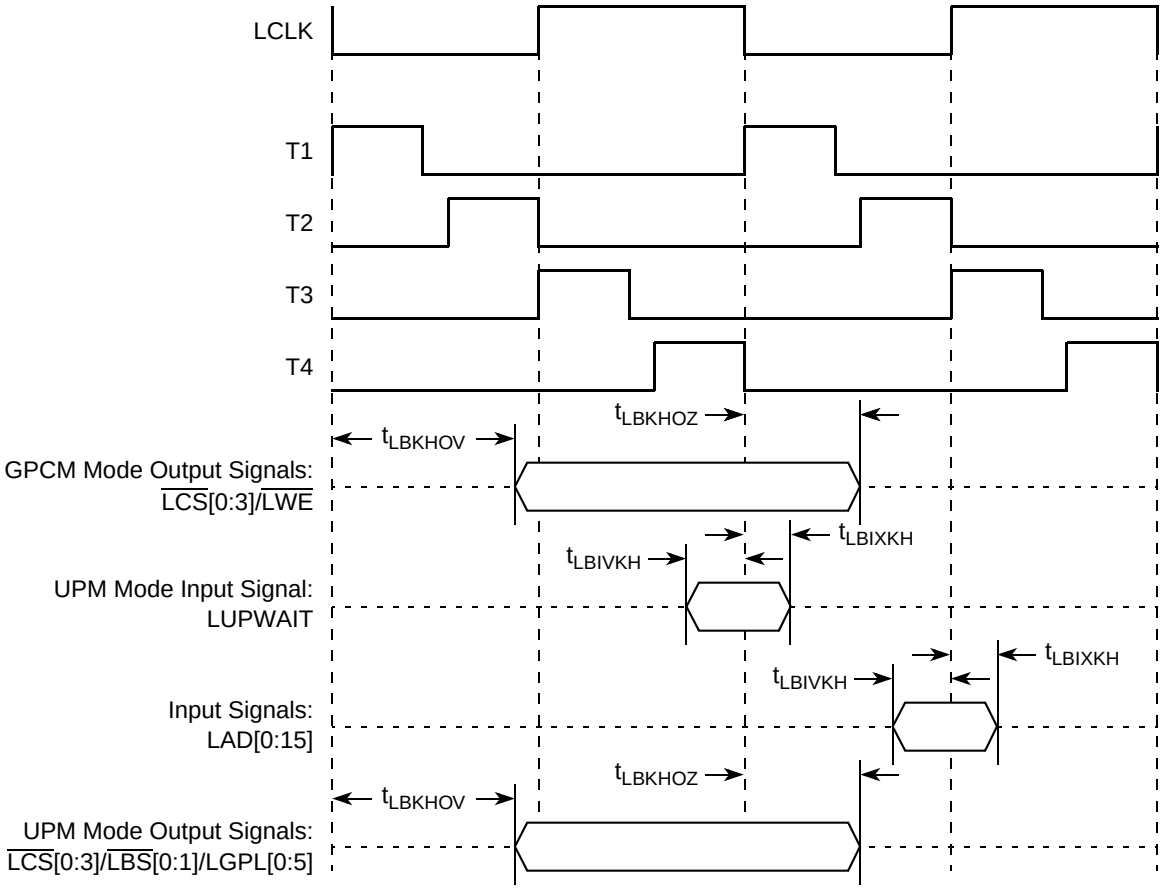


Figure 39. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

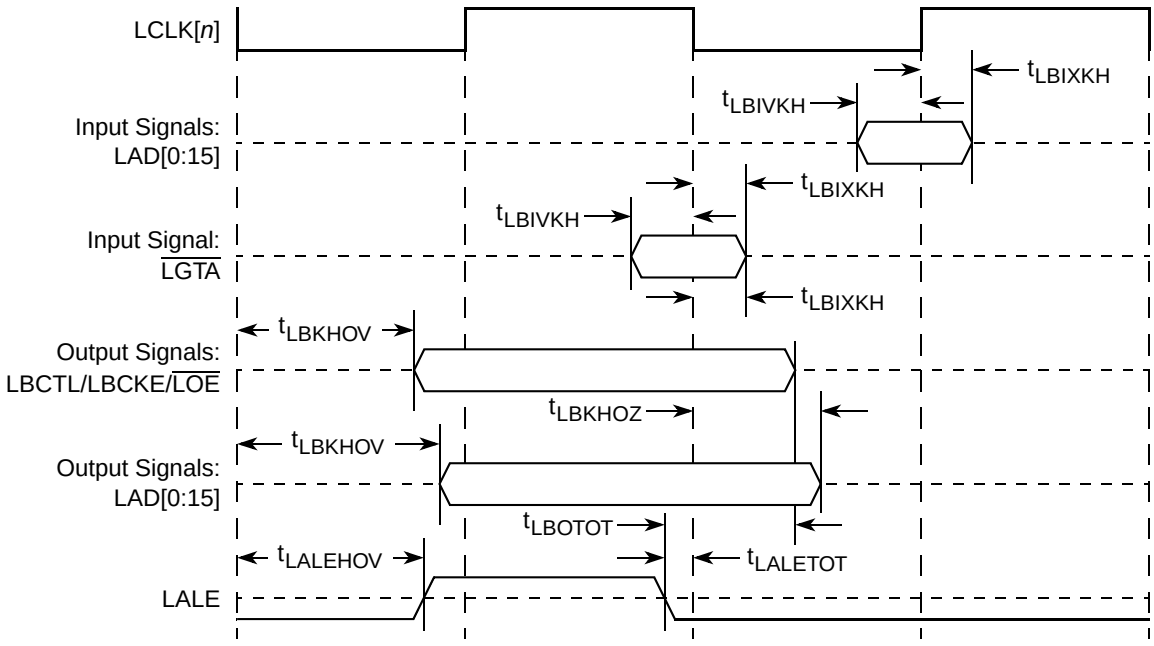


Figure 40. Local Bus Signals, LALE with Respect to LCLK

This figure shows the AC timing diagram for the I^2C bus.

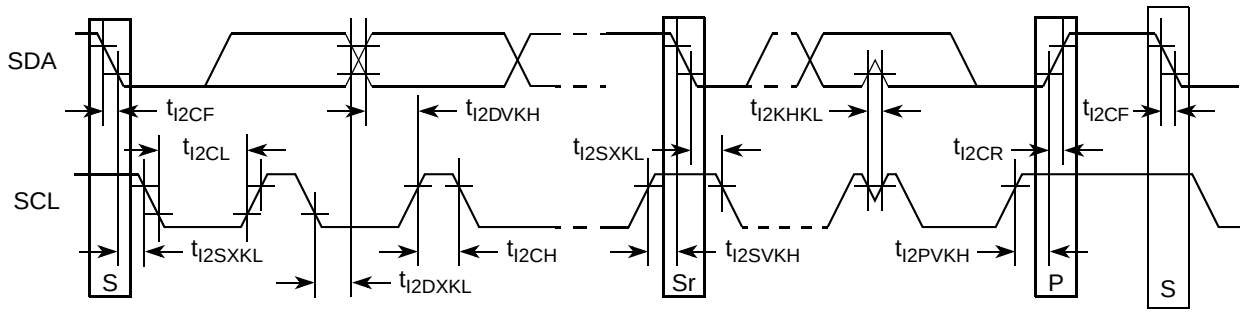


Figure 47. I^2C Bus AC Timing Diagram

14 PCI

This section describes the DC and AC electrical specifications for the PCI bus.

14.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface.

Table 50. PCI DC Electrical Characteristics[1]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	0.5 × NV_{DD}	NV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.5	0.3 × NV_{DD}	V
High-level output voltage	V_{OH}	NV_{DD} = min, I_{OH} = –100 µA	0.9 × NV_{DD}	—	V
Low-level output voltage	V_{OL}	NV_{DD} = min, I_{OL} = 100 µA	—	0.1 × NV_{DD}	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NV_{DD}	—	±5	µA

Note:
1. Note that the symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

14.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8313E is configured as a host or agent device.

This table shows the PCI AC timing specifications at 66 MHz.

Table 51. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2

15.2 Timers AC Timing Specifications

This table provides the Timers input and output AC timing specifications.

Table 54. Timers Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

This figure provides the AC test load for the Timers.

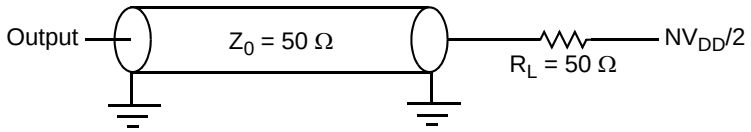


Figure 51. Timers AC Test Load

16 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

16.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO when the GPIO pins are operating from a 3.3-V supply.

Table 55. GPIO (When Operating at 3.3 V) DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	±5	μA

Note:
1. This specification only applies to GPIO pins that are operating from a 3.3-V supply. See Table 62 for the power supply listed for the individual GPIO signal.

This table provides the DC electrical characteristics for the GPIO when the GPIO pins are operating from a 2.5-V supply.

Table 56. GPIO (When Operating at 2.5 V) DC Electrical Characteristics[1]

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	NV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	NV_{DD} = min	2.00	NV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	NV_{DD} = min	V_{SS} – 0.3	0.40	V
Input high voltage	V_{IH}	—	NV_{DD} = min	1.7	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	NV_{DD} = min	–0.3	0.70	V
Input high current	I_{IH}	V_{IN} = NV_{DD}		—	10	μA
Input low current	I_{IL}	V_{IN} = V_{SS}		–15	—	μA

Note:

1. This specification only applies to GPIO pins that are operating from a 2.5-V supply. See Table 62 for the power supply listed for the individual GPIO signal

16.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 57. GPIO Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

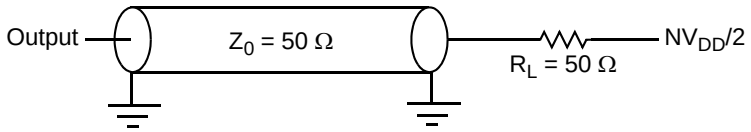


Figure 52. GPIO AC Test Load

Table 60. SPI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	±5	μA

18.2 SPI AC Timing Specifications

This table and provide the SPI input and output AC timing specifications.

Table 61. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs—master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Note:

1. Output specifications are measured from the 50% level of the rising edge of SYS_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

This figure provides the AC test load for the SPI.

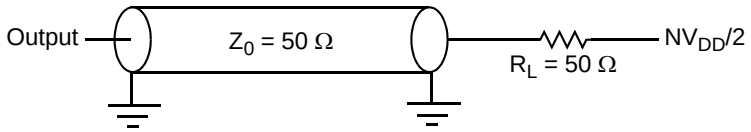


Figure 53. SPI AC Test Load

Figure 54 and Figure 55 represent the AC timing from Table 61. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TMS	E4	I	NV_{DD}	4
$\overline{\text{TRST}}$	E5	I	NV_{DD}	4
TEST				
TEST_MODE	F4	I	NV_{DD}	6
DEBUG				
$\overline{\text{QUIESCE}}$	F5	O	NV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	F2	I/O	NV_{DD}	1
$\overline{\text{PORESET}}$	F3	I	NV_{DD}	—
$\overline{\text{SRESET}}$	F1	I	NV_{DD}	—
Clocks				
SYS_CR_CLK_IN	U26	I	NV_{DD}	—
SYS_CR_CLK_OUT	U25	O	NV_{DD}	—
SYS_CLK_IN	U23	I	NV_{DD}	—
USB_CR_CLK_IN	T26	I	NV_{DD}	—
USB_CR_CLK_OUT	R26	O	NV_{DD}	—
USB_CLK_IN	T22	I	NV_{DD}	—
PCI_SYNC_OUT	U24	O	NV_{DD}	3
RTC_PIT_CLOCK	R22	I	NV_{DD}	—
PCI_SYNC_IN	T24	I	NV_{DD}	—
MISC				
THERM0	N1	I	NV_{DD}	7
THERM1	N3	I	NV_{DD}	7
PCI				
$\overline{\text{PCI\_INTA}}$	AF7	O	NV_{DD}	—
$\overline{\text{PCI\_RESET\_OUT}}$	AB11	O	NV_{DD}	—
PCI_AD0	AB20	I/O	NV_{DD}	—
PCI_AD1	AF23	I/O	NV_{DD}	—
PCI_AD2	AF22	I/O	NV_{DD}	—
PCI_AD3	AB19	I/O	NV_{DD}	—
PCI_AD4	AE22	I/O	NV_{DD}	—
PCI_AD5	AF21	I/O	NV_{DD}	—

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_AD6	AD19	I/O	NV_{DD}	—
PCI_AD7	AD20	I/O	NV_{DD}	—
PCI_AD8	AC18	I/O	NV_{DD}	—
PCI_AD9	AD18	I/O	NV_{DD}	—
PCI_AD10	AB18	I/O	NV_{DD}	—
PCI_AD11	AE19	I/O	NV_{DD}	—
PCI_AD12	AB17	I/O	NV_{DD}	—
PCI_AD13	AE18	I/O	NV_{DD}	—
PCI_AD14	AD17	I/O	NV_{DD}	—
PCI_AD15	AF19	I/O	NV_{DD}	—
PCI_AD16	AB14	I/O	NV_{DD}	—
PCI_AD17	AF15	I/O	NV_{DD}	—
PCI_AD18	AD14	I/O	NV_{DD}	—
PCI_AD19	AE14	I/O	NV_{DD}	—
PCI_AD20	AF12	I/O	NV_{DD}	—
PCI_AD21	AE11	I/O	NV_{DD}	—
PCI_AD22	AD12	I/O	NV_{DD}	—
PCI_AD23	AB13	I/O	NV_{DD}	—
PCI_AD24	AF9	I/O	NV_{DD}	—
PCI_AD25	AD11	I/O	NV_{DD}	—
PCI_AD26	AE10	I/O	NV_{DD}	—
PCI_AD27	AB12	I/O	NV_{DD}	—
PCI_AD28	AD10	I/O	NV_{DD}	—
PCI_AD29	AC10	I/O	NV_{DD}	—
PCI_AD30	AF10	I/O	NV_{DD}	—
PCI_AD31	AF8	I/O	NV_{DD}	—
PCI_C/$\overline{BE0}$	AC19	I/O	NV_{DD}	—
PCI_C/$\overline{BE1}$	AB15	I/O	NV_{DD}	—
PCI_C/$\overline{BE2}$	AF14	I/O	NV_{DD}	—
PCI_C/$\overline{BE3}$	AF11	I/O	NV_{DD}	—
PCI_PAR	AD16	I/O	NV_{DD}	—
$\overline{PCI\_FRAME}$	AF16	I/O	NV_{DD}	5

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICOE*n*] parameters select whether the PCI_SYNC_OUT is driven out on the PCI_CLK_OUT*n* signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the SYS_CLK_IN signal should be tied to VSS.

As shown in Figure 57, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbc_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{\text{PCI\_SYNC\_IN} \times (1 + \sim\overline{\text{CFG\_CLKIN\_DIV}})\} \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~$\overline{\text{CFG\_CLKIN\_DIV}}$) is the SYS_CLK_IN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*, for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + \text{RCWL[DDRCM]})$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbc_clk* frequency is determined by the following equation:

$$lbc\_clk = csb\_clk \times (1 + \text{RCWL[LBCM]})$$

Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the a LBC clock divider to create the external local bus clock outputs (LCLK[0:1]). The LBC clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 63 specifies which units have a configurable clock frequency.

Table 65. System PLL Multiplication Factors (continued)

RCWL[SPMF]	System PLL Multiplication Factor
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

Note:
1. If RCWL[DDRCM] and RCWL[LBCM] are both cleared, the system PLL VCO frequency = (CSB frequency) × (System PLL VCO Divider).
2. If either RCWL[DDRCM] or RCWL[LBCM] are set, the system PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO Divider).
3. The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz

As described in Section 20, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (SYS_CLK_IN or PCI_SYNC_IN) and the internal coherent system bus clock (*csb_clk*). This table shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN/PCI_SYNC_IN ratios.

Table 66. CSB Frequency Options

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* :Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			24	25	33.33	66.67
			csb_clk Frequency (MHz)			
High	0010	2:1				133
High	0011	3:1			100	
High	0100	4:1		100	133	
High	0101	5:1	120	125	167	
High	0110	6:1	144	150		
Low	0010	2:1				133
Low	0011	3:1			100	
Low	0100	4:11		100	133	
Low	0101	5:1	120	125	167	
Low	0110	6:1	144	150		

1 CFG_CLKIN_DIV select the ratio between SYS_CLK_IN and PCI_SYNC_OUT.

2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

20.3 Example Clock Frequency Combinations

This table shows several possible frequency combinations that can be selected based on the indicated input reference frequencies, with RCWLR[LBCM] = 0 and RCWLR[DDRCM] =1, such that the LBC operates with a frequency equal to the frequency of *csb_clk* and the DDR controller operates at twice the frequency of *csb_clk*.

Table 68. System Clock Frequencies

						LBC(lbc_clk)				e300 Core(core_clk)				
SYS_ CLK_IN/ PCI_CLK	SPMF[1]	VCOD[2]	VCO[3]	CSB (*csb_clk*)[4]	DDR (ddr_clk)	/2	/4	/8	USB ref[5]	× 1	× 1.5	× 2	× 2.5	× 3
25.0	6	2	600.0	150.0	300.0	—	37.5	18.8	Note[6]	150.0	225	300	375	—
25.0	5	2	500.0	125.0	250.0	62.5	31.25	15.6	Note 6	125.0	188	250	313	375
33.3	5	2	666.0	166.5	333.0	—	41.63	20.8	Note 6	166.5	250	333	—	—
33.3	4	2	532.8	133.2	266.4	66.6	33.3	16.7	Note 6	133.2	200	266	333	400
48.0	3	2	576.0	144.0	288.0	—	36	18.0	48.0	144.0	216	288	360	—
66.7	2	2	533.4	133.3	266.7	66.7	33.34	16.7	Note 6	133.3	200	267	333	400

Note:

1. System PLL multiplication factor.
2. System PLL VCO divider.
3. When considering operating frequencies, the valid core VCO operating range of 400–800 MHz must not be violated.
4. Due to erratum eTSEC40, *csb_clk* frequencies of less than 133 MHz do not support gigabit Ethernet data rates. The core frequency must be 333 MHz for gigabit Ethernet operation. This erratum will be fixed in revision 2 silicon.
5. Frequency of USB PLL input reference.
6. USB reference clock must be supplied from a separate source as it must be 24 or 48 MHz, the USB reference must be supplied from a separate external source using USB_CLK_IN.

21 Thermal

This section describes the thermal specifications of the MPC8313E.

21.1 Thermal Characteristics

This table provides the package thermal characteristics for the 516, 27 × 27 mm TEPBGAII.

Table 69. Package Thermal Characteristics for TEPBGAII

Characteristic	Board Type	Symbol	TEPBGA II	Unit	Note
Junction-to-ambient natural convection	Single layer board (1s)	$R_{\theta JA}$	25	°C/W	1, 2
Junction-to-ambient natural convection	Four layer board (2s2p)	$R_{\theta JA}$	18	°C/W	1, 2, 3
Junction-to-ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	20	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	15	°C/W	1, 3
Junction-to-board	—	$R_{\theta JB}$	10	°C/W	4

Table 69. Package Thermal Characteristics for TEPBGAII (continued)

Characteristic	Board Type	Symbol	TEPBGA II	Unit	Note
Junction-to-case	—	$R_{\theta JC}$	8	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	7	°C/W	6

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

21.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

21.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)
T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

21.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 70. Thermal Resistance for TEPBGAII with Heat Sink in Open Flow

Heat Sink Assuming Thermal Grease	Airflow	Thermal Resistance (°C/W)
Wakefield 53 × 53 × 2.5 mm pin fin	Natural convection	13.0
	0.5 m/s	10.6
	1 m/s	9.7
	2 m/s	9.2
	4 m/s	8.9
Aavid 35 × 31 × 23 mm pin fin	Natural convection	14.4
	0.5 m/s	11.3
	1 m/s	10.5
	2 m/s	9.9
	4 m/s	9.4
Aavid 30 × 30 × 9.4 mm pin fin	Natural convection	16.5
	0.5 m/s	13.5
	1 m/s	12.1
	2 m/s	10.9
	4 m/s	10.0
Aavid 43 × 41 × 16.5 mm pin fin	Natural convection	14.5
	0.5 m/s	11.7
	1 m/s	10.5
	2 m/s	9.7
	4 m/s	9.2

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in Table 70. More detailed thermal models can be made available on request.

- Output signals on the SerDes interface are fed from the $XPADV_{DD}$ power plane. Input signals and sensitive transceiver analog circuits are on the $XCOREV_{DD}$ supply.
- Power: $XPADV_{DD}$ consumes less than 300 mW; $XCOREV_{DD}$ + $SDAV_{DD}$ consumes less than 750 mW.

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8313E system, and the MPC8313E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA}, and LV_{DDB} pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA}, LV_{DDB}, and VSS power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA}, and LV_{DDB} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100 to 330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power ($XCOREV_{DD}$ and $XPADV_{DD}$) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor from each SerDes supply ($XCOREV_{DD}$ and $XPADV_{DD}$) to the board ground plane on each side of the device. This should be done for all SerDes supplies.