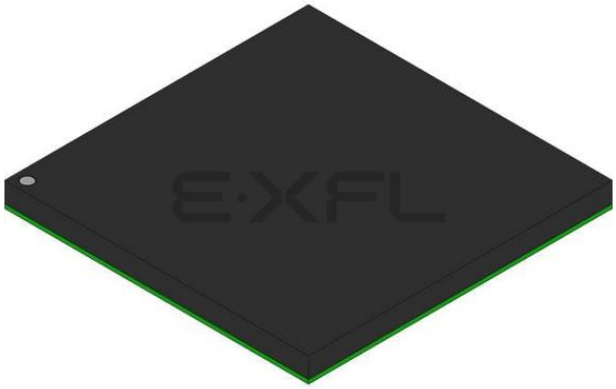

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8313czqaff

- Full and half-duplex Ethernet support (1000 Mbps supports only full-duplex):
  - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE 802.1 virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision
  - CRC generation and verification of inbound/outbound packets
  - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
  - Exact match on primary and virtual 48-bit unicast addresses
    - VRRP and HSRP support for seamless router fail-over
  - Up to 16 exact-match MAC addresses supported
  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status

1.8 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model supports 5 external and 34 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

1.9 Power Management Controller (PMC)

The MPC8313E power management controller includes the following features:

- Provides power management when the device is used in both host and agent modes
- Supports PCI power management 1.2 D0, D1, D2, D3hot, and D3cold states
- On-chip split power supply controlled through external power switch for minimum standby power
- Support for PME generation in PCI agent mode, PME detection in PCI host mode
- Supports wake-up from Ethernet (Magic Packet), USB, GPIO, and PCI (PME input as host)

1.10 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the MPC8313E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

1.11 DMA Controller, Dual I^2C, DUART, Local Bus Controller, and Timers

The MPC8313E provides an integrated four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Supports misaligned transfers

There are two I^2C controllers. These synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. The 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8313E local bus controller (LBC) port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The three user programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM or UPM controller. The FCM provides a glueless interface to parallel-bus NAND Flash E2PROM devices. The FCM contains three basic configuration register groups—BR*n*, OR*n*, and FMR. Both may exist in the same system. The local bus can operate at up to 66 MHz.

The MPC8313E system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8313E. The MPC8313E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value[1]	Unit	Current Requirement
Core supply voltage	V_{DD}	1.0 V ± 50 mV	V	469 mA
Internal core logic constant power	V_{DDC}	1.0 V ± 50 mV	V	377 mA
SerDes internal digital power	$XCOREV_{DD}$	1.0	V	170 mA
SerDes internal digital ground	$XCOREV_{SS}$	0.0	V	—
SerDes I/O digital power	$XPADV_{DD}$	1.0	V	10 mA
SerDes I/O digital ground	$XPADV_{SS}$	0.0	V	—
SerDes analog power for PLL	$SDAV_{DD}$	1.0 V ± 50 mV	V	10 mA
SerDes analog ground for PLL	$SDAV_{SS}$	0.0	V	—
Dedicated 3.3 V analog power for USB PLL	USB_PLL_PWR3	3.3 V ± 300 mV	V	2–3 mA
Dedicated 1.0 V analog power for USB PLL	USB_PLL_PWR1	1.0 V ± 50 mV	V	2–3 mA
Dedicated analog ground for USB PLL	USB_PLL_GND	0.0	V	—
Dedicated USB power for USB bias circuit	USB_VDDA_BIAS	3.3 V ± 300 mV	V	4–5 mA
Dedicated USB ground for USB bias circuit	USB_VSSA_BIAS	0.0	V	—
Dedicated power for USB transceiver	USB_VDDA	3.3 V ± 300 mV	V	75 mA
Dedicated ground for USB transceiver	USB_VSSA	0.0	V	—
Analog power for e300 core APLL	AV_{DD1} [6]	1.0 V ± 50 mV	V	2–3 mA
Analog power for system APLL	AV_{DD2} [6]	1.0 V ± 50 mV	V	2–3 mA
DDR1 DRAM I/O voltage (333 MHz, 32-bit operation)	GV_{DD}	2.5 V ± 125 mV	V	131 mA
DDR2 DRAM I/O voltage (333 MHz, 32-bit operation)	GV_{DD}	1.8 V ± 80 mV	V	140 mA
Differential reference voltage for DDR controller	MV_{REF}	1/2 DDR supply ($0.49 \times GV_{DD}$ to $0.51 \times GV_{DD}$)	V	—
Standard I/O voltage	NV_{DD}	3.3 V ± 300 mV[2]	V	74 mA
eTSEC2 I/O supply	LV_{DDA}	2.5 V ± 125 mV/ 3.3 V ± 300 mV	V	22 mA
eTSEC1/USB DR I/O supply	LV_{DDB}	2.5 V ± 125 mV/ 3.3 V ± 300 mV	V	44 mA
Supply for eLBC IOs	LV_{DD}	3.3 V ± 300 mV	V	16 mA
Analog and digital ground	V_{SS}	0.0	V	—
Junction temperature range	T_A/T_J [3]	0 to 105	°C	

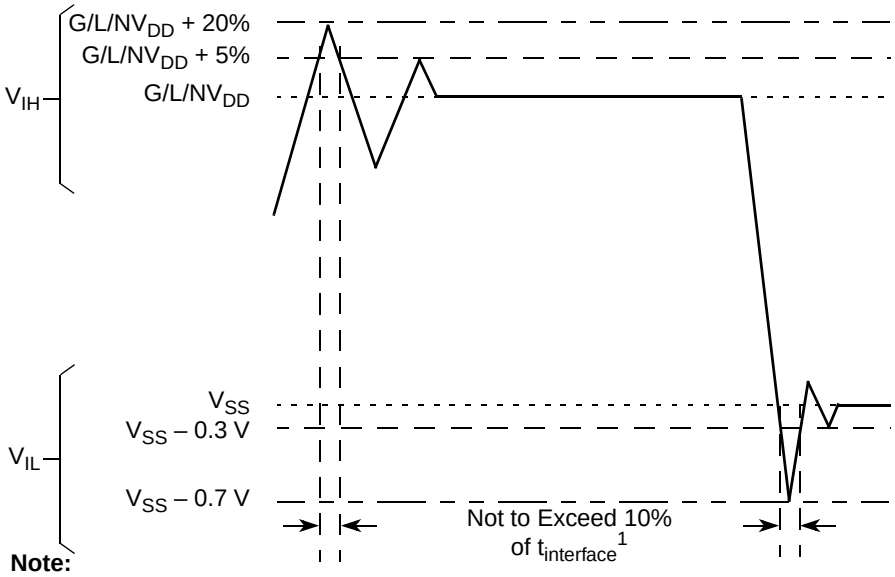
Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value[1]	Unit	Current Requirement

Note:

1. GV_{DD}, NV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. Some GPIO pins may operate from a 2.5-V supply when configured for other functions.
3. Min temperature is specified with T_A; Max temperature is specified with T_J.
4. All Power rails must be connected and power applied to the MPC8313 even if the IP interfaces are not used.
5. All I/O pins should be interfaced with peripherals operating at same voltage level.
6. This voltage is the input to the filter discussed in Section 22.2, "PLL Power Supply Filtering" and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter.

This figure shows the undershoot and overshoot voltages at the interfaces of the MPC8313E.



Note:

1. Note that $t_{interface}$ refers to the clock period associated with the bus clock interface.

Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/NV_{DD}/LV_{DD}

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	NV_{DD} = 3.3 V
PCI signals	25	
DDR signal	18	GV_{DD} = 2.5 V

Table 5. MPC8313E Typical I/O Power Dissipation (continued)

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	NV_{DD} (3.3 V)	LV_{DDA}/ LV_{DDB} (3.3 V)	LV_{DDA}/ LV_{DDB} (2.5 V)	LV_{DD} (3.3 V)	Unit	Comments
USBDR controller load = 20 pF	60 MHz	—	—	—	0.078	—	—	W	—
Other I/O	—	—	—	0.015	—	—	—	W	—

This table shows the estimated core power dissipation of the MPC8313E while transitioning into the D3 warm low-power state.

Table 6. MPC8313E Low-Power Modes Power Dissipation[1]

333-MHz Core, 167-MHz CSB[2]	Rev. 1.0[3]	Rev. 2.x or Later[3]	Unit
D3 warm	400	425	mW

Note:

1. All interfaces are enabled. For further power savings, disable the clocks to unused blocks.
2. The interfaces are run at the following frequencies: DDR: 333 MHz, eLBC 83 MHz, PCI 33 MHz, eTSEC1 and TSEC2: 167 MHz, SEC: 167 MHz, USB: 167 MHz. See the SCCR register for more information.
3. This is maximum power in D3 Warm based on a voltage of 1.05 V and a junction temperature of 105°C.

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8313E.

4.1 DC Electrical Characteristics

This table provides the system clock input (SYS_CLK_IN/PCI_SYNC_IN) DC timing specifications for the MPC8313E.

Table 7. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	NV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
SYS_CLK_IN input current	$0 V \le V_{IN} \le NV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0 V \le V_{IN} \le 0.5 V$ or $NV_{DD} – 0.5 V \le V_{IN} \le NV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0.5 V \le V_{IN} \le NV_{DD} – 0.5 V$	I_{IN}	—	±50	μA

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Note
Output leakage current	I_{OZ}	–9.9	–9.9	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Note:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 16. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM when GV_{DD}(typ) = 1.8 V.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	—

This figure shows the MII receive AC timing diagram.

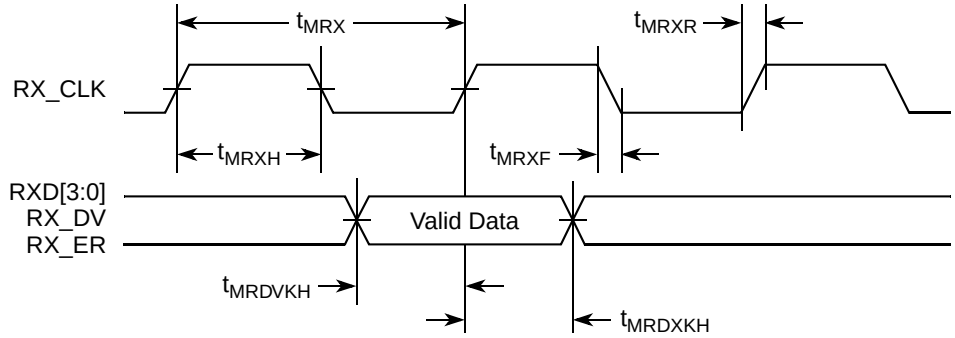


Figure 10. MII Receive AC Timing Diagram RMII AC Timing Specifications

8.2.1.3 RMII Transmit AC Timing Specifications

This table provides the RMII transmit AC timing specifications.

Table 28. RMII Transmit AC Timing Specifications

At recommended operating conditions with NV_{DD} of 3.3 V ± 0.3 V.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	10	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

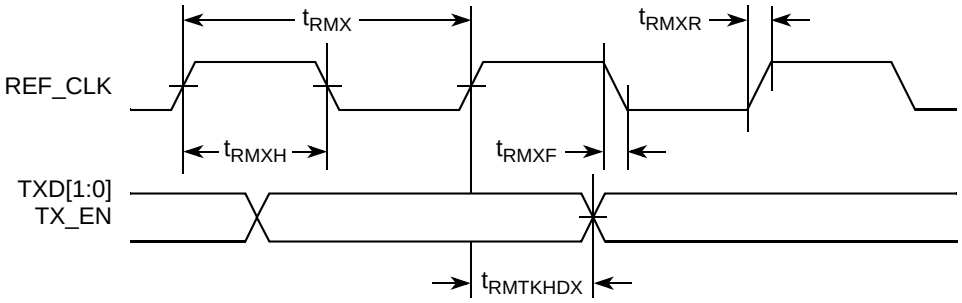


Figure 11. RMII Transmit AC Timing Diagram

Table 35. SGMII Receive AC Timing Specifications (continued)

At recommended operating conditions with $XCOREV_{DD}$ = 1.0 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Total jitter tolerance	JT	0.65	—	—	UI p-p	1
Bit error ratio	BER	—	—	10^{-12}		
Unit interval	UI	799.92	800	800.08	ps	2
AC coupling capacitor	C_{TX}	5	—	200	nF	3

Notes:
1. Measured at receiver.
2. Each UI is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.

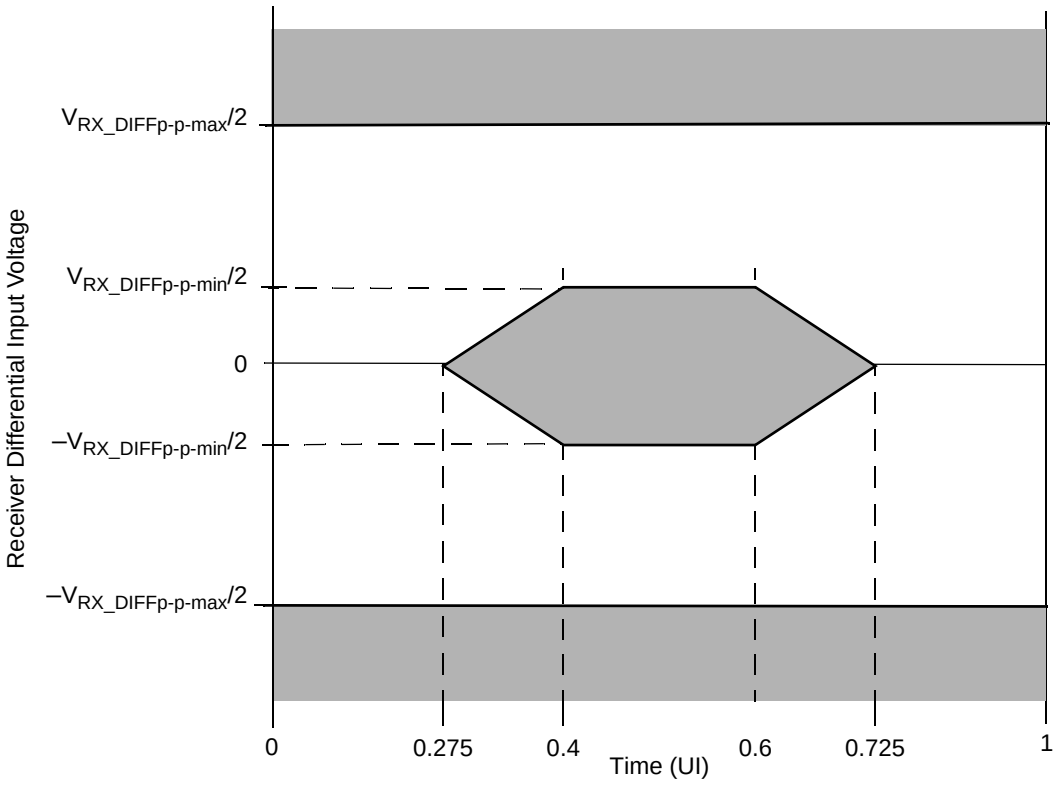


Figure 17. SGMII Receiver Input Compliance Mask

Table 37. MII Management DC Electrical Characteristics When Powered at 3.3 V (continued)

Note:
1. Note that the symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

8.5.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 38. MII Management AC Timing Specifications

At recommended operating conditions with NV_{DD} is 3.3 V ± 0.3V

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO delay	t_{MDKHDX}	10	—	170	ns	
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	
MDC fall time	t_{MDHF}	—	—	10	ns	

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)

This figure shows the MII management AC timing diagram.

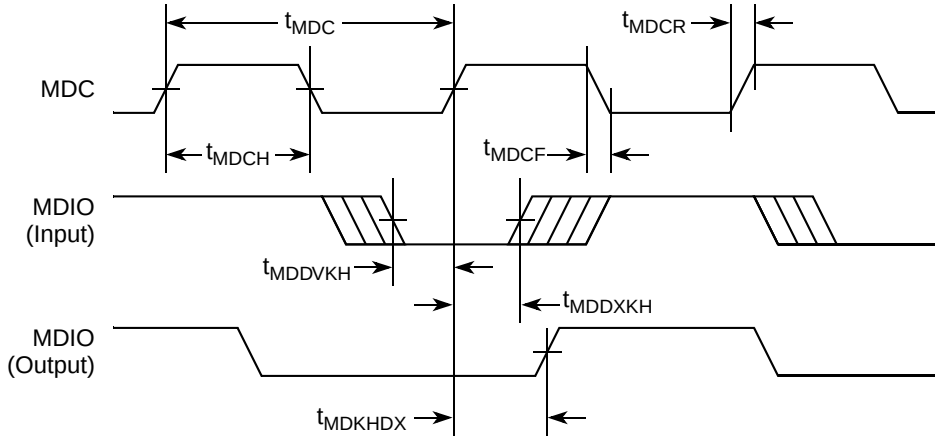


Figure 21. MII Management Interface Timing Diagram

of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

— For external DC-coupled connection, as described in Section 9.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 24 shows the SerDes reference clock input requirement for the DC-coupled connection scheme.

— For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to $XCOREV_{SS}$. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage ($XCOREV_{SS}$). Figure 25 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- Single-ended mode

— The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-to-peak (from V_{min} to V_{max}) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.

— The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 26 shows the SerDes reference clock input requirement for the single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC coupled externally. For the best noise performance, the reference of the clock could be DC or AC coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

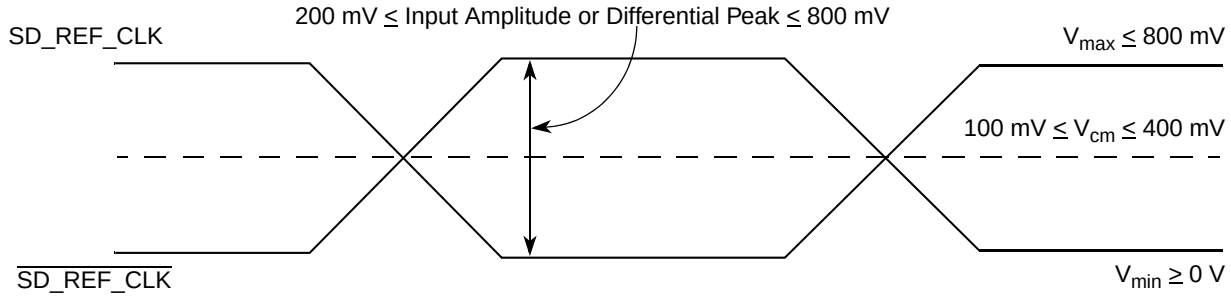


Figure 24. Differential Reference Clock Input DC Requirements (External DC-Coupled)

11 Enhanced Local Bus

This section describes the DC and AC electrical specifications for the local bus interface.

11.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface.

Table 44. Local Bus DC Electrical Characteristics at 3.3 V

Parameter	Symbol	Min	Max	Unit
High-level input voltage for Rev 1.0	V_{IH}	2.0	LV_{DD} + 0.3	V
High-level input voltage for Rev 2.x or later	V_{IH}	2.1	LV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current, (V_{IN}[1] = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	±5	μA
High-level output voltage, (LV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	LV_{DD} – 0.2	—	V
Low-level output voltage, (LV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.2	V

Note: The parameters stated in above table are valid for all revisions unless explicitly mentioned.

11.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface.

Table 45. Local Bus General Timing Parameters

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
LALE output rise to LCLK negative edge	$t_{LALEHOV}$	—	3.0	ns	
LALE output fall to LCLK negative edge	$t_{LALETOT1}$	–1.5	—	ns	5
LALE output fall to LCLK negative edge	$t_{LALETOT2}$	–5.0	—	ns	6
LALE output fall to LCLK negative edge	$t_{LALETOT3}$	–4.5	—	ns	7
Local bus clock to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD	t_{LBKHOZ}	—	4	ns	8

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_AD6	AD19	I/O	NV_{DD}	—
PCI_AD7	AD20	I/O	NV_{DD}	—
PCI_AD8	AC18	I/O	NV_{DD}	—
PCI_AD9	AD18	I/O	NV_{DD}	—
PCI_AD10	AB18	I/O	NV_{DD}	—
PCI_AD11	AE19	I/O	NV_{DD}	—
PCI_AD12	AB17	I/O	NV_{DD}	—
PCI_AD13	AE18	I/O	NV_{DD}	—
PCI_AD14	AD17	I/O	NV_{DD}	—
PCI_AD15	AF19	I/O	NV_{DD}	—
PCI_AD16	AB14	I/O	NV_{DD}	—
PCI_AD17	AF15	I/O	NV_{DD}	—
PCI_AD18	AD14	I/O	NV_{DD}	—
PCI_AD19	AE14	I/O	NV_{DD}	—
PCI_AD20	AF12	I/O	NV_{DD}	—
PCI_AD21	AE11	I/O	NV_{DD}	—
PCI_AD22	AD12	I/O	NV_{DD}	—
PCI_AD23	AB13	I/O	NV_{DD}	—
PCI_AD24	AF9	I/O	NV_{DD}	—
PCI_AD25	AD11	I/O	NV_{DD}	—
PCI_AD26	AE10	I/O	NV_{DD}	—
PCI_AD27	AB12	I/O	NV_{DD}	—
PCI_AD28	AD10	I/O	NV_{DD}	—
PCI_AD29	AC10	I/O	NV_{DD}	—
PCI_AD30	AF10	I/O	NV_{DD}	—
PCI_AD31	AF8	I/O	NV_{DD}	—
PCI_C/$\overline{BE0}$	AC19	I/O	NV_{DD}	—
PCI_C/$\overline{BE1}$	AB15	I/O	NV_{DD}	—
PCI_C/$\overline{BE2}$	AF14	I/O	NV_{DD}	—
PCI_C/$\overline{BE3}$	AF11	I/O	NV_{DD}	—
PCI_PAR	AD16	I/O	NV_{DD}	—
$\overline{PCI\_FRAME}$	AF16	I/O	NV_{DD}	5

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_TRDY	AD13	I/O	NV_{DD}	5
PCI_IRDY	AC15	I/O	NV_{DD}	5
PCI_STOP	AF13	I/O	NV_{DD}	5
PCI_DEVSEL	AC14	I/O	NV_{DD}	5
PCI_IDSEL	AF20	I	NV_{DD}	—
PCI_SERR	AE15	I/O	NV_{DD}	5
PCI_PERR	AD15	I/O	NV_{DD}	5
PCI_REQ0	AB10	I/O	NV_{DD}	—
PCI_REQ1/CPCI_HS_ES	AD9	I	NV_{DD}	—
PCI_REQ2	AD8	I	NV_{DD}	—
PCI_GNT0	AC11	I/O	NV_{DD}	—
PCI_GNT1/CPCI_HS_LED	AE7	O	NV_{DD}	—
PCI_GNT2/CPCI_HS_ENUM	AD7	O	NV_{DD}	—
M66EN	AD21	I	NV_{DD}	—
PCI_CLK0	AF17	O	NV_{DD}	—
PCI_CLK1	AB16	O	NV_{DD}	—
PCI_CLK2	AF18	O	NV_{DD}	—
PCI_PME	AD22	I/O	NV_{DD}	5
ETSEC1/_USBULPI				
TSEC1_COL/USBDR_TXDRXD0	AD2	I/O	LV_{DDB}	—
TSEC1_CRS/USBDR_TXDRXD1	AC3	I/O	LV_{DDB}	—
TSEC1_GTX_CLK/USBDR_TXDRXD2	AF3	I/O	LV_{DDB}	3, 12
TSEC1_RX_CLK/USBDR_TXDRXD3	AE3	I/O	LV_{DDB}	—
TSEC1_RX_DV/USBDR_TXDRXD4	AD3	I/O	LV_{DDB}	—
TSEC1_RXD3/USBDR_TXDRXD5	AC6	I/O	LV_{DDB}	—
TSEC1_RXD2/USBDR_TXDRXD6	AF4	I/O	LV_{DDB}	—
TSEC1_RXD1/USBDR_TXDRXD7	AB6	I/O	LV_{DDB}	—
TSEC1_RXD0/USBDR_NXT/TSEC_1588_TRIG1	AB5	I	LV_{DDB}	—
TSEC1_RX_ER/USBDR_DIR/TSEC_1588_TRIG2	AD4	I	LV_{DDB}	—
TSEC1_TX_CLK/USBDR_CLK/TSEC_1588_CLK	AF5	I	LV_{DDB}	—
TSEC1_TXD3/TSEC_1588_GCLK	AE6	O	LV_{DDB}	—
TSEC1_TXD2/TSEC_1588_PP1	AC7	O	LV_{DDB}	—

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TSEC1_TXD1/TSEC_1588_PP2	AD6	O	LV_{DDB}	—
TSEC1_TXD0/USBDR_STP/TSEC_1588_PP3	AD5	O	LV_{DDB}	—
TSEC1_TX_EN/TSEC_1588_ALARM1	AB7	O	LV_{DDB}	—
TSEC1_TX_ER/TSEC_1588_ALARM2	AB8	O	LV_{DDB}	—
TSEC1_GTX_CLK125	AE1	I	LV_{DDB}	—
TSEC1_MDC/LB_POR_CFG_BOOT_ECC_DIS	AF6	O	NV_{DD}	9, 11
TSEC1_MDIO	AB9	I/O	NV_{DD}	—
ETSEC2				
TSEC2_COL/GTM1_TIN4/GTM2_TIN3/GPIO15	AB4	I/O	LV_{DDA}	—
TSEC2_CRS/$\overline{\text{GTM1\_TGATE4}}$/$\overline{\text{GTM2\_TGATE3}}$/GPIO16	AB3	I/O	LV_{DDA}	—
TSEC2_GTX_CLK/$\overline{\text{GTM1\_TOUT4}}$/$\overline{\text{GTM2\_TOUT3}}$/GPIO17	AC1	I/O	LV_{DDA}	12
TSEC2_RX_CLK/GTM1_TIN2/GTM2_TIN1/GPIO18	AC2	I/O	LV_{DDA}	—
TSCE2_RX_DV/$\overline{\text{GTM1\_TGATE2}}$/$\overline{\text{GTM2\_TGATE1}}$/GPIO19	AA3	I/O	LV_{DDA}	—
TSEC2_RXD3/GPIO20	Y5	I/O	LV_{DDA}	—
TSEC2_RXD2/GPIO21	AA4	I/O	LV_{DDA}	—
TSEC2_RXD1/GPIO22	AB2	I/O	LV_{DDA}	—
TSEC2_RXD0/GPIO23	AA5	I/O	LV_{DDA}	—
TSEC2_RX_ER/$\overline{\text{GTM1\_TOUT2}}$/$\overline{\text{GTM2\_TOUT1}}$/GPIO24	AA2	I/O	LV_{DDA}	—
TSEC2_TX_CLK/GPIO25	AB1	I/O	LV_{DDA}	—
TSEC2_TXD3/CFG_RESET_SOURCE0	W3	I/O	LV_{DDA}	—
TSEC2_TXD2/CFG_RESET_SOURCE1	Y1	I/O	LV_{DDA}	—
TSEC2_TXD1/CFG_RESET_SOURCE2	W5	I/O	LV_{DDA}	—
TSEC2_TXD0/CFG_RESET_SOURCE3	Y3	I/O	LV_{DDA}	—
TSEC2_TX_EN/GPIO26	AA1	I/O	LV_{DDA}	—
TSEC2_TX_ER/GPIO27	W1	I/O	LV_{DDA}	—
SGMII PHY				
TXA	U3	O		—
$\overline{\text{TXA}}$	V3	O		—
RXA	U1	I		—
$\overline{\text{RXA}}$	V1	I		—
TXB	P4	O		—
$\overline{\text{TXB}}$	N4	O		—

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
RXB	R1	I		—
$\overline{\text{RXB}}$	P1	I		—
SD_IMP_CAL_RX	V5	I		200 Ω ± 10% to GND
$\overline{\text{SD\_REF\_CLK}}$	T5	I		—
SD_REF_CLK	T4	I		—
SD_PLL_TPD	T2	O		—
SD_IMP_CAL_TX	N5	I		100 Ω ± 10% to GND
SDAVDD	R5	I/O		—
SD_PLL_TPA_ANA	R4	O		—
SDAVSS	R3	I/O		—
USB PHY				
USB_DP	P26	I/O		—
USB_DM	N26	I/O		—
USB_VBUS	P24	I/O		—
USB_TPA	L26	I/O		—
USB_RBIAS	M24	I/O		—
USB_PLL_PWR3	M26	I/O		—
USB_PLL_GND	N24	I/O		—
USB_PLL_PWR1	N25	I/O		—
USB_VSSA_BIAS	M25	I/O		—
USB_VDDA_BIAS	M22	I/O		—
USB_VSSA	N22	I/O		—
USB_VDDA	P22	I/O		—
GTM/USB				
USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2/LSRCID0	AD23	I/O	NV_{DD}	—
USBDR_PWRFAULT/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$/ LSRCID1	AE23	I/O	NV_{DD}	—
USBDR_PCTL0/$\overline{\text{GTM1\_TOUT1}}$/LSRCID2	AC22	O	NV_{DD}	—
USBDR_PCTL1/LBC_PM_REF_10/LSRCID3	AB21	O	NV_{DD}	—

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 70. Thermal Resistance for TEPBGAII with Heat Sink in Open Flow

Heat Sink Assuming Thermal Grease	Airflow	Thermal Resistance (°C/W)
Wakefield 53 × 53 × 2.5 mm pin fin	Natural convection	13.0
	0.5 m/s	10.6
	1 m/s	9.7
	2 m/s	9.2
	4 m/s	8.9
Aavid 35 × 31 × 23 mm pin fin	Natural convection	14.4
	0.5 m/s	11.3
	1 m/s	10.5
	2 m/s	9.9
	4 m/s	9.4
Aavid 30 × 30 × 9.4 mm pin fin	Natural convection	16.5
	0.5 m/s	13.5
	1 m/s	12.1
	2 m/s	10.9
	4 m/s	10.0
Aavid 43 × 41 × 16.5 mm pin fin	Natural convection	14.5
	0.5 m/s	11.7
	1 m/s	10.5
	2 m/s	9.7
	4 m/s	9.2

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in Table 70. More detailed thermal models can be made available on request.

21.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

21.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction to case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)
T_C = case temperature of the package
$R_{\theta JC}$ = junction-to-case thermal resistance
P_D = power dissipation

22 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8313E SYS_CLK_IN

22.1 System Clocking

The MPC8313E includes three PLLs.

1. The platform PLL (AV_{DD2}) generates the platform clock from the externally supplied SYS_CLK_IN input in PCI host mode or SYS_CLK_IN/PCI_SYNC_IN in PCI agent mode. The frequency ratio between the platform and SYS_CLK_IN is selected using the platform PLL ratio configuration bits as described in Section 20.1, “System PLL Configuration.”
2. The e300 core PLL (AV_{DD1}) generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 20.2, “Core PLL Configuration.”
3. There is a PLL for the SerDes block.

- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

22.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA}, or LV_{DDB} as required. Unused active high inputs should be connected to V_{SS}. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA}, LV_{DDB}, and V_{SS} pins of the device.

22.6 Output Buffer DC Impedance

The MPC8313E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to NV_{DD} or V_{SS}. Then, the value of each resistor is varied until the pad voltage is $NV_{DD}/2$ (see Figure 60). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $NV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

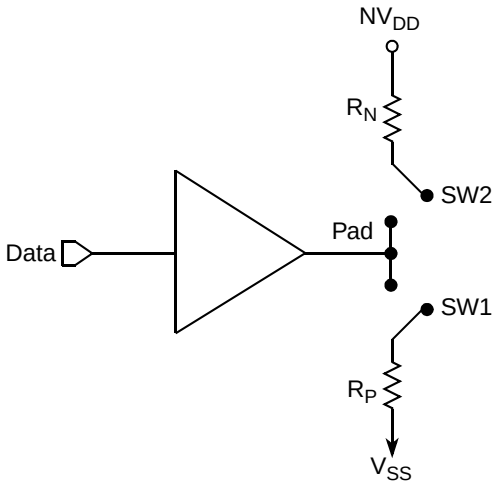


Figure 60. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal NV_{DD}, 105°C.

Table 71. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (Not Including PCI Output Clocks)	PCI Output Clocks (Including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
R_P	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
Differential	NA	NA	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_J = 105 °C.

22.7 Configuration Pin Muxing

The MPC8313E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{PORESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

22.8 Pull-Up Resistor Requirements

The MPC8313E requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C, and IPIC (integrated programmable interrupt controller).

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 61. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions because most have asynchronous behavior and spurious assertion, which give unpredictable results.

Refer to the *PCI 2.2 Specification*, for all pull-ups required for PCI.

22.9 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in IEEE 1149.1, but is provided on any Freescale devices that are built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, systems generally assert $\overline{\text{TRST}}$ during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ is not practical.

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Document Number: MPC8313EEC
Rev. 4
11/2011