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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8313czqagdc

1.6 USB Dual-Role Controller

The MPC8313E USB controller includes the following features:

- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Compatible with *Universal Serial Bus Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
 - Supports one upstream facing port
 - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
 - Supports USB root hub with one downstream-facing port
 - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI + low pin interface (ULPI) or on-chip USB 2.0 full-speed/high-speed PHY

1.7 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8313E eTSECs include the following features:

- Two RGMII/SGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3®, 802.3u®, 802.3x®, 802.3z®, 802.3au®, and 802.3ab®
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status
- Three-speed support (10/100/1000 Mbps)
- On-chip high-speed serial interface to external SGMII PHY interface
- Support for IEEE Std 1588™
- Support for two full-duplex FIFO interface modes
- Multiple PHY interface configuration
- TCP/IP acceleration and QoS features available
- IP v4 and IP v6 header recognition on receive
- IP v4 header checksum verification and generation
- TCP and UDP checksum verification and generation
- Per-packet configurable acceleration
- Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2®, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
- Transmission from up to eight physical queues.
- Reception to up to eight physical queues

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings¹

Characteristic		Symbol	Max Value	Unit	Note
Core supply voltage		V_{DD}	−0.3 to 1.26	V	—
PLL supply voltage		AV_{DD}	−0.3 to 1.26	V	—
Core power supply for SerDes transceivers		$XCOREV_{DD}$	−0.3 to 1.26	V	—
Pad power supply for SerDes transceivers		$XPADV_{DD}$	−0.3 to 1.26	V	—
DDR and DDR2 DRAM I/O voltage		GV_{DD}	−0.3 to 2.75 −0.3 to 1.98	V	—
PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage		NV_{DD}/LV_{DD}	−0.3 to 3.6	V	—
eTSEC, USB		LV_{DDA}/LV_{ddb}	−0.3 to 3.6	V	—
Input voltage	DDR DRAM signals	MV_{IN}	−0.3 to ($GV_{DD} + 0.3$)	V	2, 5
	DDR DRAM reference	MV_{REF}	−0.3 to ($GV_{DD} + 0.3$)	V	2, 5
	Enhanced three-speed Ethernet signals	LV_{IN}	−0.3 to ($LV_{DDA} + 0.3$) or −0.3 to ($LV_{ddb} + 0.3$)	V	4, 5
	Local bus, DUART, SYS_CLK_IN, system control, and power management, I ² C, and JTAG signals	NV_{IN}	−0.3 to ($NV_{DD} + 0.3$)	V	3, 5
	PCI	NV_{IN}	−0.3 to ($NV_{DD} + 0.3$)	V	6
Storage temperature range		T_{STG}	−55 to 150	°C	—

Notes:

- Functional and tested operating conditions are given in [Table 2](#). Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** NV_{IN} must not exceed NV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** LV_{IN} must not exceed LV_{DDA}/LV_{ddb} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the MPC8313E. Note that the values in this table are the recommended and tested operating conditions. If a particular block is given a voltage falling within the range in the Recommended Value column, the MPC8313E is capable of delivering the amount of current listed in the Current Requirement column; this is the maximum current possible. Proper device operation outside of these conditions is not guaranteed.

Table 3. Output Drive Capability (continued)

Driver Type	Output Impedance (Ω)	Supply Voltage
DDR2 signal	18	$GV_{DD} = 1.8\text{ V}$
DUART, system control, I ² C, JTAG, SPI	42	$NV_{DD} = 3.3\text{ V}$
GPIO signals	42	$NV_{DD} = 3.3\text{ V}$
eTSEC signals	42	$LV_{DDA}, LV_{ddb} = 2.5/3.3\text{ V}$
USB signals	42	$LV_{ddb} = 2.5/3.3\text{ V}$

2.2 Power Sequencing

The MPC8313E does not require the core supply voltage (V_{DD} and V_{DDC}) and I/O supply voltages (GV_{DD} , LV_{DD} , and NV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD} and V_{DDC}) before the I/O voltage (GV_{DD} , LV_{DD} , and NV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating $\overline{\text{PORESET}}$.

Note that there is no specific power down sequence requirement for the MPC8313E. I/O voltage supplies (GV_{DD} , LV_{DD} , and NV_{DD}) do not have any ordering requirements with respect to one another.

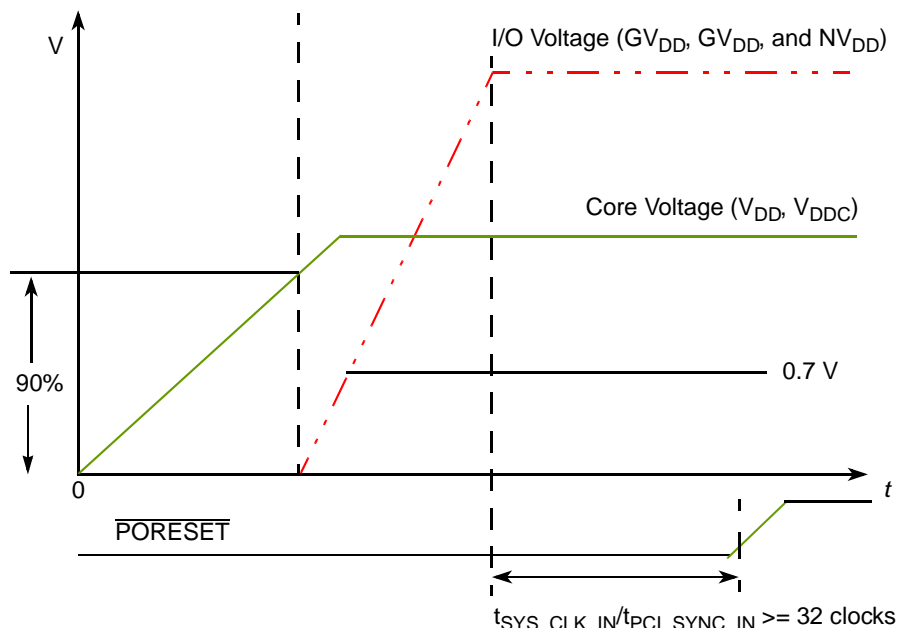


Figure 3. Power-Up Sequencing Example

3 Power Characteristics

The estimated typical power dissipation, not including I/O supply power, for this family of MPC8313E devices is shown in this table. [Table 5](#) shows the estimated typical I/O power dissipation.

Table 4. MPC8313E Power Dissipation¹

Core Frequency (MHz)	CSB Frequency (MHz)	Typical ²	Maximum for Rev. 1.0 Silicon ³	Maximum for Rev. 2.x or Later Silicon ³	Unit
333	167	820	1020	1200	mW
400	133	820	1020	1200	mW

Note:

1. The values do not include I/O supply power or AV_{DD} , but do include core, USB PLL, and a portion of SerDes digital power (not including $XCOREV_{DD}$, $XPADV_{DD}$, or $SDAV_{DD}$, which all have dedicated power supplies for the SerDes PHY).
2. Typical power is based on a voltage of $V_{DD} = 1.05$ V and an artificial smoker test running at room temperature.
3. Maximum power is based on a voltage of $V_{DD} = 1.05$ V, a junction temperature of $T_J = 105^\circ\text{C}$, and an artificial smoker test.

This table describes a typical scenario where blocks with the stated percentage of utilization and impedances consume the amount of power described.

Table 5. MPC8313E Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	NV_{DD} (3.3 V)	$LV_{DDA}/$ LV_{DDB} (3.3 V)	$LV_{DDA}/$ LV_{DDB} (2.5 V)	LV_{DD} (3.3 V)	Unit	Comments
DDR 1, 60% utilization, 50% read/write $R_s = 22 \Omega$ $R_t = 50 \Omega$ single pair of clock capacitive load: data = 8 pF, control address = 8 pF, clock = 8 pF	333 MHz, 32 bits	—	0.355	—	—	—	—	W	—
	266 MHz, 32 bits	—	0.323	—	—	—	—	W	—
DDR 2, 60% utilization, 50% read/write $R_s = 22 \Omega$ $R_t = 75 \Omega$ single pair of clock capacitive load: data = 8 pF, control address = 8 pF, clock = 8 pF	333 MHz, 32 bits	0.266	—	—	—	—	—	W	—
	266 MHz, 32 bits	0.246	—	—	—	—	—	W	—
PCI I/O load = 50 pF	33 MHz	—	—	0.120	—	—	—	W	—
	66 MHz	—	—	0.249	—	—	—	W	—
Local bus I/O load = 20 pF	66 MHz	—	—	—	—	—	0.056	W	—
	50 MHz	—	—	—	—	—	0.040	W	—
TSEC I/O load = 20 pF	MII, 25 MHz	—	—	—	0.008	—	—	W	Multiple by number of interface used
	RGMII, 125 MHz	—	—	—	0.078	0.044	—	W	

5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications.

Table 10. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{\text{PCI_SYNC_IN}}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock and power applied to SYS_CLK_IN when the device is in PCI host mode	32	—	$t_{\text{SYS_CLK_IN}}$	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock and power applied to PCI_SYNC_IN when the device is in PCI agent mode	32	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{\text{PCI_SYNC_IN}}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	$t_{\text{SYS_CLK_IN}}$	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{\text{PCI_SYNC_IN}}$	1
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR configuration signal drivers with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to turn on POR configuration signal drivers with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{\text{PCI_SYNC_IN}}$	1, 3

Notes:

1. $t_{\text{PCI_SYNC_IN}}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is in PCI host mode the primary clock is applied to the SYS_CLK_IN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV.
2. $t_{\text{SYS_CLK_IN}}$ is the clock period of the input clock applied to SYS_CLK_IN. It is only valid when the device is in PCI host mode.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

This table provides the PLL lock times.

Table 11. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface. Note that DDR SDRAM is $\text{GV}_{\text{DD}}(\text{typ}) = 2.5 \text{ V}$ and DDR2 SDRAM is $\text{GV}_{\text{DD}}(\text{typ}) = 1.8 \text{ V}$.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) when $GV_{DD}(typ) = 1.8\text{ V}$.

Table 12. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 1.8\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	-9.9	9.9	μA	4
Output high current ($V_{OUT} = 1.420\text{ V}$)	I_{OH}	-13.4	—	mA	—
Output low current ($V_{OUT} = 0.280\text{ V}$)	I_{OL}	13.4	—	mA	—

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail should track variations in the DC level of MV_{REF} .
4. Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

This table provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8\text{ V}$.

Table 13. DDR2 SDRAM Capacitance for $GV_{DD}(typ) = 1.8\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, \overline{DQS}	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, \overline{DQS}	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 1.8\text{ V} \pm 0.090\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 14. DDR SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 2.5\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	2.3	2.7	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.15$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.15$	V	—

Table 14. DDR SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 2.5\text{ V}$ (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Note
Output leakage current	I_{OZ}	-9.9	-9.9	μA	4
Output high current ($V_{OUT} = 1.95\text{ V}$)	I_{OH}	-16.2	—	mA	—
Output low current ($V_{OUT} = 0.35\text{ V}$)	I_{OL}	16.2	—	mA	—

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail should track variations in the DC level of MV_{REF} .
4. Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

This table provides the DDR capacitance when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 15. DDR SDRAM Capacitance for $GV_{DD}(typ) = 2.5\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5\text{ V} \pm 0.125\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF} .

Table 16. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:

1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ) = 1.8\text{ V}$.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of $1.8 \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.25$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.25$	—	V	—

This table provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of $2.5 \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	—	V	—

This table provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions, with GV_{DD} of $2.5 \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ	t_{CISKEW}	—	—	ps	1, 2
333 MHz	—	–750	750	—	—
266 MHz	—	–750	750	—	—

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

This figure illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

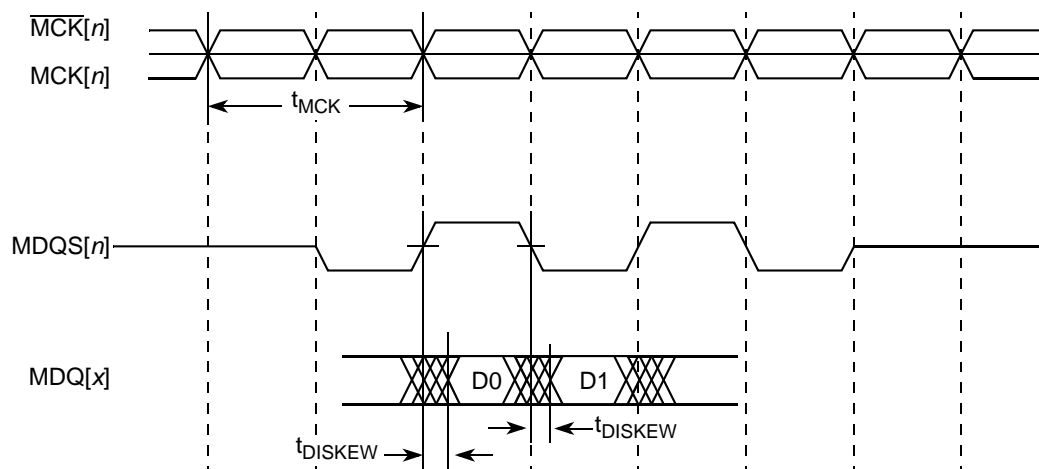


Figure 4. DDR Input Timing Diagram

NOTE

For the ADDR/CMD setup and hold specifications in [Table 21](#), it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

This figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

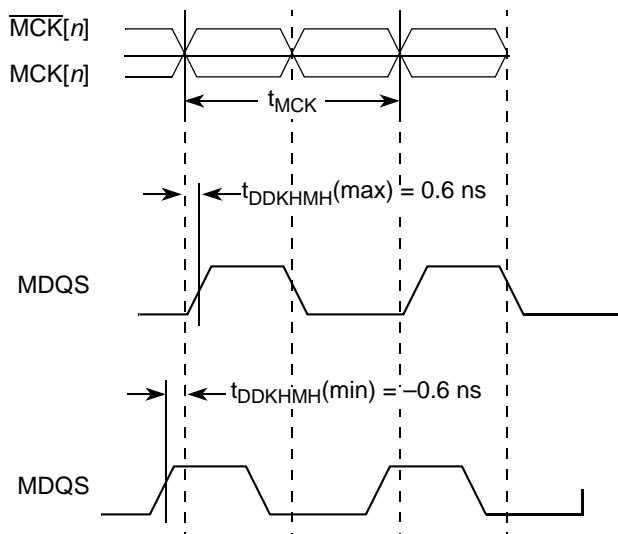


Figure 5. Timing Diagram for t_{DDKHMH}

This figure shows the DDR and DDR2 SDRAM output timing diagram.

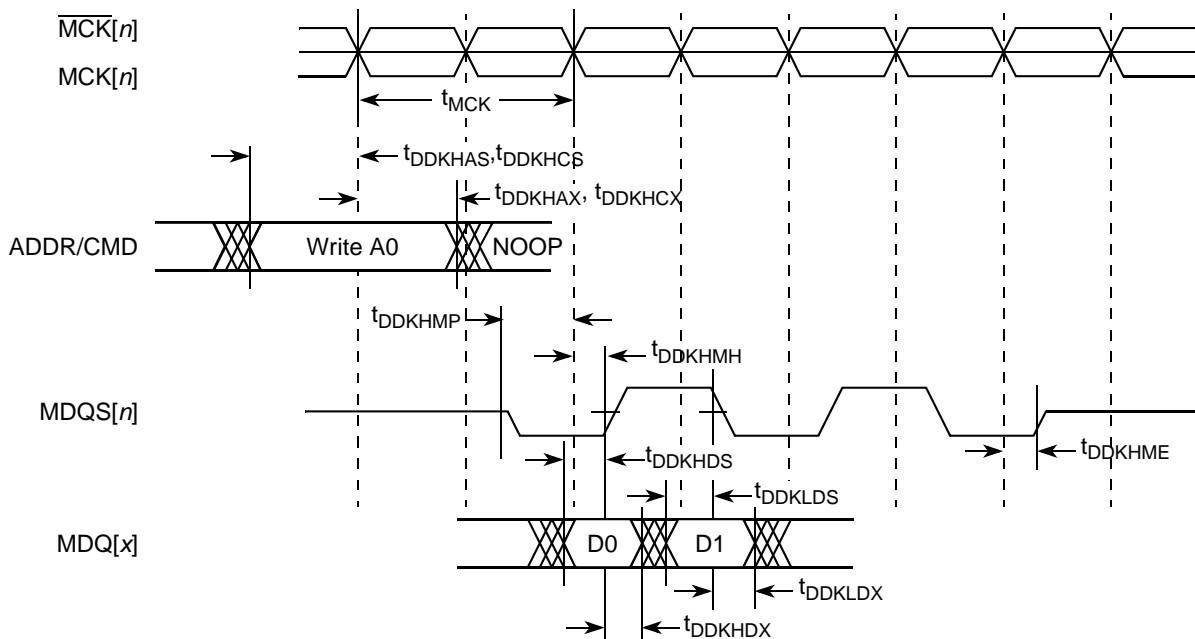


Figure 6. DDR and DDR2 SDRAM Output Timing Diagram

8.2.2 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 30. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{DDB} of $2.5\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	-0.5	—	0.5	ns
Data to clock input skew (at receiver) ²	t_{SKRGT}	1.0	—	2.6	ns
Clock cycle duration ³	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T ^{4, 5}	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX ^{3, 5}	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12}^6	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Note:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the RTBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
- For 10 and 100 Mbps, t_{RGT} scales to $400\text{ ns} \pm 40\text{ ns}$ and $40\text{ ns} \pm 4\text{ ns}$, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- Duty cycle reference is $LV_{DDA}/2$ or $LV_{DDB}/2$.
- This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

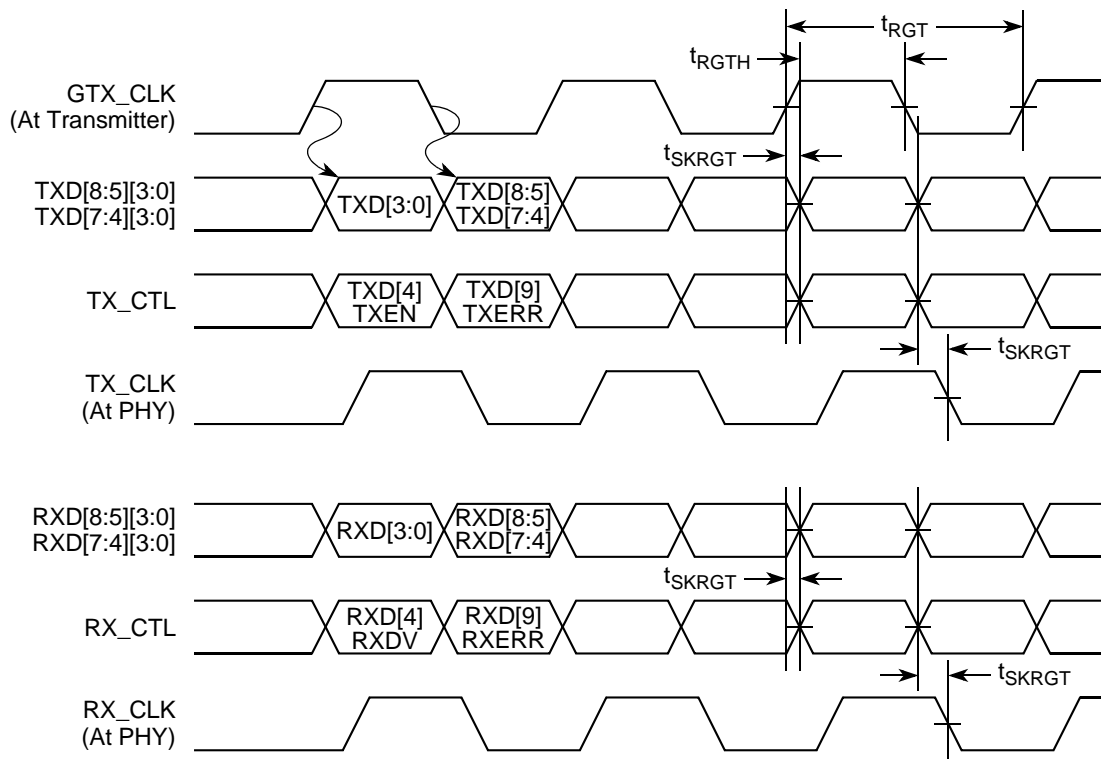


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-coupled serial link from the dedicated SerDes interface of MPC8313E as shown in [Figure 15](#), where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features a 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XCOREVSS. The reference circuit of the SerDes transmitter and receiver is shown in [Figure 33](#).

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in [Section 22.5, "Connection Recommendations,"](#) as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the TSEC_GTX_CLK125 clock is not required for this port. Instead, the SerDes reference clock is required on SD_REF_CLK and $\overline{SD_REF_CLK}$ pins.

8.3.1 DC Requirements for SGMII SD_REF_CLK and $\overline{SD_REF_CLK}$

The characteristics and DC requirements of the separate SerDes reference clock are described in [Section 9, "High-Speed Serial Interfaces \(HSSI\)."](#)

8.3.2 AC Requirements for SGMII SD_REF_CLK and SD_REF_CLK

This table lists the SGMII SerDes reference clock AC requirements. Note that SD_REF_CLK and SD_REF_CLK are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Table 31. SD_REF_CLK and SD_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit
t_{REF}	REFCLK cycle time	—	8	—	ns
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps

8.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 32 and Table 33 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX[n] and SD_TX[n]) as depicted in Figure 16.

Table 32. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$XCOREV_{DD}$	0.95	1.0	1.05	V	
Output high voltage	V_{OH}	—	—	$XCOREV_{DD-Typ}/2 + V_{OD} _{-max}/2$	mV	1
Output low voltage	V_{OL}	$XCOREV_{DD-Typ}/2 - V_{OD} _{-max}/2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	
Output differential voltage ^{2, 3}	$ V_{OD} $	323	500	725	mV	Equalization setting: 1.0x
Output offset voltage	V_{OS}	425	500	575	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	
Mismatch in a pair	ΔR_O	—	—	10	%	
Change in V_{OD} between 0 and 1	$\Delta V_{OD} $	—	—	25	mV	
Change in V_{OS} between 0 and 1	ΔV_{OS}	—	—	25	mV	
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	

Notes:

1. This will not align to DC-coupled SGMII. $XCOREV_{DD-Typ} = 1.0$ V.
2. $|V_{OD}| = |V_{TXn} - V_{\overline{TXn}}|$. $|V_{OD}|$ is also referred as output differential peak voltage. $V_{TX-DIFFp-p} = 2 * |V_{OD}|$.
3. The $|V_{OD}|$ value shown in the Typ column is based on the condition of $XCOREV_{DD-Typ} = 1.0$ V, no common mode offset variation ($V_{OS} = 500$ mV), SerDes transmitter is terminated with 100- Ω differential load between TX[n] and $\overline{TX}[n]$.
4. V_{OS} is also referred to as output common mode voltage.

Table 33. SGMII DC Receiver Electrical Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Common mode input voltage	V_{CM}	—	$V_{XCOREVSS}$	—	V	4

Notes:

1. Input must be externally AC-coupled.
2. $V_{RX_DIFFp-p}$ is also referred to as peak to peak input differential voltage
3. V_{CM_ACp-p} is also referred to as peak to peak AC common mode voltage.
4. On-chip termination to $XCOREV_{SS}$.

8.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (TX[n] and $\overline{TX}[n]$) or at the receiver inputs (RX[n] and $\overline{RX}[n]$) as depicted in Figure 18, respectively.

8.3.4.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 34. SGMII Transmit AC Timing Specifications

At recommended operating conditions with $XCOREV_{DD} = 1.0\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter	JD	—	—	0.17	UI p-p	
Total jitter	JT	—	—	0.35	UI p-p	
Unit interval	UI	799.92	800	800.08	ps	1
V_{OD} fall time (80%–20%)	t_{fall}	50	—	120	ps	
V_{OD} rise time (20%–80%)	t_{rise}	50	—	120	ps	

Note:

1. Each UI is 800 ps \pm 100 ppm.

8.3.4.2 SGMII Receive AC Timing Specifications

This table provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 17 shows the SGMII receiver input compliance mask eye diagram.

Table 35. SGMII Receive AC Timing Specifications

At recommended operating conditions with $XCOREV_{DD} = 1.0\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter tolerance	JD	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal jitter tolerance	JSIN	0.1	—	—	UI p-p	1

Table 49. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 48).

Parameter	Symbol ¹	Min	Max	Unit
Data hold time: CBUS compatible masters I ² C bus devices	t_{I2DXKL}	— 0 ²	— 0.9 ³	μs
Fall time of both SDA and SCL signals ⁵	t_{I2CF}	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times NV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times NV_{DD}$	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The MPC8313E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5. The MPC8313E does not follow the *I²C-BUS Specifications, Version 2.1*, regarding the t_{I2CF} AC parameter.

This figure provides the AC test load for the I²C.

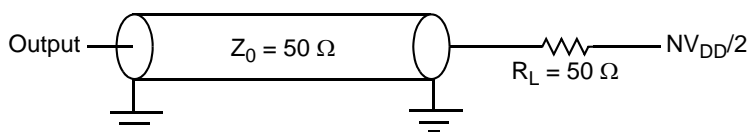


Figure 46. I²C AC Test Load

15.2 Timers AC Timing Specifications

This table provides the Timers input and output AC timing specifications.

Table 54. Timers Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

This figure provides the AC test load for the Timers.

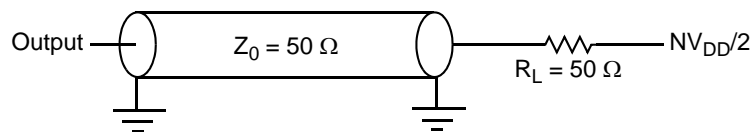


Figure 51. Timers AC Test Load

16 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

16.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO when the GPIO pins are operating from a 3.3-V supply.

Table 55. GPIO (When Operating at 3.3 V) DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -8.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V
Input high voltage	V_{IH}	—	2.0	$NV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq NV_{DD}$	—	± 5	μA

Note:

1. This specification only applies to GPIO pins that are operating from a 3.3-V supply. See [Table 62](#) for the power supply listed for the individual GPIO signal.

This table provides the DC electrical characteristics for the GPIO when the GPIO pins are operating from a 2.5-V supply.

Table 56. GPIO (When Operating at 2.5 V) DC Electrical Characteristics¹

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	NV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$	$NV_{DD} = \text{min}$	2.00	$NV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$	$NV_{DD} = \text{min}$	$V_{SS} - 0.3$	0.40	V
Input high voltage	V_{IH}	—	$NV_{DD} = \text{min}$	1.7	$NV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	$NV_{DD} = \text{min}$	-0.3	0.70	V
Input high current	I_{IH}	$V_{IN} = NV_{DD}$		—	10	μA
Input low current	I_{IL}	$V_{IN} = V_{SS}$		-15	—	μA

Note:

1. This specification only applies to GPIO pins that are operating from a 2.5-V supply. See [Table 62](#) for the power supply listed for the individual GPIO signal

16.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 57. GPIO Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

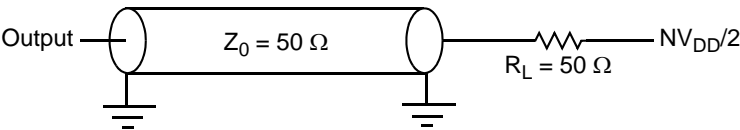


Figure 52. GPIO AC Test Load

Table 62. MPC8313E TEPBGAI Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
SPI				
SPIMOSI/GTM1_TIN3/GTM2_TIN4/GPIO28/LSRCID4	H1	I/O	NV _{DD}	—
SPIMISO/GTM1_TGATE3/GTM2_TGATE4/GPIO29/LDVAL	H3	I/O	NV _{DD}	—
SPICLK/GTM1_TOUT3/GPIO30	G1	I/O	NV _{DD}	—
SPISEL/GPIO31	G3	I/O	NV _{DD}	—
Power and Ground Supplies				
AV _{DD1}	F14	Power for e300 core APLL (1.0 V)	—	—
AV _{DD2}	P21	Power for system APLL (1.0 V)	—	—
GV _{DD}	A2,A3,A4,A24,A25,B3,B4,B5,B12,B13,B20,B21,B24,B25,B26,D1,D2,D8,D9,D16,D17	Power for DDR1 and DDR2 DRAM I/O voltage (1.8/2.5 V)	—	—
LV _{DD}	D24,D25,G23,H23,R23,T23,W25,Y25,AA22,AC23	Power for local bus (3.3 V)	—	—
LV _{DDA}	W2,Y2	Power for eTSEC2 (2.5 V, 3.3 V)	—	—
LV _{ddb}	AC8,AC9,AE4,AE5	Power for eTSEC1/USB DR (2.5 V, 3.3 V)	—	—
MV _{REF}	C14,D14	Reference voltage signal for DDR	—	—
NV _{DD}	G4,H4,L2,M2,AC16,AC17,AD25,AD26,AE12,AE13,AE20,AE21,AE24,AE25,AE26,AF24,AF25	Standard I/O voltage (3.3 V)	—	—
V _{DD}	K11,K12,K13,K14,K15,K16,L10,L17,M10,M17,N10,N17,U12,U13,	Power for core (1.0 V)	—	—
V _{DDC}	F6,F10,F19,K6,K10,K17,K21,P6,P10,P17,R10,R17,T10,T17,U10,U11,U14,U15,U16,U17,W6,W21,AA6,AA10,AA14,AA19	Internal core logic constant power (1.0 V)	—	—

Table 69. Package Thermal Characteristics for TEPBGAI (continued)

Characteristic	Board Type	Symbol	TEPBGA II	Unit	Note
Junction-to-case	—	$R_{\theta JC}$	8	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	7	°C/W	6

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

21.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

21.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

21.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter

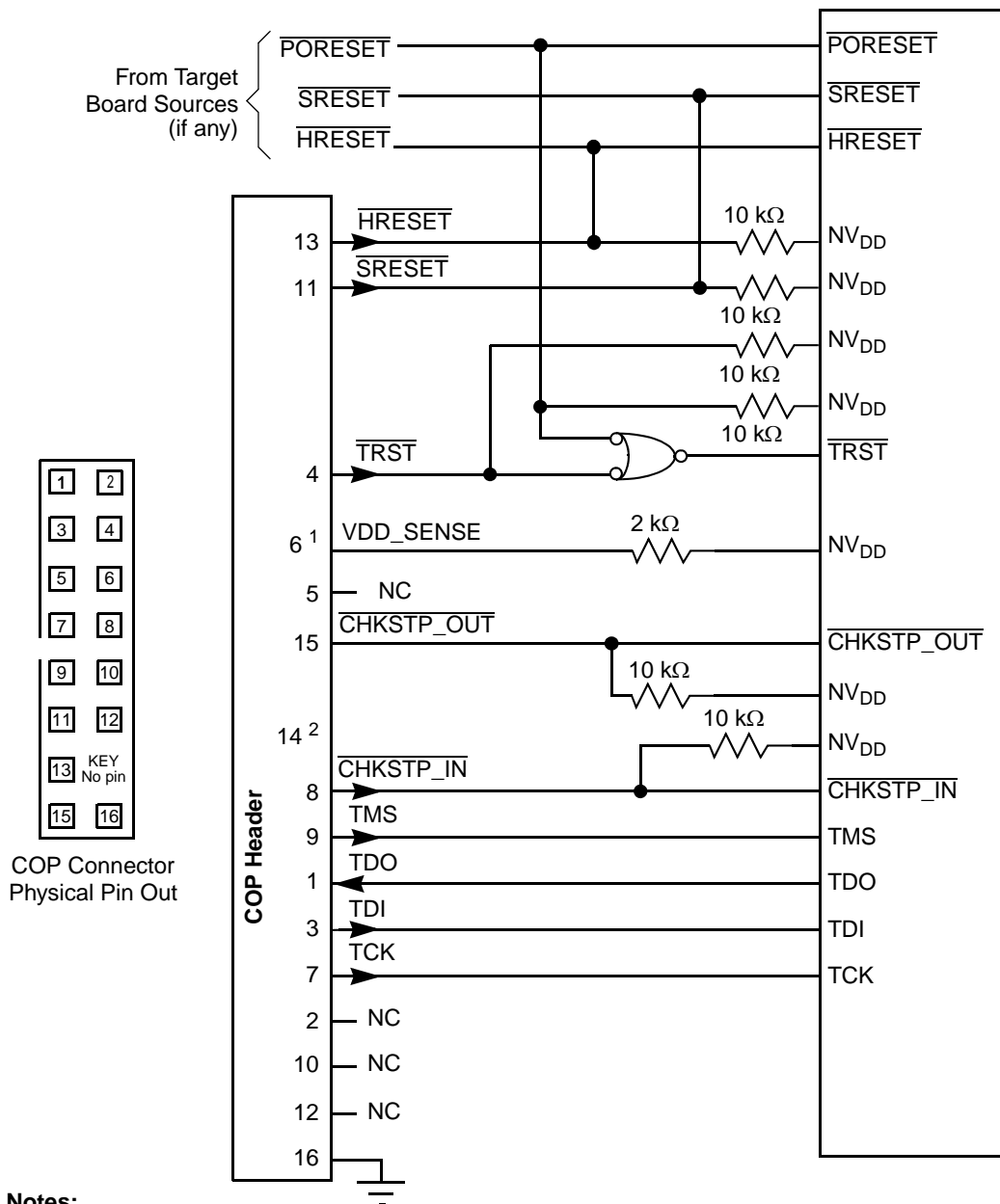
$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 70. Thermal Resistance for TEPBGAll with Heat Sink in Open Flow

Heat Sink Assuming Thermal Grease	Airflow	Thermal Resistance (°C/W)
Wakefield 53 × 53 × 2.5 mm pin fin	Natural convection	13.0
	0.5 m/s	10.6
	1 m/s	9.7
	2 m/s	9.2
	4 m/s	8.9
Aavid 35 × 31 × 23 mm pin fin	Natural convection	14.4
	0.5 m/s	11.3
	1 m/s	10.5
	2 m/s	9.9
	4 m/s	9.4
Aavid 30 × 30 × 9.4 mm pin fin	Natural convection	16.5
	0.5 m/s	13.5
	1 m/s	12.1
	2 m/s	10.9
	4 m/s	10.0
Aavid 43 × 41 × 16.5 mm pin fin	Natural convection	14.5
	0.5 m/s	11.7
	1 m/s	10.5
	2 m/s	9.7
	4 m/s	9.2

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in [Table 70](#). More detailed thermal models can be made available on request.



Notes:

1. Some systems require power to be fed from the application board into the debugger repeater card via the COP header. In this case the resistor value for VDD_SENSE should be around 20 Ω .
2. Key location; pin 14 is not physically present on the COP header.

Figure 61. JTAG Interface Connection

23 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in [Section 23.1, “Part Numbers Fully Addressed by this Document.”](#)