E·XFL

NXP USA Inc. - MPC8313ECVRAGDB Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	·
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8313ecvragdb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



- Full and half-duplex Ethernet support (1000 Mbps supports only full-duplex):
 - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
 - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE 802.1 virtual local area network (VLAN) tags and priority
 - VLAN insertion and deletion
 - Per-frame VLAN control word or default VLAN for each eTSEC
 - Extracted VLAN control word passed to software separately
 - Retransmission following a collision
 - CRC generation and verification of inbound/outbound packets
 - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
 - MAC address recognition:
 - Exact match on primary and virtual 48-bit unicast addresses
 - VRRP and HSRP support for seamless router fail-over
 - Up to 16 exact-match MAC addresses supported
 - Broadcast address (accept/reject)
 - Hash table match on up to 512 multicast addresses
 - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status

1.8 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model supports 5 external and 34 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

1.9 Power Management Controller (PMC)

The MPC8313E power management controller includes the following features:

- Provides power management when the device is used in both host and agent modes
- Supports PCI power management 1.2 D0, D1, D2, D3hot, and D3cold states
- On-chip split power supply controlled through external power switch for minimum standby power
- Support for PME generation in PCI agent mode, PME detection in PCI host mode
- Supports wake-up from Ethernet (Magic Packet), USB, GPIO, and PCI (PME input as host)



Characteristic	Symbol	Recommended Value ¹	Unit	Current Requirement
Core supply voltage	V _{DD}	1.0 V ± 50 mV	V	469 mA
Internal core logic constant power	V _{DDC}	1.0 V ± 50 mV	V	377 mA
SerDes internal digital power	XCOREV _{DD}	1.0	V	170 mA
SerDes internal digital ground	XCOREV _{SS}	0.0	V	—
SerDes I/O digital power	XPADV _{DD}	1.0	V	10 mA
SerDes I/O digital ground	XPADV _{SS}	0.0	V	_
SerDes analog power for PLL	SDAV _{DD}	1.0 V ± 50 mV	V	10 mA
SerDes analog ground for PLL	SDAV _{SS}	0.0	V	—
Dedicated 3.3 V analog power for USB PLL	USB_PLL_PWR3	3.3 V ± 300 mV	V	2–3 mA
Dedicated 1.0 V analog power for USB PLL	USB_PLL_PWR1	1.0 V ± 50 mV	V	2–3 mA
Dedicated analog ground for USB PLL	USB_PLL_GND	0.0	V	—
Dedicated USB power for USB bias circuit	USB_VDDA_BIAS	3.3 V ± 300 mV	V	4–5 mA
Dedicated USB ground for USB bias circuit	USB_VSSA_BIAS	0.0	V	—
Dedicated power for USB transceiver	USB_VDDA	3.3 V ± 300 mV	V	75 mA
Dedicated ground for USB transceiver	USB_VSSA	0.0	V	
Analog power for e300 core APLL	AV _{DD1} ⁶	1.0 V ± 50 mV	V	2–3 mA
Analog power for system APLL	AV _{DD2} ⁶	1.0 V ± 50 mV	V	2–3 mA
DDR1 DRAM I/O voltage (333 MHz, 32-bit operation)	GV _{DD}	2.5 V ± 125 mV	V	131 mA
DDR2 DRAM I/O voltage (333 MHz, 32-bit operation)	GV _{DD}	1.8 V ± 80 mV	V	140 mA
Differential reference voltage for DDR controller	MV _{REF}	$\begin{array}{c} \mbox{1/2 DDR supply} \\ \mbox{(0.49 \times GV_{DD} to} \\ \mbox{0.51 \times GV_{DD})} \end{array}$	V	_
Standard I/O voltage	NV _{DD}	$3.3 \text{ V} \pm 300 \text{ mV}^2$	V	74 mA
eTSEC2 I/O supply	LV _{DDA}	2.5 V ± 125 mV/ 3.3 V ± 300 mV	V	22 mA
eTSEC1/USB DR I/O supply	LV _{DDB}	2.5 V ± 125 mV/ 3.3 V ± 300 mV	V	44 mA
Supply for eLBC IOs	LV _{DD}	3.3 V ± 300 mV	V	16 mA
Analog and digital ground	V _{SS}	0.0	V	_
Junction temperature range	T _A /T _J ³	0 to 105	°C	

Table 2. Recommended Operating Conditions



Driver Type	Output Impedance (Ω)	Supply Voltage
DDR2 signal	18	GV _{DD} = 1.8 V
DUART, system control, I ² C, JTAG, SPI	42	NV _{DD} = 3.3 V
GPIO signals	42	NV _{DD} = 3.3 V
eTSEC signals	42	LV_{DDA} , LV_{DDB} = 2.5/3.3 V
USB signals	42	LV _{DDB} = 2.5/3.3 V

Table 3. Output Drive Capability (continued)

2.2 Power Sequencing

The MPC8313E does not require the core supply voltage (V_{DD} and V_{DDC}) and I/O supply voltages (GV_{DD} , LV_{DD} , and NV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD} and V_{DDC}) before the I/O voltage (GV_{DD} , LV_{DD} , and NV_{DD}) and assert PORESET before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating PORESET.

Note that there is no specific power down sequence requirement for the MPC8313E. I/O voltage supplies $(GV_{DD}, LV_{DD}, and NV_{DD})$ do not have any ordering requirements with respect to one another.



Figure 3. Power-Up Sequencing Example



4.2 AC Electrical Characteristics

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the system clock input (SYS_CLK_IN/PCI_CLK) AC timing specifications for the MPC8313E.

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Note
SYS_CLK_IN/PCI_CLK frequency	fsys_clk_in	24	_	66.67	MHz	1
SYS_CLK_IN/PCI_CLK cycle time	^t SYS_CLK_IN	15	_	_	ns	—
SYS_CLK_IN rise and fall time	t _{KH} , t _{KL}	0.6	0.8	4	ns	2
PCI_CLK rise and fall time	t _{PCH} , t _{PCL}	0.6	0.8	1.2	ns	2
SYS_CLK_IN/PCI_CLK duty cycle	t _{KHK} /t _{SYS_CLK_IN}	40	_	60	%	3
SYS_CLK_IN/PCI_CLK jitter	_	_	_	±150	ps	4, 5

Table 8. SYS_CLK_IN AC Timing Specifications

Notes:

1. Caution: The system, core, security block must not exceed their respective maximum or minimum operating frequencies.

2. Rise and fall times for SYS_CLK_IN/PCI_CLK are measured at 0.4 and 2.4 V.

3. Timing is guaranteed by design and characterization.

4. This represents the total input jitter-short term and long term-and is guaranteed by design.

5. The SYS_CLK_IN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.

5 **RESET** Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8313E.

5.1 **RESET DC Electrical Characteristics**

This table provides the DC electrical characteristics for the RESET pins.

Table 9. RESET Pins DC Electrical Characteristic
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Characteristic	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	—	2.1	NV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0~V \leq V_{IN} \leq NV_{DD}$	—	±5	μA
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V



Parameter	Symbol ¹	Min	Max	Unit	Note
MCK[<i>n</i>] cycle time, MCK[<i>n</i>]/MCK[<i>n</i>] crossing	t _{MCK}	6	10	ns	2
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz	t _{DDKHAS}	2.1 2.5	_	ns	3
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz	t _{DDKHAX}	2.0 2.7	_	ns	3
MCS[<i>n</i>] output setup with respect to MCK 333 MHz 266 MHz	t _{DDKHCS}	2.1 3.15	_	ns	3
MCS[<i>n</i>] output hold with respect to MCK 333 MHz 266 MHz	t _{DDKHCX}	2.0 2.7	_	ns	3
MCK to MDQS Skew	t _{DDKHMH}	-0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS 333 MHz 266 MHz	^t DDKHDS, ^t DDKLDS	800 900		ps	5
MDQ//MDM output hold with respect to MDQS 333 MHz 266 MHz	^t DDKHDX, ^t DDKLDX	750 1000		ps	5
MDQS preamble start	t _{DDKHMP}	$-0.5\times t_{MCK}-0.6$	$-0.5 \times t_{\text{MCK}} + 0.6$	ns	6
MDQS epilogue end	t _{DDKHME}	-0.6	0.6	ns	6

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Silicon Rev 2.x or Later

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 </sub>
- 2. All MCK/MCK referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ//MDM/MDQS.
- 4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual, for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.



This figure provides the AC test load for the DDR bus.



Figure 7. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V _{IH}	2.0	NV _{DD} + 0.3	V
Low-level input voltage NV _{DD}	V _{IL}	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	$NV_{DD} - 0.2$	—	V
Low-level output voltage, I _{OL} = 100 μA	V _{OL}	—	0.2	V
Input current (0 V \leq V _{IN} \leq NV _{DD})	I _{IN}	—	±5	μA

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	_	2

Notes:

1. Actual attainable baud rate is limited by the latency of interrupt processing.

2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.





Figure 15. 4-Wire AC-Coupled SGMII Serial Link Connection Example



Figure 16. SGMII Transmitter DC Measurement Circuit

Table 33.	SGMII DC	Receiver	Electrical	Characteristics
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Parameter	Symbol	Min	Тур	Max	Unit	Note
Supply voltage	XCOREV _{DD}	0.95	1.0	1.05	V	
DC Input voltage range			N/A			1
Input differential voltage	V _{RX_DIFFp-p}	100	—	1200	mV	2
Loss of signal threshold	VL _{OS}	30	—	100	mV	
Input AC common mode voltage	V _{CM_ACp-p}	—	—	100	mV	3
Receiver differential input impedance	Z _{RX_DIFF}	80	100	120	Ω	
Receiver common mode input impedance	Z _{RX_CM}	20	—	35	Ω	



Table 36. eTSEC IEEE 1588 AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5%.

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Note
TSEC_1588_CLK peak-to-peak jitter	t _{T1588} CLKINJ	—	_	250	ps	
Rise time eTSEC_1588_CLK (20%-80%)	t _{T1588} CLKINR	1.0	_	2.0	ns	
Fall time eTSEC_1588_CLK (80%–20%)	t _{T1588} CLKINF	1.0	_	2.0	ns	
TSEC_1588_CLK_OUT clock period	t _{T1588} CLKOUT	$2 \times t_{T1588CLK}$	_	_	ns	
TSEC_1588_CLK_OUT duty cycle	^t t1588CLKOTH /t _{T1588} CLKOUT	30	50	70	%	
TSEC_1588_PULSE_OUT	t _{T1588OV}	0.5	_	3.0	ns	
TSEC_1588_TRIG_IN pulse width	t _{T1588} TRIGH	$2 \times t_{T1588CLK_MAX}$	_	—	ns	2

Notes:

1. T_{RX_CLK} is the max clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for a description of TMR_CTRL registers.

2. It need to be at least two times of clock period of clock selected by TMR_CTRL[CKSEL]. See the MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual, for a description of TMR_CTRL registers.

The maximum value of t_{T1588CLK} is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of t_{T1588CLK} is 3600, 280, and 56 ns, respectively.

8.5 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, RMII, RGMII, SGMII, and RTBI are specified in Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics."

8.5.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. Table 37 provide the DC electrical characteristics for MDIO and MDC.

Parameter	Symbol	Condi	Min	Мах	Unit	
Supply voltage (3.3 V)	NV _{DD}		—			V
Output high voltage	V _{OH}	I _{OH} = -1.0 mA	NV _{DD} = Min	2.10	NV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$NV_{DD} = Min$	V _{SS}	0.50	V
Input high voltage	V _{IH}		2.0	_	V	
Input low voltage	V _{IL}			0.80	V	
Input high current	I _{IH}	NV _{DD} = Max	$V_{IN}^{1} = 2.1 V$	—	40	μΑ
Input low current	Ι _{IL}	NV _{DD} = Max	V _{IN} = 0.5 V	-600	—	μΑ

 Table 37. MII Management DC Electrical Characteristics When Powered at 3.3 V



9 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

9.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 22 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TXn and \overline{TXn}) or a receiver input (RXn and \overline{RXn}). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-ended swing

The transmitter output signals and the receiver input signals TXn, \overline{TXn} , RXn, and \overline{RXn} each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

2. Differential output voltage, V_{OD} (or differential output swing):

The differential output voltage (or swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{TXn} - V_{\overline{TXn}}$. The V_{OD} value can be either positive or negative.

3. Differential input voltage, V_{ID} (or differential input swing):

The differential input voltage (or swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{RXn} - V_{\overline{RXn}}$. The V_{ID} value can be either positive or negative.

- 4. Differential peak voltage, V_{DIFFp} The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.
- 5. Differential peak-to-peak, V_{DIFFp-p}

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

6. Differential waveform

The differential waveform is constructed by subtracting the inverting signal (TX*n*, for example) from the non-inverting signal (TX*n*, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 22 as an example for differential waveform.

7. Common mode voltage, V_{cm}



This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8313E SerDes reference clock input's DC requirement.



Figure 27. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8313E SerDes reference clock input's allowed range (100 to 400 mV), the AC-coupled connection scheme must be used. It assumes the LVDS output driver features a 50- Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.



Figure 28. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the MPC8313E SerDes reference clock input's DC requirement, AC coupling has to be used. Figure 29





Figure 32. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. Refer to the following section for detailed information:

• Section 8.3.2, "AC Requirements for SGMII SD_REF_CLK and SD_REF_CLK"

9.2.4.1 Spread Spectrum Clock

SD_REF_CLK/SD_REF_CLK are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

9.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for the SerDes data lane's transmitter and receiver.



Figure 33. SerDes Transmitter and Receiver Reference Circuits

The SerDes data lane's DC and AC specifications are defined in the interface protocol section listed below (SGMII) based on the application usage:

• Section 8.3, "SGMII Interface Electrical Characteristics"

Please note that a external AC-coupling capacitor is required for the above serial transmission protocol with the capacitor value defined in the specifications of the protocol section.



Table 45. Local Bus General Timing Parameters (continued)

	Parameter	Symbol ¹	Min	Max	Unit	Note
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Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1).
 </sub>
- 2. All timings are in reference to falling edge of LCLK0 (for all outputs and for LGTA and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
- 3. All signals are measured from NV_{DD}/2 of the rising/falling edge of LCLK0 to $0.4 \times NV_{DD}$ of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. t_{LBOTOT1} and t_{LALETOT1} should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- 6. t_{LBOTOT2} and t_{LALETOT2} should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- 7. t_{LBOTOT3} and t_{LALETOT3} should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.
- 8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This figure provides the AC test load for the local bus.



Figure 36. Local Bus AC Test Load



Table 49. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 48).

Parameter	Symbol ¹	Min	Max	Unit
Data hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	$\overline{0^2}$	 0.9 ³	μs
Fall time of both SDA and SCL signals ⁵	t _{I2CF}	—	300	ns
Setup time for STOP condition	t _{I2PVKH}	0.6	_	μs
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	_	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times NV_{DD}$	_	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times \text{NV}_{\text{DD}}$	_	V

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{12DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. Also, t_{12SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{12C} clock reference (K) going to the bigh (H) state or hold time. Also, t_{12PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{12C} clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 </sub>
- The MPC8313E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- 3. The maximum t_{12DVKH} has only to be met if the device does not stretch the LOW period (t_{12CL}) of the SCL signal.
- 4. C_B = capacitance of one bus line in pF.
- 5. The MPC8313E does not follow the l^2C -BUS Specifications, Version 2.1, regarding the t_{I2CF} AC parameter.

This figure provides the AC test load for the I^2C .



Figure 46. I²C AC Test Load



Parameter	Symbol ¹	Min	Мах	Unit	Note
Clock to output high impedance	t _{PCKHOZ}	_	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t _{PCIXKH}	0	—	ns	2, 4

Table 51. PCI AC Timing Specifications at 66 MHz (continued)

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
</sub></sub>

2. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.

- 3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.

This table shows the PCI AC timing specifications at 33 MHz.

Table 52. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Мах	Unit	Note
Clock to output valid	^t PCKHOV	—	11	ns	2
Output hold from clock	t _{PCKHOX}	2	—	ns	2
Clock to output high impedance	t _{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	^t PCIVKH	3.0	—	ns	2, 4
Input hold from clock	t _{PCIXKH}	0	—	ns	2, 4

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
</sub>

- 2. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.
- 3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.

This figure provides the AC test load for PCI.



Figure 48. PCI AC Test Load



Table 62. MPC8313E TEPBGAII Pi	inout Listing (continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Note
MEMC_MCS0	D10	0	GV _{DD}	_
MEMC_MCS1	A10	0	GV _{DD}	_
MEMC_MCKE	B14	0	GV _{DD}	3
MEMC_MCK	A13	0	GV _{DD}	_
MEMC_MCK	A14	0	GV _{DD}	_
MEMC_MODT0	B23	0	GV _{DD}	_
MEMC_MODT1	C23	0	GV _{DD}	_
Local Bus	Controller Interface			
LAD0	K25	I/O	LV _{DD}	11
LAD1	K24	I/O	LV _{DD}	11
LAD2	K23	I/O	LV _{DD}	11
LAD3	K22	I/O	LV _{DD}	11
LAD4	J25	I/O	LV _{DD}	11
LAD5	J24	I/O	LV _{DD}	11
LAD6	J23	I/O	LV _{DD}	11
LAD7	J22	I/O	LV _{DD}	11
LAD8	H24	I/O	LV _{DD}	11
LAD9	F26	I/O	LV _{DD}	11
LAD10	G24	I/O	LV _{DD}	11
LAD11	F25	I/O	LV _{DD}	11
LAD12	E25	I/O	LV _{DD}	11
LAD13	F24	I/O	LV _{DD}	11
LAD14	G22	I/O	LV _{DD}	11
LAD15	F23	I/O	LV _{DD}	11
LA16	AC25	0	LV _{DD}	11
LA17	AC26	0	LV _{DD}	11
LA18	AB22	0	LV _{DD}	11
LA19	AB23	0	LV _{DD}	11
LA20	AB24	0	LV _{DD}	11
LA21	AB25	0	LV _{DD}	11
LA22	AB26	0	LV _{DD}	11
LA23	E22	0	LV _{DD}	11



The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICOEn] parameters select whether the PCI_SYNC_OUT is driven out on the PCI_CLK_OUTn signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the SYS_CLK_IN signal should be tied to VSS.

As shown in Figure 57, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (csb_clk), the internal clock for the DDR controller (ddr_clk), and the internal clock for the local bus interface unit (lbc_clk).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = \{PCI_SYNC_IN \times (1 + \sim \overline{CFG_CLKIN_DIV})\} \times SPMF$$

In PCI host mode, PCI_SYNC_IN \times (1 + \sim CFG_CLKIN_DIV) is the SYS_CLK_IN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, "Reset, Clocking, and Initialization," in the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*, for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

 $ddr_clk = csb_clk \times (1 + \text{RCWL}[\text{DDRCM}])$

Note that ddr_clk is not the external memory bus frequency; ddr_clk passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and MCK). However, the data rate is the same frequency as ddr_clk .

The internal *lbc_clk* frequency is determined by the following equation:

 $lbc_clk = csb_clk \times (1 + \text{RCWL[LBCM]})$

Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the a LBC clock divider to create the external local bus clock outputs (LCLK[0:1]). The LBC clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the csb_clk frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 63 specifies which units have a configurable clock frequency.



Unit	Default Frequency	Options
TSEC1	csb_clk	Off, csb_clk, csb_clk/2, csb_clk/3
TSEC2	csb_clk	Off, csb_clk, csb_clk/2, csb_clk/3
Security Core, I ² C, SAP, TPR	csb_clk	Off, csb_clk, csb_clk/2, csb_clk/3
USB DR	csb_clk	Off, csb_clk, csb_clk/2, csb_clk/3
PCI and DMA complex	csb_clk	Off, csb_clk

Table 63. Configurable Clock Units

This table provides the operating frequencies for the MPC8313E TEPBGAII under recommended operating conditions (see Table 2).

Characteristic ¹	Maximum Operating Frequency	Unit
e300 core frequency (core_clk)	333	MHz
Coherent system bus frequency (<i>csb_clk</i>)	167	MHz
DDR1/2 memory bus frequency (MCK) ²	167	MHz
Local bus frequency (LCLKn) ³	66	MHz
PCI input frequency (SYS_CLK_IN or PCI_CLK)	66	MHz

Table 64. Operating Frequencies for TEPBGAII

Note:

- The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK[0:1], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM] and SCCR[USBDRCM] must be programmed such that the maximum internal operating frequency of the security core and USB modules do not exceed their respective value listed in this table.
- 2. The DDR data rate is 2x the DDR memory bus frequency.
- 3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbc_clk* frequency (depending on LCRR[CLKDIV]), which is in turn, 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

20.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. This table shows the multiplication factor encodings for the system PLL.

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3

Table 65. System PLL Multiplication Factors



RCWL[SPMF]	System PLL Multiplication Factor
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

Table 65. System PLL Multiplication Factors (continued)

Note:

1. If RCWL[DDRCM] and RCWL[LBCM] are both cleared, the system PLL VCO frequency = (CSB frequency) × (System PLL VCO Divider).

2. If either RCWL[DDRCM] or RCWL[LBCM] are set, the system PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO Divider).

3. The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz

As described in Section 20, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (SYS_CLK_IN or PCI_SYNC_IN) and the internal coherent system bus clock (*csb_clk*). This table shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN/PCI_SYNC_IN ratios.

			Input Clock Frequency (MHz) ²			
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> :Input Clock Ratio ²	24	25	33.33	66.67
			<i>csb_clk</i> Frequency (MHz)			
High	0010	2:1				133
High	0011	3:1			100	
High	0100	4:1		100	133	
High	0101	5:1	120	125	167	
High	0110	6:1	144	150		
Low	0010	2:1				133
Low	0011	3:1			100	
Low	0100	4:11		100	133	
Low	0101	5:1	120	125	167	
Low	0110	6:1	144	150		

Table 66. CSB Frequency Options

¹ CFG_CLKIN_DIV select the ratio between SYS_CLK_IN and PCI_SYNC_OUT.

² SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.



Heat sink Vendors include the following list:				
Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988			
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601			
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277			
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770			
Tyco Electronics Chip Coolers [™] P.O. Box 3668 Harrisburg, PA 17105 Internet: www.chipcoolers.com	800-522-6752			
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-2800			
Interface material vendors include the following:				
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850			
Dow-Corning Corporation Corporate Center	800-248-2481			
PO BOX 994				
Midland, MI 48686-0994 Internet: www.dowcorning.com				
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674			
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572			



Rev. Number	Date	Substantive Change(s)		
2	10/2008	 Added Note "The information in this document is accurate for revision 1.0, and 2.x and later. See Section 24.1, "Part Numbers Fully Addressed by this Document," before Section 1, "Overview." Added part numbering details for all the silicon revisions in Table 74. Changed V_{IH} from 2.7 V to 2.4 V in Table 7. Added a row for V_{IH} level for Rev 2.x or later in Table 45. Added a column for maximum power dissipation in low power mode for Rev 2.x or later silicon in Table 6. Added a column for Power Nos for Rev 2.x or later silicon and added a row for 400 MHz in Table 4. Added Table 21 for DDR AC Specs on Rev 2.x or later silicon. Added Section 9, "High-Speed Serial Interfaces (HSSI)," Added LFWE, LFCLE, LFALE, LOE, LFRE, LFWP, LGTA, LUPWAIT, and LFRB in Table 63. In Table 39, added note 2: "This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)" Removed mentions of SGMII (SGMII has separate specs) from Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics." Corrected Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII/SGMII/RTBI Electrical Characteristics." Corrected Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII/SGMII/RTBI Electrical Characteristics." to state that RGMII/RTBI interfaces only operate at 2.5 V, not 3.3 V. Added ZQ package to ordering information In Table 74 and Section 19.1, "Package Parameters for the MPC8313E TEPBGAII" (applicable to both silicon rev. 1.0 and 2.1) Removed footnotes 5 and 6 from Table 1 (left over when the PCI undershoot/overshoot voltages and maximum AC waveforms were removed from Section 2.1.2, "Power Supply Voltage Specification"). Removed SD_PLL_TPD (T2) and SD_PLL_TPA_ANA (R4) from T		
		• Auueu Section 24.2, Fait Marking, and Figure 62.		

Table 73. Document Revision History (continued)

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