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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	267MHz
Co-Processors/DSP	Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8313eczqadd

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1.6 USB Dual-Role Controller

The MPC8313E USB controller includes the following features:

- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Compatible with Universal Serial Bus Specification, Rev. 2.0
- Supports operation as a stand-alone USB device
 - Supports one upstream facing port
 - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
 - Supports USB root hub with one downstream-facing port
 - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI + low pin interface (ULPI) or on-chip USB 2.0 full-speed/high-speed PHY

1.7 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8313E eTSECs include the following features:

- Two RGMII/SGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3®, 802.3u®, 802.3x®, 802.3z®, 802.3au®, and 802.3ab®
- Support for Wake-on-Magic Packet[™], a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status
- Three-speed support (10/100/1000 Mbps)
- On-chip high-speed serial interface to external SGMII PHY interface
- Support for IEEE Std 1588TM
- Support for two full-duplex FIFO interface modes
- Multiple PHY interface configuration
- TCP/IP acceleration and QoS features available
- IP v4 and IP v6 header recognition on receive
- IP v4 header checksum verification and generation
- TCP and UDP checksum verification and generation
- Per-packet configurable acceleration
- Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2[®], PPPoE session, MPLS stacks, and ESP/AH IP-security headers
- Transmission from up to eight physical queues.
- Reception to up to eight physical queues



Driver Type	Output Impedance (Ω)	Supply Voltage
DDR2 signal	18	GV _{DD} = 1.8 V
DUART, system control, I ² C, JTAG, SPI	42	NV _{DD} = 3.3 V
GPIO signals	42	NV _{DD} = 3.3 V
eTSEC signals	42	LV_{DDA} , LV_{DDB} = 2.5/3.3 V
USB signals	42	LV _{DDB} = 2.5/3.3 V

Table 3. Output Drive Capability (continued)

2.2 Power Sequencing

The MPC8313E does not require the core supply voltage (V_{DD} and V_{DDC}) and I/O supply voltages (GV_{DD} , LV_{DD} , and NV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD} and V_{DDC}) before the I/O voltage (GV_{DD} , LV_{DD} , and NV_{DD}) and assert PORESET before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating PORESET.

Note that there is no specific power down sequence requirement for the MPC8313E. I/O voltage supplies $(GV_{DD}, LV_{DD}, and NV_{DD})$ do not have any ordering requirements with respect to one another.



Figure 3. Power-Up Sequencing Example



4.2 AC Electrical Characteristics

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the system clock input (SYS_CLK_IN/PCI_CLK) AC timing specifications for the MPC8313E.

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Note
SYS_CLK_IN/PCI_CLK frequency	fsys_clk_in	24	_	66.67	MHz	1
SYS_CLK_IN/PCI_CLK cycle time	^t SYS_CLK_IN	15	_	_	ns	—
SYS_CLK_IN rise and fall time	t _{KH} , t _{KL}	0.6	0.8	4	ns	2
PCI_CLK rise and fall time	t _{PCH} , t _{PCL}	0.6	0.8	1.2	ns	2
SYS_CLK_IN/PCI_CLK duty cycle	t _{KHK} /t _{SYS_CLK_IN}	40	_	60	%	3
SYS_CLK_IN/PCI_CLK jitter	_	_	_	±150	ps	4, 5

Table 8. SYS_CLK_IN AC Timing Specifications

Notes:

1. Caution: The system, core, security block must not exceed their respective maximum or minimum operating frequencies.

2. Rise and fall times for SYS_CLK_IN/PCI_CLK are measured at 0.4 and 2.4 V.

3. Timing is guaranteed by design and characterization.

4. This represents the total input jitter-short term and long term-and is guaranteed by design.

5. The SYS_CLK_IN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.

5 **RESET** Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8313E.

5.1 **RESET DC Electrical Characteristics**

This table provides the DC electrical characteristics for the RESET pins.

Table 9. RESET Pins DC Electrical Characteristic
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Characteristic	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	—	2.1	NV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0~V \leq V_{IN} \leq NV_{DD}$	—	±5	μA
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V



This figure provides the AC test load for the DDR bus.



Figure 7. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V _{IH}	2.0	NV _{DD} + 0.3	V
Low-level input voltage NV _{DD}	V _{IL}	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	$NV_{DD} - 0.2$	—	V
Low-level output voltage, I _{OL} = 100 μA	V _{OL}	—	0.2	V
Input current (0 V \leq V _{IN} \leq NV _{DD})	I _{IN}	—	±5	μA

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	_	2

Notes:

1. Actual attainable baud rate is limited by the latency of interrupt processing.

2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.



Parameters	Symbol	Conditions		Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -1.0 mA	LV_{DDA} or $LV_{DDB} = Min$	2.00	LV _{DDA} + 0.3 or LV _{DDB} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	LV_{DDA} or $LV_{DDB} = Min$	V _{SS} – 0.3	0.40	V
Input high voltage	V _{IH}	_	LV_{DDA} or $LV_{DDB} = Min$	1.7	LV _{DDA} + 0.3 or LV _{DDB} + 0.3	V
Input low voltage	V _{IL}	—	LV_{DDA} or LV_{DDB} = Min	-0.3	0.70	V
Input high current	Ι _{ΙΗ}	$V_{IN}^{1} = LV_{DDA} \text{ or } LV_{DDB}$		—	10	μA
Input low current	۱ _{IL}	N	$V_{\rm IN}^{1} = V_{\rm SS}^{1}$	-15	_	μA

Table 25. RGMII/RTBI DC Electrical Characteristics (continued)

Note:

1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.2 MII, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for MII, RMII, RGMII, and RTBI are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 26. MII Transmit AC Timing Specifications

At recommended operating conditions with $LV_{DDA}/LV_{DDB}/NV_{DD}$ of 3.3 V ± 0.3 V.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TX_CLK clock period 10 Mbps	t _{MTX}	_	400	—	ns
TX_CLK clock period 100 Mbps	t _{MTX}	_	40	—	ns
TX_CLK duty cycle	t _{MTXH} /t _{MTX}	35	_	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t _{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V _{IL} (min) to V _{IH} (max)	t _{MTXR}	1.0	_	4.0	ns
TX_CLK data clock fall $V_{IH}(max)$ to $V_{IL}(min)$	t _{MTXF}	1.0		4.0	ns

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>



8.2.2 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 30. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DDA}/LV_{DDB} of 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
Data to clock output skew (at transmitter)	t _{SKRGT}	-0.5	_	0.5	ns
Data to clock input skew (at receiver) ²	t _{SKRGT}	1.0	_	2.6	ns
Clock cycle duration ³	t _{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T ^{4, 5}	t _{RGTH} /t _{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX ^{3, 5}	t _{RGTH} /t _{RGT}	40	50	60	%
Rise time (20%–80%)	t _{RGTR}	_	_	0.75	ns
Fall time (20%–80%)	t _{RGTF}	_	_	0.75	ns
GTX_CLK125 reference clock period	t _{G12} 6	_	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t _{G125H} /t _{G125}	47		53	%

Note:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the RTBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- 2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
- 3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- 5. Duty cycle reference is $LV_{DDA}/2$ or $LV_{DDB}/2$.
- 6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- 7. The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm





Figure 15. 4-Wire AC-Coupled SGMII Serial Link Connection Example



Figure 16. SGMII Transmitter DC Measurement Circuit

Table 33.	SGMII DC	Receiver	Electrical	Characteristics
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Parameter	Symbol	Min	Тур	Max	Unit	Note
Supply voltage	XCOREV _{DD}	0.95	1.0	1.05	V	
DC Input voltage range			N/A			1
Input differential voltage	V _{RX_DIFFp-p}	100	—	1200	mV	2
Loss of signal threshold	VL _{OS}	30	—	100	mV	
Input AC common mode voltage	V _{CM_ACp-p}	—	—	100	mV	3
Receiver differential input impedance	Z _{RX_DIFF}	80	100	120	Ω	
Receiver common mode input impedance	Z _{RX_CM}	20	—	35	Ω	





Figure 25. Differential Reference Clock Input DC Requirements (External AC-Coupled)





9.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to XCOREV_{SS}, the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce a signal with too large of an amplitude and may need to be DC-biased at the clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC coupling.

NOTE

Figure 27 through Figure 30 are for conceptual reference only. Due to the fact that the clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is possible that the clock circuit reference designs provided by clock driver chip vendors are different from what is shown in the figures. They might also vary from one vendor to the other. Therefore, Freescale can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. It is recommended that the system designer contact the selected clock driver chip vendor for the optimal reference circuits for the MPC8313E SerDes reference clock receiver requirement provided in this document.



assumes that the LVPECL clock driver's output impedance is 50 Ω . R1 is used to DC-bias the LVPECL outputs prior to AC coupling. Its value could be ranged from 140 to 240 Ω depending on the clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50- Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8313E SerDes3 reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω . Consult with the clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.



Figure 29. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the MPC8313E SerDes reference clock input's DC requirement.



Figure 30. Single-Ended Connection (Reference Only)





Figure 32. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. Refer to the following section for detailed information:

• Section 8.3.2, "AC Requirements for SGMII SD_REF_CLK and SD_REF_CLK"

9.2.4.1 Spread Spectrum Clock

SD_REF_CLK/SD_REF_CLK are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

9.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for the SerDes data lane's transmitter and receiver.



Figure 33. SerDes Transmitter and Receiver Reference Circuits

The SerDes data lane's DC and AC specifications are defined in the interface protocol section listed below (SGMII) based on the application usage:

• Section 8.3, "SGMII Interface Electrical Characteristics"

Please note that a external AC-coupling capacitor is required for the above serial transmission protocol with the capacitor value defined in the specifications of the protocol section.



This figure provides the boundary-scan timing diagram.



Figure 44. Boundary-Scan Timing Diagram

This figure provides the test access port timing diagram.



Figure 45. Test Access Port Timing Diagram



This figure shows the AC timing diagram for the I^2C bus.



Figure 47. I²C Bus AC Timing Diagram

14 PCI

This section describes the DC and AC electrical specifications for the PCI bus.

14.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface.

Table 50. PCI DC Electrical Characteristics¹

Parameter	Symbol	Test Condition	Min	Мах	Unit
High-level input voltage	V _{IH}	$V_{OUT} \ge V_{OH}$ (min) or	$0.5 imes NV_{DD}$	NV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	$V_{OUT} \le V_{OL}$ (max)	-0.5	$0.3\times \text{NV}_{\text{DD}}$	V
High-level output voltage	V _{OH}	$NV_{DD} = min, I_{OH} = -100 \ \mu A$	$0.9 imes NV_{DD}$	-	V
Low-level output voltage	V _{OL}	NV_{DD} = min, I_{OL} = 100 μ A	_	$0.1 imes NV_{DD}$	V
Input current	I _{IN}	$0~V \leq V_{IN} \leq NV_{DD}$	_	±5	μΑ

Note:

1. Note that the symbol V_{IN} , in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

14.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8313E is configured as a host or agent device.

This table shows the PCI AC timing specifications at 66 MHz.

Table 51. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol ¹	Min	Max	Unit	Note
Clock to output valid	^t PCKHOV	—	6.0	ns	2
Output hold from clock	t _{PCKHOX}	1	—	ns	2



Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_AD6	AD19	I/O	NV _{DD}	
PCI_AD7	AD20	I/O	NV _{DD}	_
PCI_AD8	AC18	I/O	NV _{DD}	_
PCI_AD9	AD18	I/O	NV _{DD}	_
PCI_AD10	AB18	I/O	NV _{DD}	_
PCI_AD11	AE19	I/O	NV _{DD}	_
PCI_AD12	AB17	I/O	NV _{DD}	_
PCI_AD13	AE18	I/O	NV _{DD}	_
PCI_AD14	AD17	I/O	NV _{DD}	_
PCI_AD15	AF19	I/O	NV _{DD}	_
PCI_AD16	AB14	I/O	NV _{DD}	_
PCI_AD17	AF15	I/O	NV _{DD}	_
PCI_AD18	AD14	I/O	NV _{DD}	_
PCI_AD19	AE14	I/O	NV _{DD}	_
PCI_AD20	AF12	I/O	NV _{DD}	_
PCI_AD21	AE11	I/O	NV _{DD}	_
PCI_AD22	AD12	I/O	NV _{DD}	_
PCI_AD23	AB13	I/O	NV _{DD}	_
PCI_AD24	AF9	I/O	NV _{DD}	_
PCI_AD25	AD11	I/O	NV _{DD}	_
PCI_AD26	AE10	I/O	NV _{DD}	_
PCI_AD27	AB12	I/O	NV _{DD}	_
PCI_AD28	AD10	I/O	NV _{DD}	_
PCI_AD29	AC10	I/O	NV _{DD}	_
PCI_AD30	AF10	I/O	NV _{DD}	_
PCI_AD31	AF8	I/O	NV _{DD}	_
PCI_C/BE0	AC19	I/O	NV _{DD}	
PCI_C/BE1	AB15	I/O	NV _{DD}	_
PCI_C/BE2	AF14	I/O	NV _{DD}	
PCI_C/BE3	AF11	I/O	NV _{DD}	
PCI_PAR	AD16	I/O	NV _{DD}	—
PCI_FRAME	AF16	I/O	NV_{DD}	5

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)



Table 62. MPC8313E T	FEPBGAll Pinout	Listing (continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Note
TSEC1_TXD1/TSEC_1588_PP2	AD6	0	LV _{DDB}	
TSEC1_TXD0/USBDR_STP/TSEC_1588_PP3	AD5	0	LV _{DDB}	_
TSEC1_TX_EN/TSEC_1588_ALARM1	AB7	0	LV _{DDB}	_
TSEC1_TX_ER/TSEC_1588_ALARM2	AB8	0	LV _{DDB}	
TSEC1_GTX_CLK125	AE1	I	LV _{DDB}	
TSEC1_MDC/LB_POR_CFG_BOOT_ECC_DIS	AF6	0	NV _{DD}	9, 11
TSEC1_MDIO	AB9	I/O	NV _{DD}	_
	ETSEC2			
TSEC2_COL/GTM1_TIN4/GTM2_TIN3/GPIO15	AB4	I/O	LV _{DDA}	_
TSEC2_CRS/GTM1_TGATE4/GTM2_TGATE3/GPIO16	AB3	I/O	LV _{DDA}	
TSEC2_GTX_CLK/GTM1_TOUT4/GTM2_TOUT3/GPIO17	AC1	I/O	LV _{DDA}	12
TSEC2_RX_CLK/GTM1_TIN2/GTM2_TIN1/GPIO18	AC2	I/O	LV _{DDA}	
TSCE2_RX_DV/GTM1_TGATE2/GTM2_TGATE1/GPIO19	AA3	I/O	LV _{DDA}	
TSEC2_RXD3/GPIO20	Y5	I/O	LV _{DDA}	
TSEC2_RXD2/GPIO21	AA4	I/O	LV _{DDA}	
TSEC2_RXD1/GPIO22	AB2	I/O	LV _{DDA}	
TSEC2_RXD0/GPIO23	AA5	I/O	LV _{DDA}	_
TSEC2_RX_ER/GTM1_TOUT2/GTM2_TOUT1/GPIO24	AA2	I/O	LV _{DDA}	_
TSEC2_TX_CLK/GPIO25	AB1	I/O	LV _{DDA}	
TSEC2_TXD3/CFG_RESET_SOURCE0	W3	I/O	LV _{DDA}	
TSEC2_TXD2/CFG_RESET_SOURCE1	Y1	I/O	LV _{DDA}	_
TSEC2_TXD1/CFG_RESET_SOURCE2	W5	I/O	LV _{DDA}	
TSEC2_TXD0/CFG_RESET_SOURCE3	Y3	I/O	LV _{DDA}	
TSEC2_TX_EN/GPIO26	AA1	I/O	LV _{DDA}	
TSEC2_TX_ER/GPIO27	W1	I/O	LV _{DDA}	
	SGMII PHY			
ТХА	U3	0		_
TXA	V3	0		_
RXA	U1	Ι		
RXA	V1	Ι		
ТХВ	P4	0		
ТХВ	N4	0		—



Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
	SPI			
SPIMOSI/GTM1_TIN3/GTM2_TIN4/GPIO28/LSRCID4	H1	I/O	NV _{DD}	_
SPIMISO/GTM1_TGATE3/GTM2_TGATE4/GPIO29/ LDVAL	НЗ	I/O	NV_{DD}	_
SPICLK/GTM1_TOUT3/GPIO30	G1	I/O	NV _{DD}	
SPISEL/GPIO31	G3	I/O	NV _{DD}	_
Power ar	nd Ground Supplies			
AV _{DD1}	F14	Power for e300 core APLL (1.0 V)	_	
AV _{DD2}	P21	Power for system APLL (1.0 V)	—	_
GV _{DD}	A2,A3,A4,A24,A25,B3, B4,B5,B12,B13,B20,B21, B24,B25,B26,D1,D2,D8, D9,D16,D17	Power for DDR1 and DDR2 DRAM I/O voltage (1.8/2.5 V)	_	_
LV _{DD}	D24,D25,G23,H23,R23, T23,W25,Y25,AA22,AC23	Power for local bus (3.3 V)	—	_
LV _{DDA}	W2,Y2	Power for eTSEC2 (2.5 V, 3.3 V)	—	_
LV _{DDB}	AC8,AC9,AE4,AE5	Power for eTSEC1/ USB DR (2.5 V, 3.3 V)	_	_
MV _{REF}	C14,D14	Reference voltage signal for DDR	—	_
NV _{DD}	G4,H4,L2,M2,AC16,AC17, AD25,AD26,AE12,AE13, AE20,AE21,AE24,AE25, AE26,AF24,AF25	Standard I/O voltage (3.3 V)	_	_
V _{DD}	K11,K12,K13,K14,K15, K16,L10,L17,M10,M17, N10,N17,U12,U13,	Power for core (1.0 V)	_	_
V _{DDC}	F6,F10,F19,K6,K10,K17, K21,P6,P10,P17,R10,R17, T10,T17,U10,U11,U14, U15,U16,U17,W6,W21, AA6,AA10,AA14,AA19	Internal core logic constant power (1.0 V)	_	_



20.3 Example Clock Frequency Combinations

This table shows several possible frequency combinations that can be selected based on the indicated input reference frequencies, with RCWLR[LBCM] = 0 and RCWLR[DDRCM] =1, such that the LBC operates with a frequency equal to the frequency of csb_clk and the DDR controller operates at twice the frequency of csb_clk .

						LBC(lbc_clk)			e	300 Co	ore(cor	e_clk)		
SYS_ CLK_IN/ PCI_CLK	SPMF ¹	VCOD ²	VCO ³	CSB (<i>csb_clk</i>) ⁴	DDR (ddr_clk)	/2	/4	/8	USB ref ⁵	× 1	× 1.5	× 2	× 2.5	× 3
25.0	6	2	600.0	150.0	300.0	_	37.5	18.8	Note ⁶	150.0	225	300	375	_
25.0	5	2	500.0	125.0	250.0	62.5	31.25	15.6	Note 6	125.0	188	250	313	375
33.3	5	2	666.0	166.5	333.0	_	41.63	20.8	Note 6	166.5	250	333	_	_
33.3	4	2	532.8	133.2	266.4	66.6	33.3	16.7	Note 6	133.2	200	266	333	400
48.0	3	2	576.0	144.0	288.0	_	36	18.0	48.0	144.0	216	288	360	_
66.7	2	2	533.4	133.3	266.7	66.7	33.34	16.7	Note 6	133.3	200	267	333	400

Note:

1. System PLL multiplication factor.

2. System PLL VCO divider.

3. When considering operating frequencies, the valid core VCO operating range of 400–800 MHz must not be violated.

4. Due to erratum eTSEC40, *csb_clk* frequencies of less than 133 MHz do not support gigabit Ethernet data rates. The core frequency must be 333 MHz for gigabit Ethernet operation. This erratum will be fixed in revision 2 silicon.

5. Frequency of USB PLL input reference.

6. USB reference clock must be supplied from a separate source as it must be 24 or 48 MHz, the USB reference must be supplied from a separate external source using USB_CLK_IN.

21 Thermal

This section describes the thermal specifications of the MPC8313E.

21.1 Thermal Characteristics

This table provides the package thermal characteristics for the 516, 27×27 mm TEPBGAII.

Table	69.	Package	Thermal	Characteristics	for	TEPBGAII
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Characteristic	Board Type	Symbol	TEPBGA II	Unit	Note
Junction-to-ambient natural convection	Single layer board (1s)	$R_{ ext{ heta}JA}$	25	°C/W	1, 2
Junction-to-ambient natural convection	Four layer board (2s2p)	$R_{ ext{ heta}JA}$	18	°C/W	1, 2, 3
Junction-to-ambient (@200 ft/min)	Single layer board (1s)	$R_{ hetaJMA}$	20	°C/W	1, 3
Junction-to-ambient (@200 ft/min)	Four layer board (2s2p)	$R_{ hetaJMA}$	15	°C/W	1, 3
Junction-to-board	_	$R_{ heta JB}$	10	°C/W	4



Table 69. Package Thermal Characteristics for TEPBGAII (continued)

Characteristic	Board Type	Symbol	TEPBGA II	Unit	Note
Junction-to-case	_	$R_{ ext{ heta}JC}$	8	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	7	°C/W	6

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

- 3. Per JEDEC JESD51-6 with the board horizontal.
- 4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- 6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

21.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

21.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 T_J = junction temperature (°C) T_A = ambient temperature for the package (°C) $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W) P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_I - T_A$) are possible.

21.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter



- Output signals on the SerDes interface are fed from the XPADV_{DD} power plane. Input signals and sensitive transceiver analog circuits are on the XCOREV_{DD} supply.
- Power: XPADV_{DD} consumes less than 300 mW; XCOREV_{DD} + SDAV_{DD} consumes less than 750 mW.

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8313E system, and the MPC8313E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , NV_{DD} , GV_{DD} , LV_{DD} , LV_{DDA} , and LV_{DDB} pin of the device. These decoupling capacitors should receive their power from separate V_{DD} , NV_{DD} , GV_{DD} , LV_{DDA} , LV_{DDB} , and VSS power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , NV_{DD} , GV_{DD} , LV_{DD} , LV_{DDA} , and LV_{DDB} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100 to 330 μ F (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (XCOREV_{DD} and XPADV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor from each SerDes supply (XCOREV_{DD} and XPADV_{DD}) to the board ground plane on each side of the device. This should be done for all SerDes supplies.



Table 73	. Document	Revision	History	(continued)
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Rev. Number	Date	Substantive Change(s)	
1	3/2008	 In Table 63, added LBC_PM_REF_10 & LSRCID3 as muxed with USBDR_PCTL1 In Table 63, added LSRCID2 as muxed with USBDR_PCTL0 In Table 63, added LSRCID0 as muxed with USBDR_PWRFAULT In Table 63, added LSRCID0 as muxed with USBDR_DRIVE_VBUS In Table 63, moved T1, U2,& V2 from V_{DD} to XCOREVDD. In Table 63, moved P2, R2, & T3 from V_{SS} to XCOREVSS. In Table 63, moved P3, & V4 from V_{DD} to XPADVDD. In Table 63, neved "Double with pad" for AV_{DD1} and AV_{DD2} and moved AV_{DD1} and AV_{DD2} to Power and Ground Supplies section In Table 63, added muxing in pinout to show new options for selecting IEEE 1588 functionality. Added footnote 8 In Table 63, updated muxing in pinout to show new LBC ECC boot enable control muxed with eTSEC1_MDC Added pin type information for power supplies. Removed N1 and N3 from Vss section of Table 63. Added Therm0 and Therm1 (N1 and N3, respectively). Added note 7 to state: "Internal thermally sensitive resistor value varies linearly with temperature. Useful for determining the junction temperature." In Table 65 corrected maximum frequency of Local Bus Frequency from "33–66" to 66 MHz In Table 65 corrected maximum frequency of PCI from "24–66" to 66 MHz Added "which is determined by RCWLR[COREPLL]," to the note in Section 20.2, "Core PLL Configuration" about the VCO divider. 	
0	6/2007	 Added "(VCOD)" next to VCO divider column in Table 68. Added footnote stating that core_clk frequency must not exceed its maximum, so 2.5:1 and 3:1 <i>core_clk:csb_clk</i> ratios are invalid for certain <i>csb_clk</i> values. In Table 69, notes were confusing. Added note 3 for VCO column, note 4 for CSB (<i>csb_clk</i>) column, note 5 for USB ref column, and note 6 to replace "Note 1". Clarified note 4 to explain erratum eTSEC40. In Table 69, updated note 6 to specify USB reference clock frequencies limited to 24 and 48 for rev. 2 silicon. Replaced Table 71 "Thermal Resistance for TEPBGAII with Heat Sink in Open Flow". Removed last row of Table 19. Removed last row of Table 19. Removed 200 MHz rows from Table 21 and Table 5. Changed VIH minimum spec from 2.0 to 2.1 for clock, PIC, JTAG, SPI, and reset pins in Table 9, Table 47, Table 54, Table 59, and Table 61. Added Figure 4 showing the DDR input timing diagram. In Table 19, removed "MDM" from the "MDQS-MDQ/MECC/MDM" text under the Parameter column for the tCISKEW parameter. MDM is an output signal and should be removed from the input AC timing spec table (tCISKEW). Added "and power" to rows 2 and 3 in Table 10 Added the sentence "Once both the power supplies" and PORESET to Section 2.2, "Power Sequencing," and Figure 3. In Figure 35, corrected "USB0_CLK/USB1_CLK/DR_CLK" with "USBDR_CLK" In Table 42, clarified that AC specs are for ULPI only. 	
0	6/2007	Initial release.	

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