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NXP USA Inc. - MPC8313ECZQADDC Datasheet



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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	267MHz
Co-Processors/DSP	Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8313eczqaddc

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1 Overview

The MPC8313E incorporates the e300c3 core, which includes 16 Kbytes of L1 instruction and data caches and on-chip memory management units (MMUs). The MPC8313E has interfaces to dual enhanced three-speed 10/100/1000 Mbps Ethernet controllers, a DDR1/DDR2 SDRAM memory controller, an enhanced local bus controller, a 32-bit PCI controller, a dedicated security engine, a USB 2.0 dual-role controller and an on-chip high-speed PHY, a programmable interrupt controller, dual I²C controllers, a 4-channel DMA controller, and a general-purpose I/O port. This figure shows a block diagram of the MPC8313E.



Figure 1. MPC8313E Block Diagram

The MPC8313E security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

1.1 MPC8313E Features

The following features are supported in the MPC8313E:

- Embedded PowerPCTM e300 processor core built on Power ArchitectureTM technology; operates at up to 333 MHz.
- High-performance, low-power, and cost-effective host processor
- DDR1/DDR2 memory controller—one 16-/32-bit interface at up to 333 MHz supporting both DDR1 and DDR2
- 16-Kbyte instruction cache and 16-Kbyte data cache, a floating point unit, and two integer units
- Peripheral interfaces such as 32-bit PCI interface with up to 66-MHz operation, 16-bit enhanced local bus interface with up to 66-MHz operation, and USB 2.0 (high speed) with an on-chip PHY.
- Security engine provides acceleration for control and data plane security protocols
- Power management controller for low-power consumption
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration



1.2 Serial Interfaces

The following interfaces are supported in the MPC8313E: dual UART, dual I²C, and an SPI interface.

1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE Std 802.11i®, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are as follows:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-224, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

1.4 DDR Memory Controller

The MPC8313E DDR1/DDR2 memory controller includes the following features:

- Single 16- or 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 333 MHz
- Support for two physical banks (chip selects), each bank independently addressable
- 64-Mbit to 2-Gbit (for DDR1) and to 4-Gbit (for DDR2) devices with x8/x16/x32 data ports (no direct x4 support)
- Support for one 16-bit device or two 8-bit devices on a 16-bit bus, or one 32-bit device or two 16-bit devices on a 32-bit bus
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

1.5 PCI Controller

The MPC8313E PCI controller includes the following features:

- PCI specification revision 2.3 compatible
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency



1.6 USB Dual-Role Controller

The MPC8313E USB controller includes the following features:

- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Compatible with Universal Serial Bus Specification, Rev. 2.0
- Supports operation as a stand-alone USB device
 - Supports one upstream facing port
 - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
 - Supports USB root hub with one downstream-facing port
 - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI + low pin interface (ULPI) or on-chip USB 2.0 full-speed/high-speed PHY

1.7 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8313E eTSECs include the following features:

- Two RGMII/SGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3®, 802.3u®, 802.3x®, 802.3z®, 802.3au®, and 802.3ab®
- Support for Wake-on-Magic Packet[™], a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status
- Three-speed support (10/100/1000 Mbps)
- On-chip high-speed serial interface to external SGMII PHY interface
- Support for IEEE Std 1588TM
- Support for two full-duplex FIFO interface modes
- Multiple PHY interface configuration
- TCP/IP acceleration and QoS features available
- IP v4 and IP v6 header recognition on receive
- IP v4 header checksum verification and generation
- TCP and UDP checksum verification and generation
- Per-packet configurable acceleration
- Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2[®], PPPoE session, MPLS stacks, and ESP/AH IP-security headers
- Transmission from up to eight physical queues.
- Reception to up to eight physical queues



1.10 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the MPC8313E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

1.11 DMA Controller, Dual I²C, DUART, Local Bus Controller, and Timers

The MPC8313E provides an integrated four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Supports misaligned transfers

There are two I²C controllers. These synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. The 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8313E local bus controller (LBC) port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The three user programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM or UPM controller. The FCM provides a glueless interface to parallel-bus NAND Flash E2PROM devices. The FCM contains three basic configuration register groups—BR*n*, OR*n*, and FMR. Both may exist in the same system. The local bus can operate at up to 66 MHz.

The MPC8313E system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8313E. The MPC8313E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.



Driver Type	Output Impedance (Ω)	Supply Voltage
DDR2 signal	18	GV _{DD} = 1.8 V
DUART, system control, I ² C, JTAG, SPI	42	NV _{DD} = 3.3 V
GPIO signals	42	NV _{DD} = 3.3 V
eTSEC signals	42	LV_{DDA} , LV_{DDB} = 2.5/3.3 V
USB signals	42	LV _{DDB} = 2.5/3.3 V

Table 3. Output Drive Capability (continued)

2.2 Power Sequencing

The MPC8313E does not require the core supply voltage (V_{DD} and V_{DDC}) and I/O supply voltages (GV_{DD} , LV_{DD} , and NV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD} and V_{DDC}) before the I/O voltage (GV_{DD} , LV_{DD} , and NV_{DD}) and assert PORESET before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating PORESET.

Note that there is no specific power down sequence requirement for the MPC8313E. I/O voltage supplies $(GV_{DD}, LV_{DD}, and NV_{DD})$ do not have any ordering requirements with respect to one another.



Figure 3. Power-Up Sequencing Example



6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) when $GV_{DD}(typ) = 1.8 \text{ V}.$

Parameter/Condition	Symbol	Min	Мах	Unit	Note
I/O supply voltage	GV _{DD}	1.7	1.9	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.125	GV _{DD} + 0.3	V	_
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.125	V	_
Output leakage current	I _{OZ}	-9.9	9.9	μΑ	4
Output high current ($V_{OUT} = 1.420 \text{ V}$)	I _{OH}	-13.4	—	mA	
Output low current (V _{OUT} = 0.280 V)	I _{OL}	13.4	_	mA	_

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

This table provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8$ V.

Table 13.	DDR2 SD	RAM Capa	citance for	GV _{DD} (tvp) =	1.8 V
				~ ` ```````````````````````````````````	

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, DQS	CIO	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	_	0.5	pF	1

Note:

1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when $GV_{DD}(typ) = 2.5 \text{ V}.$

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Note
I/O supply voltage	GV _{DD}	2.3	2.7	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.15	GV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.15	V	—



6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Rev. 1.0 Silicon

Parameter	Symbol ¹	Min	Мах	Unit	Note
MCK[<i>n</i>] cycle time, MCK[<i>n</i>]/MCK[<i>n</i>] crossing	t _{MCK}	6	10	ns	2
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz	^t DDKHAS	2.1 2.5	_	ns	3
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz	t _{ddkhax}	2.4 3.15		ns	3
MCS[<i>n</i>] output setup with respect to MCK 333 MHz 266 MHz	^t DDKHCS	2.4 3.15		ns	3
MCS[<i>n</i>] output hold with respect to MCK 333 MHz 266 MHz	^t DDKHCX	2.4 3.15	_	ns	3
MCK to MDQS Skew	t _{DDKHMH}	-0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS 333 MHz 266 MHz	^t DDKHDS, ^t DDKLDS	800 900	—	ps	5
MDQ//MDM output hold with respect to MDQS 333 MHz 266 MHz	^t DDKHDX, ^t DDKLDX	900 1100		ps	5
MDQS preamble start	t _{DDKHMP}	$-0.5\times t_{\text{MCK}}-0.6$	$-0.5 imes t_{MCK}$ + 0.6	ns	6
MDQS epilogue end	t _{DDKHME}	-0.6	0.6	ns	6

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 </sub>
- 2. All MCK/MCK referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ//MDM/MDQS.
- 4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual, for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.



This figure shows the MII receive AC timing diagram.



Figure 10. MII Receive AC Timing Diagram RMII AC Timing Specifications

8.2.1.3 RMII Transmit AC Timing Specifications

This table provides the RMII transmit AC timing specifications.

Table 28. RMII Transmit AC Timing Specifications

At recommended operating conditions with NV_{DD} of 3.3 V \pm 0.3 V.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
REF_CLK clock	t _{RMX}	_	20	_	ns
REF_CLK duty cycle	t _{RMXH/} t _{RMX}	35	_	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTKHDX}	2	_	10	ns
REF_CLK data clock rise $V_{IL}(min)$ to $V_{IH}(max)$	t _{RMXR}	1.0	_	4.0	ns
REF_CLK data clock fall $V_{IH}(max)$ to $V_{IL}(min)$	t _{RMXF}	1.0		4.0	ns

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first three letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{RMTKHDX} symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

This figure shows the RMII transmit AC timing diagram.



Figure 11. RMII Transmit AC Timing Diagram



Table 35. SGMII Receive AC Timing Specifications (continued)

At recommended operating conditions with XCOREV_{DD} = 1.0 V \pm 5%.

Parameter	Symbol	Min	Тур	Max	Unit	Note
Total jitter tolerance	JT	0.65	_	_	UI p-p	1
Bit error ratio	BER	_	_	10 ⁻¹²		
Unit interval	UI	799.92	800	800.08	ps	2
AC coupling capacitor	C _{TX}	5	_	200	nF	3

Notes:

1. Measured at receiver.

2. Each UI is 800 ps ± 100 ppm.

3. The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.



Figure 17. SGMII Receiver Input Compliance Mask



9 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

9.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 22 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TXn and \overline{TXn}) or a receiver input (RXn and \overline{RXn}). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-ended swing

The transmitter output signals and the receiver input signals TXn, \overline{TXn} , RXn, and \overline{RXn} each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

2. Differential output voltage, V_{OD} (or differential output swing):

The differential output voltage (or swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{TXn} - V_{\overline{TXn}}$. The V_{OD} value can be either positive or negative.

3. Differential input voltage, V_{ID} (or differential input swing):

The differential input voltage (or swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{RXn} - V_{\overline{RXn}}$. The V_{ID} value can be either positive or negative.

- 4. Differential peak voltage, V_{DIFFp} The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.
- 5. Differential peak-to-peak, V_{DIFFp-p}

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

6. Differential waveform

The differential waveform is constructed by subtracting the inverting signal (TX*n*, for example) from the non-inverting signal (TX*n*, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 22 as an example for differential waveform.

7. Common mode voltage, V_{cm}





Figure 25. Differential Reference Clock Input DC Requirements (External AC-Coupled)





9.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to XCOREV_{SS}, the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce a signal with too large of an amplitude and may need to be DC-biased at the clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC coupling.

NOTE

Figure 27 through Figure 30 are for conceptual reference only. Due to the fact that the clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is possible that the clock circuit reference designs provided by clock driver chip vendors are different from what is shown in the figures. They might also vary from one vendor to the other. Therefore, Freescale can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. It is recommended that the system designer contact the selected clock driver chip vendor for the optimal reference circuits for the MPC8313E SerDes reference clock receiver requirement provided in this document.



assumes that the LVPECL clock driver's output impedance is 50 Ω . R1 is used to DC-bias the LVPECL outputs prior to AC coupling. Its value could be ranged from 140 to 240 Ω depending on the clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50- Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8313E SerDes3 reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω . Consult with the clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.



Figure 29. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the MPC8313E SerDes reference clock input's DC requirement.



Figure 30. Single-Ended Connection (Reference Only)



This figure provides the boundary-scan timing diagram.



Figure 44. Boundary-Scan Timing Diagram

This figure provides the test access port timing diagram.



Figure 45. Test Access Port Timing Diagram



15.2 Timers AC Timing Specifications

This table provides the Timers input and output AC timing specifications.

Table 54. Timers Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
Timers inputs—minimum pulse width	t _{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.

2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

This figure provides the AC test load for the Timers.



Figure 51. Timers AC Test Load

16 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

16.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO when the GPIO pins are operating from a 3.3-V supply.

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	_	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V
Input high voltage	V _{IH}	—	2.0	NV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0~V \leq V_{IN} \leq NV_{DD}$	—	±5	μΑ

 Table 55. GPIO (When Operating at 3.3 V) DC Electrical Characteristics

Note:

1. This specification only applies to GPIO pins that are operating from a 3.3-V supply. See Table 62 for the power supply listed for the individual GPIO signal.



19.3 Pinout Listings

This table provides the pin-out listing for the MPC8313E, TEPBGAII package.

Signal	Package Pin Number	Pin Type	Power Supply	Note
DDR Memo	ry Controller Interface			
MEMC_MDQ0	A8	I/O	GV _{DD}	—
MEMC_MDQ1	A9	I/O	GV _{DD}	—
MEMC_MDQ2	C10	I/O	GV _{DD}	—
MEMC_MDQ3	C9	I/O	GV _{DD}	—
MEMC_MDQ4	E9	I/O	GV _{DD}	_
MEMC_MDQ5	E11	I/O	GV _{DD}	_
MEMC_MDQ6	E10	I/O	GV _{DD}	—
MEMC_MDQ7	C8	I/O	GV _{DD}	—
MEMC_MDQ8	E8	I/O	GV _{DD}	—
MEMC_MDQ9	A6	I/O	GV _{DD}	—
MEMC_MDQ10	B6	I/O	GV _{DD}	—
MEMC_MDQ11	C6	I/O	GV _{DD}	—
MEMC_MDQ12	C7	I/O	GV _{DD}	—
MEMC_MDQ13	D7	I/O	GV _{DD}	—
MEMC_MDQ14	D6	I/O	GV _{DD}	—
MEMC_MDQ15	A5	I/O	GV _{DD}	—
MEMC_MDQ16	A19	I/O	GV _{DD}	—
MEMC_MDQ17	D18	I/O	GV _{DD}	—
MEMC_MDQ18	A17	I/O	GV _{DD}	—
MEMC_MDQ19	E17	I/O	GV _{DD}	—
MEMC_MDQ20	E16	I/O	GV _{DD}	—
MEMC_MDQ21	C18	I/O	GV _{DD}	—
MEMC_MDQ22	D19	I/O	GV _{DD}	—
MEMC_MDQ23	C19	I/O	GV _{DD}	—
MEMC_MDQ24	E19	I/O	GV _{DD}	_
MEMC_MDQ25	A22	I/O	GV _{DD}	—
MEMC_MDQ26	C21	I/O	GV _{DD}	—
MEMC_MDQ27	C20	I/O	GV _{DD}	—
MEMC_MDQ28	A21	I/O	GV _{DD}	—

Table 62. MPC8313E TEPBGAII Pinout Listing



	Package Pin Number	Pin Type	Supply	Note
MEMC_MDQ29	A20	I/O	GV _{DD}	
MEMC_MDQ30	C22	I/O	GV _{DD}	
MEMC_MDQ31	B22	I/O	GV _{DD}	
MEMC_MDM0	B7	0	GV _{DD}	
MEMC_MDM1	E6	0	GV _{DD}	
MEMC_MDM2	E18	0	GV _{DD}	
MEMC_MDM3	E20	0	GV _{DD}	
MEMC_MDQS0	A7	I/O	GV _{DD}	
MEMC_MDQS1	E7	I/O	GV _{DD}	
MEMC_MDQS2	B19	I/O	GV _{DD}	
MEMC_MDQS3	A23	I/O	GV _{DD}	
MEMC_MBA0	D15	0	GV _{DD}	
MEMC_MBA1	A18	0	GV _{DD}	
MEMC_MBA2	A15 O		GV _{DD}	_
MEMC_MA0	E12 O		GV _{DD}	_
MEMC_MA1	D11	0	GV _{DD}	_
MEMC_MA2	B11	0	GV _{DD}	_
MEMC_MA3	A11	0	GV _{DD}	_
MEMC_MA4	A12	0	GV _{DD}	_
MEMC_MA5	E13	0	GV _{DD}	_
MEMC_MA6	C12	0	GV _{DD}	—
MEMC_MA7	E14	0	GV _{DD}	—
MEMC_MA8	B15	0	GV _{DD}	_
MEMC_MA9	C17	0	GV _{DD}	_
MEMC_MA10	C13	0	GV _{DD}	_
MEMC_MA11	A16	0	GV _{DD}	_
MEMC_MA12	C15	0	GV _{DD}	_
MEMC_MA13	C16	0	GV _{DD}	_
MEMC_MA14	E15	0	GV _{DD}	_
MEMC_MWE	B18	0	GV _{DD}	_
MEMC_MRAS	C11	0	GV _{DD}	_
MEMC_MCAS	B10	0	GV _{DD}	_

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)



Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LA14/TSEC_1588_TRIG1	L24	0	LV _{DD}	8
LA15/TSEC_1588_ALARM2	K26	0	LV _{DD}	8
	DUART		·	
UART_SOUT1/MSRCID0 N2 O N				
UART_SIN1/MSRCID1	M5	I/O	NV _{DD} —	
UART_CTS1/GPIO8/MSRCID2	M1	I/O	NV _{DD}	—
UART_RTS1/GPIO9/MSRCID3	K1	I/O N\		—
UART_SOUT2/MSRCID4/TSEC_1588_CLK	M3	0	NV _{DD}	8
UART_SIN2/MDVAL/TSEC_1588_GCLK	L1	I/O	NV _{DD}	8
UART_CTS2/TSEC_1588_PP1	L5	I/O	NV _{DD}	8
UART_RTS2/TSEC_1588_PP2	L3	I/O	NV _{DD}	8
ľ	² C interface		·	
IIC1_SDA/CKSTOP_OUT/TSEC_1588_TRIG1	J4	I/O	NV _{DD}	2, 8
IIC1_SCL/CKSTOP_IN/TSEC_1588_ALARM2	J2	I/O	NV _{DD}	2, 8
IIC2_SDA/PMC_PWR_OK/GPIO10	J3	I/O	NV _{DD} 2	
IIC2_SCL/GPIO11	H5	I/O	NV _{DD}	
	Interrupts			
MCP_OUT	G5	0	NV _{DD}	2
IRQ0/MCP_IN	K5	I	NV _{DD}	—
IRQ1	K4	I	NV _{DD}	—
IRQ2	K2	I	NV _{DD}	—
IRQ3/CKSTOP_OUT	К3	I/O	NV _{DD}	—
IRQ4/CKSTOP_IN/GPIO12	J1	I/O	NV _{DD}	—
Configuration				
CFG_CLKIN_DIV	D5	I	NV _{DD} —	
EXT_PWR_CTRL	J5	0	NV _{DD} —	
CFG_LBIU_MUX_EN	R24	I	NV _{DD}	—
JTAG				
ТСК	E1	I	NV _{DD}	_
TDI	E2	I	NV _{DD}	4
TDO	E3	O NV _E		3



Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_TRDY	AD13	I/O	NV _{DD}	5
PCI_IRDY	AC15	I/O	NV _{DD}	5
PCI_STOP	AF13	I/O	NV _{DD}	5
PCI_DEVSEL	AC14	I/O	NV _{DD}	5
PCI_IDSEL	AF20	I	NV _{DD}	—
PCI_SERR	AE15	I/O	NV _{DD}	5
PCI_PERR	AD15	I/O	NV _{DD}	5
PCI_REQ0	AB10	I/O	NV _{DD}	—
PCI_REQ1/CPCI_HS_ES	AD9	I	NV _{DD}	—
PCI_REQ2	AD8	I	NV _{DD}	—
PCI_GNT0	AC11	I/O	NV _{DD}	—
PCI_GNT1/CPCI_HS_LED	AE7	0	NV _{DD}	—
PCI_GNT2/CPCI_HS_ENUM	AD7	0	NV _{DD}	—
M66EN	AD21	I	NV _{DD}	—
PCI_CLK0	AF17	0	NV _{DD}	
PCI_CLK1	AB16	0	NV _{DD}	—
PCI_CLK2	AF18	0	NV _{DD}	—
PCI_PME	AD22	I/O	NV _{DD}	5
ETSEC1/_USBULPI				
TSEC1_COL/USBDR_TXDRXD0	AD2	I/O	I/O LV _{DDB}	
TSEC1_CRS/USBDR_TXDRXD1	AC3	I/O	LV _{DDB}	—
TSEC1_GTX_CLK/USBDR_TXDRXD2	AF3	I/O	LV _{DDB}	3, 12
TSEC1_RX_CLK/USBDR_TXDRXD3	AE3	I/O	LV _{DDB}	—
TSEC1_RX_DV/USBDR_TXDRXD4	AD3	I/O LV _{DD}		—
TSEC1_RXD3/USBDR_TXDRXD5	AC6	I/O LV _{DI}		—
TSEC1_RXD2/USBDR_TXDRXD6	AF4	I/O	LV _{DDB}	—
TSEC1_RXD1/USBDR_TXDRXD7	AB6	I/O	LV _{DDB}	—
TSEC1_RXD0/USBDR_NXT/TSEC_1588_TRIG1	AB5	I	LV _{DDB} —	
TSEC1_RX_ER/USBDR_DIR/TSEC_1588_TRIG2	AD4	I LV		—
TSEC1_TX_CLK/USBDR_CLK/TSEC_1588_CLK	AF5	I LV _I		—
TSEC1_TXD3/TSEC_1588_GCLK	AE6	0 L\		—
TSEC1_TXD2/TSEC_1588_PP1	AC7	0	LV _{DDB}	

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)



- Output signals on the SerDes interface are fed from the XPADV_{DD} power plane. Input signals and sensitive transceiver analog circuits are on the XCOREV_{DD} supply.
- Power: XPADV_{DD} consumes less than 300 mW; XCOREV_{DD} + SDAV_{DD} consumes less than 750 mW.

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8313E system, and the MPC8313E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , NV_{DD} , GV_{DD} , LV_{DD} , LV_{DDA} , and LV_{DDB} pin of the device. These decoupling capacitors should receive their power from separate V_{DD} , NV_{DD} , GV_{DD} , LV_{DDA} , LV_{DDB} , and VSS power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , NV_{DD} , GV_{DD} , LV_{DD} , LV_{DDA} , and LV_{DDB} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100 to 330 μ F (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (XCOREV_{DD} and XPADV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor from each SerDes supply (XCOREV_{DD} and XPADV_{DD}) to the board ground plane on each side of the device. This should be done for all SerDes supplies.



Table 73	. Document	Revision	History	(continued)
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Rev. Number	Date	Substantive Change(s)
1	3/2008	 In Table 63, added LBC_PM_REF_10 & LSRCID3 as muxed with USBDR_PCTL1 In Table 63, added LSRCID2 as muxed with USBDR_PCTL0 In Table 63, added LSRCID0 as muxed with USBDR_PWRFAULT In Table 63, added LSRCID0 as muxed with USBDR_DRIVE_VBUS In Table 63, moved T1, U2,& V2 from V_{DD} to XCOREVDD. In Table 63, moved P2, R2, & T3 from V_{SS} to XCOREVSS. In Table 63, moved P3, & V4 from V_{DD} to XPADVDD. In Table 63, neved "Double with pad" for AV_{DD1} and AV_{DD2} and moved AV_{DD1} and AV_{DD2} to Power and Ground Supplies section In Table 63, added muxing in pinout to show new options for selecting IEEE 1588 functionality. Added footnote 8 In Table 63, updated muxing in pinout to show new LBC ECC boot enable control muxed with eTSEC1_MDC Added pin type information for power supplies. Removed N1 and N3 from Vss section of Table 63. Added Therm0 and Therm1 (N1 and N3, respectively). Added note 7 to state: "Internal thermally sensitive resistor value varies linearly with temperature. Useful for determining the junction temperature." In Table 65 corrected maximum frequency of Local Bus Frequency from "33–66" to 66 MHz In Table 65 corrected maximum frequency of PCI from "24–66" to 66 MHz Added "which is determined by RCWLR[COREPLL]," to the note in Section 20.2, "Core PLL Configuration" about the VCO divider.
0	6/2007	 Added "(VCOD)" next to VCO divider column in Table 68. Added footnote stating that core_clk frequency must not exceed its maximum, so 2.5:1 and 3:1 <i>core_clk:csb_clk</i> ratios are invalid for certain <i>csb_clk</i> values. In Table 69, notes were confusing. Added note 3 for VCO column, note 4 for CSB (<i>csb_clk</i>) column, note 5 for USB ref column, and note 6 to replace "Note 1". Clarified note 4 to explain erratum eTSEC40. In Table 69, updated note 6 to specify USB reference clock frequencies limited to 24 and 48 for rev. 2 silicon. Replaced Table 71 "Thermal Resistance for TEPBGAII with Heat Sink in Open Flow". Removed last row of Table 19. Removed last row of Table 19. Removed 200 MHz rows from Table 21 and Table 5. Changed VIH minimum spec from 2.0 to 2.1 for clock, PIC, JTAG, SPI, and reset pins in Table 9, Table 47, Table 54, Table 59, and Table 61. Added Figure 4 showing the DDR input timing diagram. In Table 19, removed "MDM" from the "MDQS-MDQ/MECC/MDM" text under the Parameter column for the tCISKEW parameter. MDM is an output signal and should be removed from the input AC timing spec table (tCISKEW). Added "and power" to rows 2 and 3 in Table 10 Added the sentence "Once both the power supplies" and PORESET to Section 2.2, "Power Sequencing," and Figure 3. In Figure 35, corrected "USB0_CLK/USB1_CLK/DR_CLK" with "USBDR_CLK" In Table 42, clarified that AC specs are for ULPI only.
0	6/2007	Initial release.