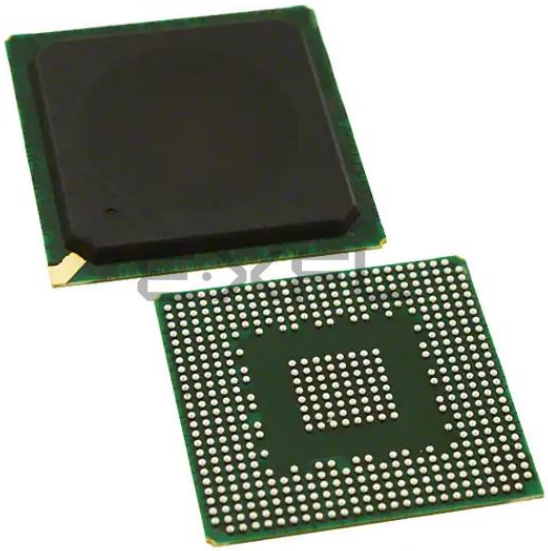

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

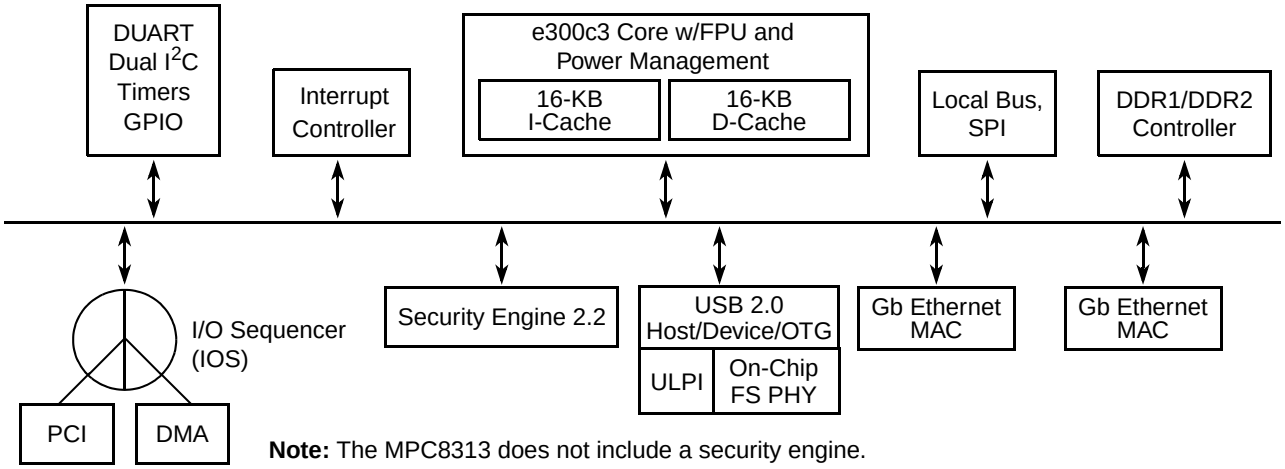
Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8313eczqaff

1 Overview

The MPC8313E incorporates the e300c3 core, which includes 16 Kbytes of L1 instruction and data caches and on-chip memory management units (MMUs). The MPC8313E has interfaces to dual enhanced three-speed 10/100/1000 Mbps Ethernet controllers, a DDR1/DDR2 SDRAM memory controller, an enhanced local bus controller, a 32-bit PCI controller, a dedicated security engine, a USB 2.0 dual-role controller and an on-chip high-speed PHY, a programmable interrupt controller, dual I^2C controllers, a 4-channel DMA controller, and a general-purpose I/O port. This figure shows a block diagram of the MPC8313E.



Note: The MPC8313 does not include a security engine.

Figure 1. MPC8313E Block Diagram

The MPC8313E security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

1.1 MPC8313E Features

The following features are supported in the MPC8313E:

- Embedded PowerPC™ e300 processor core built on Power Architecture™ technology; operates at up to 333 MHz.
- High-performance, low-power, and cost-effective host processor
- DDR1/DDR2 memory controller—one 16-/32-bit interface at up to 333 MHz supporting both DDR1 and DDR2
- 16-Kbyte instruction cache and 16-Kbyte data cache, a floating point unit, and two integer units
- Peripheral interfaces such as 32-bit PCI interface with up to 66-MHz operation, 16-bit enhanced local bus interface with up to 66-MHz operation, and USB 2.0 (high speed) with an on-chip PHY.
- Security engine provides acceleration for control and data plane security protocols
- Power management controller for low-power consumption
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration

This table provides the input AC timing specifications for the DDR SDRAM when GV_{DD}(typ) = 2.5 V.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	—

This table provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions. with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ	t_{CISKEW}	—	—	ps	1, 2
333 MHz	—	–750	750	—	—
266 MHz	—	–750	750	—	—

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[*n*] and any corresponding bit that is captured with MDQS[*n*]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

This figure illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

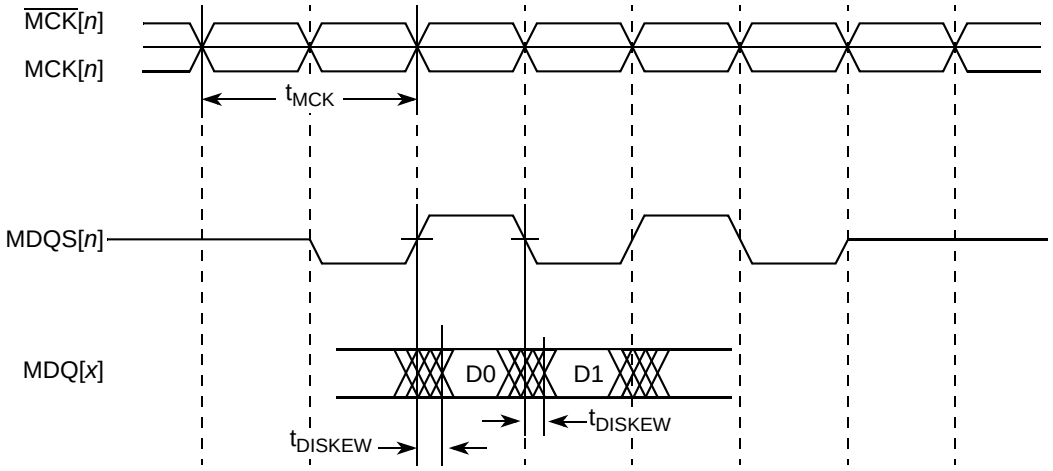


Figure 4. DDR Input Timing Diagram

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Rev. 1.0 Silicon

Parameter	Symbol [1]	Min	Max	Unit	Note
MCK[*n*] cycle time, MCK[*n*]/$\overline{\text{MCK}}$[*n*] crossing	t_{MCK}	6	10	ns	2
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz	t_{DDKHAS}	 2.1 2.5	 — —	ns	3
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz	t_{DDKHAX}	 2.4 3.15	 — —	ns	3
$\overline{\text{MCS}}$[*n*] output setup with respect to MCK 333 MHz 266 MHz	t_{DDKHCS}	 2.4 3.15	 — —	ns	3
$\overline{\text{MCS}}$[*n*] output hold with respect to MCK 333 MHz 266 MHz	t_{DDKHCX}	 2.4 3.15	 — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS 333 MHz 266 MHz	t_{DDKHDS}, t_{DDKLDS}	 800 900	 — —	ps	5
MDQ//MDM output hold with respect to MDQS 333 MHz 266 MHz	t_{DDKHDX}, t_{DDKLDX}	 900 1100	 — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

This figure shows the MII receive AC timing diagram.

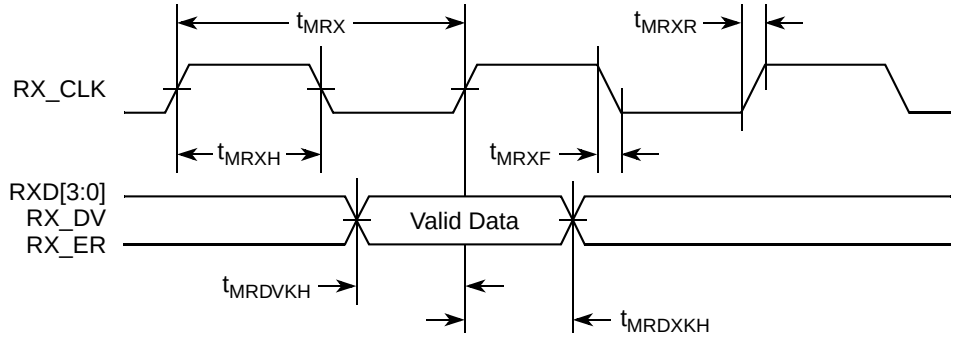


Figure 10. MII Receive AC Timing Diagram RMII AC Timing Specifications

8.2.1.3 RMII Transmit AC Timing Specifications

This table provides the RMII transmit AC timing specifications.

Table 28. RMII Transmit AC Timing Specifications

At recommended operating conditions with NV_{DD} of 3.3 V ± 0.3 V.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	10	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

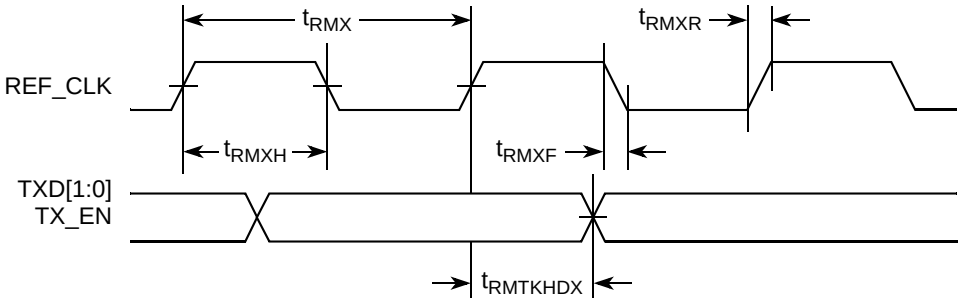


Figure 11. RMII Transmit AC Timing Diagram

8.2.1.4 RMII Receive AC Timing Specifications

This table provides the RMII receive AC timing specifications.

Table 29. RMII Receive AC Timing Specifications

At recommended operating conditions with NV_{DD} of 3.3 V ± 0.3 V.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This table provides the AC test load.

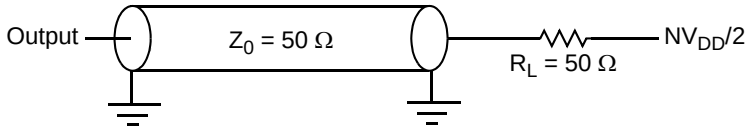


Figure 12. AC Test Load

This table shows the RMII receive AC timing diagram.

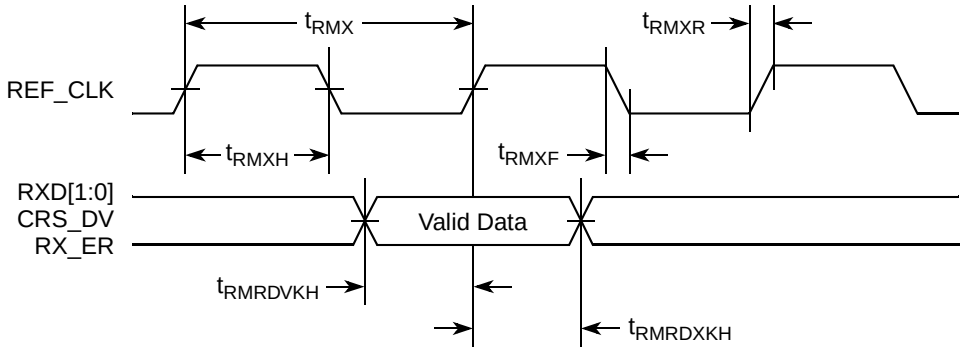


Figure 13. RMII Receive AC Timing Diagram

Table 33. SGMII DC Receiver Electrical Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Common mode input voltage	V_{CM}	—	$V_{xcorevss}$	—	V	4

Notes:
1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak to peak input differential voltage
3. $V_{CM\_ACp\text{-}p}$ is also referred to as peak to peak AC common mode voltage.
4. On-chip termination to $XCOREV_{SS}$.

8.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (TX[*n*] and $\overline{\text{TX}}$[*n*]) or at the receiver inputs (RX[*n*] and $\overline{\text{RX}}$[*n*]) as depicted in Figure 18, respectively.

8.3.4.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 34. SGMII Transmit AC Timing Specifications

At recommended operating conditions with $XCOREV_{DD}$ = 1.0 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter	JD	—	—	0.17	UI p-p	
Total jitter	JT	—	—	0.35	UI p-p	
Unit interval	UI	799.92	800	800.08	ps	1
V_{OD} fall time (80%–20%)	tfall	50	—	120	ps	
V_{OD} rise time (20%–80%)	t_{rise}	50	—	120	ps	

Note:
1. Each UI is 800 ps ± 100 ppm.

8.3.4.2 SGMII Receive AC Timing Specifications

This table provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 17 shows the SGMII receiver input compliance mask eye diagram.

Table 35. SGMII Receive AC Timing Specifications

At recommended operating conditions with $XCOREV_{DD}$ = 1.0 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter tolerance	JD	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal jitter tolerance	JSIN	0.1	—	—	UI p-p	1

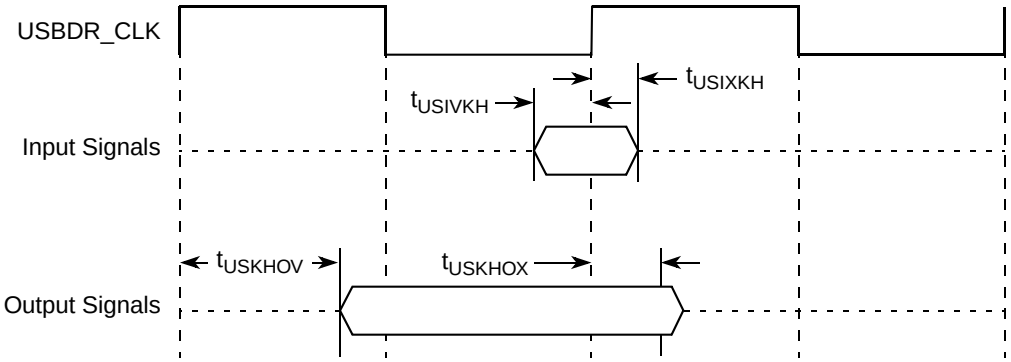


Figure 35. USB Signals

10.2 On-Chip USB PHY

This section describes the DC and AC electrical specifications for the on-chip USB PHY of the MPC8313E. See Chapter 7 in the *USB Specifications Rev. 2*, for more information.

This table provides the USB clock input (USB_CLK_IN) DC timing specifications.

Table 42. USB_CLK_IN DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2.7	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	–0.3	0.4	V

This table provides the USB clock input (USB_CLK_IN) AC timing specifications.

Table 43. USB_CLK_IN AC Timing Specifications

Parameter/Condition	Conditions	Symbol	Min	Typ	Max	Unit
Frequency range	—	$f_{USB\_CLK\_IN}$	—	24	48	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	–0.005	0	0.005	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/time interval error	Peak-to-peak value measured with a second order high-pass filter of 500 kHz bandwidth	t_{CLK_PJ}	—	—	200	ps

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE Std 1149.1 (JTAG) interface.

Table 46. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

12.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std 1149.1 (JTAG) interface. This table provides the JTAG AC timing specifications as defined in Figure 41 through Figure 45.

Table 47. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5

Table 49. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 48).

Parameter	Symbol[1]	Min	Max	Unit
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0[2]	 — 0.9[3]	µs
Fall time of both SDA and SCL signals[5]	t_{I2CF}	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times NV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times NV_{DD}$	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The MPC8313E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5. The MPC8313E does not follow the *I²C-BUS Specifications, Version 2.1,* regarding the t_{I2CF} AC parameter.

This figure provides the AC test load for the I²C.

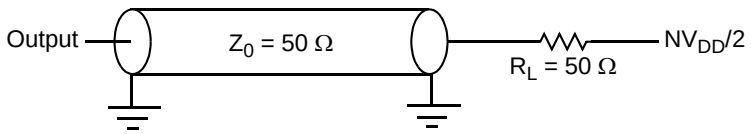


Figure 46. I²C AC Test Load

This figure shows the PCI input AC timing conditions.

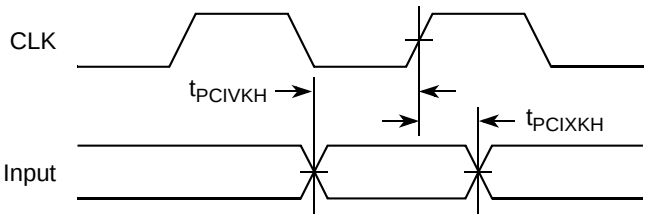


Figure 49. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

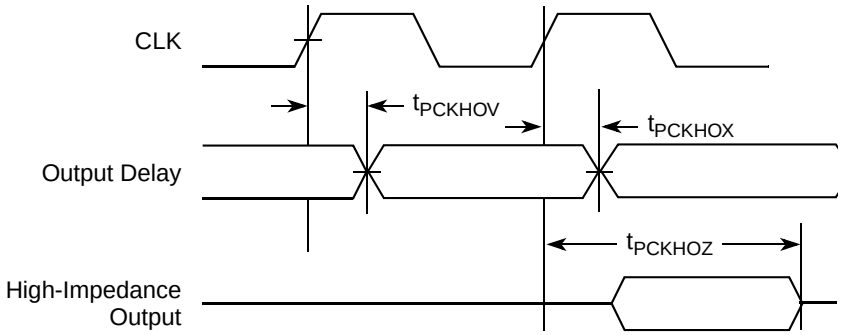


Figure 50. PCI Output AC Timing Measurement Condition

15 Timers

This section describes the DC and AC electrical specifications for the timers.

15.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the MPC8313E timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 53. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	±5	μA

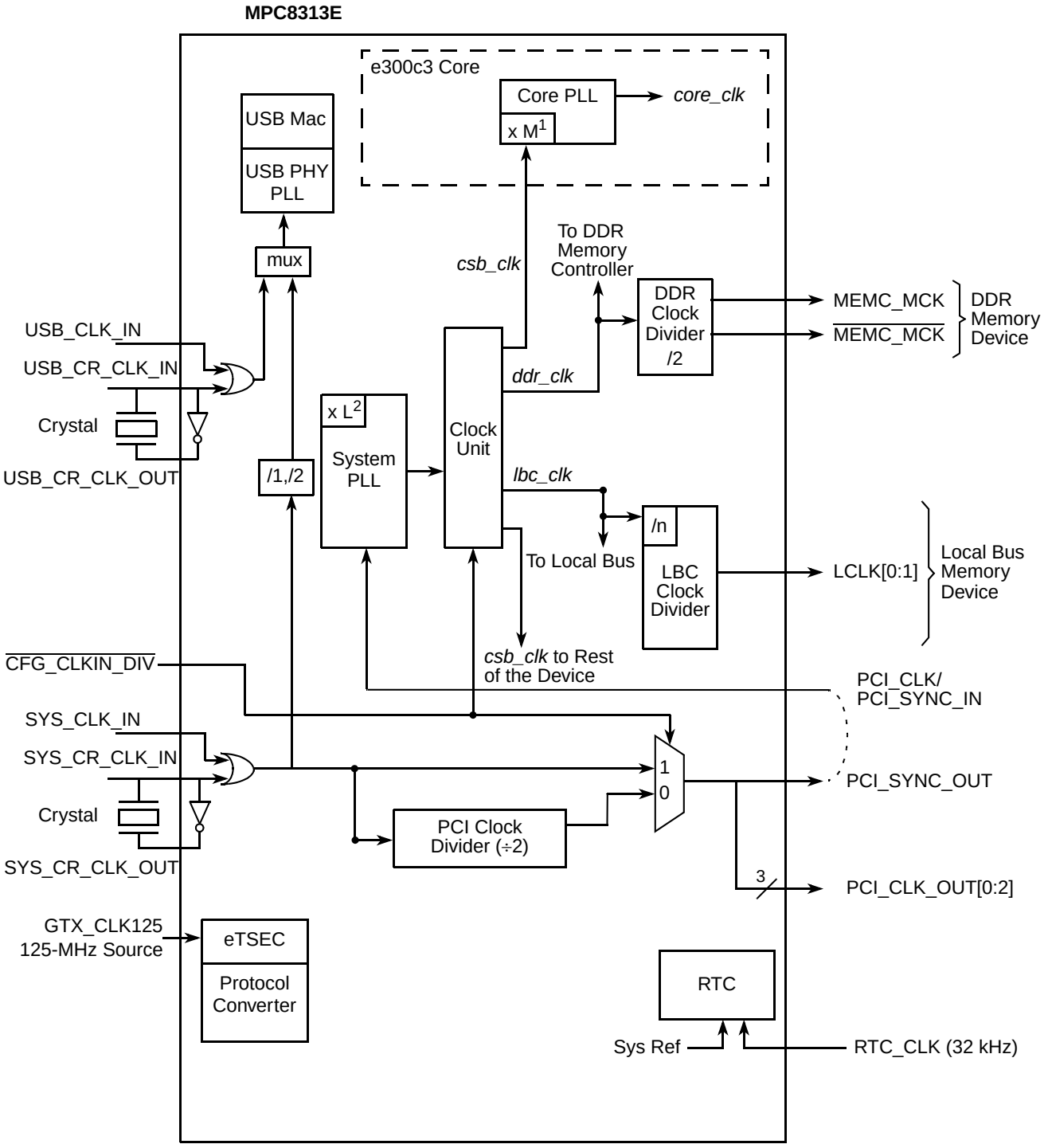
Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
V_{SS}	B1,B2,B8,B9,B16,B17,C1, C2,C3,C4,C5,C24,C25, C26,D3,D4,D12,D13,D20, D21,F8,F11,F13,F16,F17, F21,G2,G25,H2,H6,H21, H25,L4,L6,L11,L12,L13, L14,L15,L16,L21,L23,M4, M11,M12,M13,M14,M15, M16,M23,N6,N11,N12, N13,N14,N15,N16, N21,N23,P11,P12,P13, P14,P15,P16,P23,P25, R11,R12,R13,R14,R15, R16,R25,T6,T11,T12,T13, T14,T15,T16,T21,T25,U5, U6,U21,W4,W23,Y4,Y23, AA8,AA11,AA13,AA16, AA17,AA21,AC4,AC5, AC12,AC13,AC20,AC21, AD1,AE2,AE8,AE9,AE16, AE17,AF2	—	—	—
$XCOREV_{DD}$	T1,U2,V2	Core power for SerDes transceivers (1.0 V)	—	—
$XCOREV_{SS}$	P2,R2,T3	—	—	—
$XPADV_{DD}$	P5,U4	Pad power for SerDes transceivers (1.0 V)	—	—
$XPADV_{SS}$	P3,V4	—	—	—

Notes:
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NV_{DD}.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. This pin must always be tied to V_{SS}.
7. Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.
8. 1588 signals are available on these pins only in MPC8313 Rev 2.x or later.
9. LB_POR_CFG_BOOT_ECC_DIS is available only in MPC8313 Rev 2.x or later.
10. This pin has an internal pull-up.
11. This pin has an internal pull-down.
12. In MII mode, GTX_CLK should be pulled down by 300Ω to V_{SS}.

20 Clocking

This figure shows the internal distribution of clocks within the MPC8313E.



1 Multiplication factor M = 1, 1.5, 2, 2.5, and 3. Value is decided by RCWLR[COREPLL].
2 Multiplication factor L = 2, 3, 4, 5, and 6. Value is decided by RCWLR[SPMF].

Figure 57. MPC8313E Clock Subsystem

Table 63. Configurable Clock Units

Unit	Default Frequency	Options
TSEC1	*csb_clk*	Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3
TSEC2	*csb_clk*	Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3
Security Core, I^2C, SAP, TPR	*csb_clk*	Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3
USB DR	*csb_clk*	Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3
PCI and DMA complex	*csb_clk*	Off, *csb_clk*

This table provides the operating frequencies for the MPC8313E TEPBGAII under recommended operating conditions (see Table 2).

Table 64. Operating Frequencies for TEPBGAII

Characteristic[1]	Maximum Operating Frequency	Unit
e300 core frequency (*core_clk*)	333	MHz
Coherent system bus frequency (*csb_clk*)	167	MHz
DDR1/2 memory bus frequency (MCK)[2]	167	MHz
Local bus frequency (LCLK*n*)[3]	66	MHz
PCI input frequency (SYS_CLK_IN or PCI_CLK)	66	MHz

Note:

1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK[0:1], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM] and SCCR[USBDRCM] must be programmed such that the maximum internal operating frequency of the security core and USB modules do not exceed their respective value listed in this table.
2. The DDR data rate is 2x the DDR memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbc_clk* frequency (depending on LCRR[CLKDIV]), which is in turn, 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

20.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. This table shows the multiplication factor encodings for the system PLL.

Table 65. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)
T_B = board temperature at the package perimeter (°C)
$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51–8
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

21.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)
T_T = thermocouple temperature on top of package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

21.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to- ambient thermal resistance (°C/W)

Heat sink Vendors include the following list:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-2800

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Corporate Center PO BOX 994 Midland, MI 48686-0994 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

21.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

21.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction to case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)
T_C = case temperature of the package
$R_{\theta JC}$ = junction-to-case thermal resistance
P_D = power dissipation

22 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8313E SYS_CLK_IN

22.1 System Clocking

The MPC8313E includes three PLLs.

1. The platform PLL (AV_{DD2}) generates the platform clock from the externally supplied SYS_CLK_IN input in PCI host mode or SYS_CLK_IN/PCI_SYNC_IN in PCI agent mode. The frequency ratio between the platform and SYS_CLK_IN is selected using the platform PLL ratio configuration bits as described in Section 20.1, “System PLL Configuration.”
2. The e300 core PLL (AV_{DD1}) generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 20.2, “Core PLL Configuration.”
3. There is a PLL for the SerDes block.

- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

22.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA}, or LV_{DDB} as required. Unused active high inputs should be connected to V_{SS}. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA}, LV_{DDB}, and V_{SS} pins of the device.

22.6 Output Buffer DC Impedance

The MPC8313E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to NV_{DD} or V_{SS}. Then, the value of each resistor is varied until the pad voltage is $NV_{DD}/2$ (see Figure 60). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $NV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

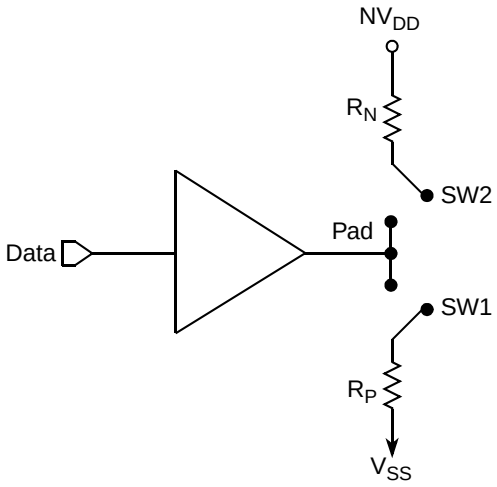


Figure 60. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

24 Revision History

This table summarizes a revision history for this document.

Table 73. Document Revision History

Rev. Number	Date	Substantive Change(s)
4	11/2011	• In Table 2, added following notes: – Note 3: Min temperature is specified with T_A; Max temperature is specified with T_J – Note 4: All Power rails must be connected and power applied to the MPC8313 even if the IP interfaces are not used. – Note 5: All I/O pins should be interfaced with peripherals operating at same voltage level. – Note 6: This voltage is the input to the filter discussed in Section 22.2, “PLL Power Supply Filtering.” and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter • Decoupled PCI_CLK and SYS_CLK_IN rise and fall times in Table 8. Relaxed maximum rise/fall time of SYS_CLK_IN to 4ns. • Added a note in Table 27 stating “The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm." • In Table 30: – Changed max value of t_{skrgt} in “Data to clock input skew (at receiver)” row from 2.8 to 2.6. – Added Note 7, stating that, “The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm.” • Added a note stating “eTSEC should be interfaced with peripheral operating at same voltage level” in Section 8.1.1, “TSEC DC Electrical Characteristics.” • TSEC1_MDC and TSEC_MDIO are powered at 3.3V by NVDD. Replaced LVDDA/LVDDB with NVDD and removed instances of 2.5V at several places in Section 8.5, “Ethernet Management Interface Electrical Characteristics.” • In Table 43, changed min/max values of t_{CLK_TOL} from 0.05 to 0.005. • In Table 62: – Added Note 2 for LGPL4 in showing LGPL4 as open-drain. – Removed Note 2 from TSEC1_MDIO. – Added Note 10: This pin has an internal pull-up. – Added Note 11: This pin has an internal pull-down. – Added Note 12: “In MII mode, GTX_CLK should be pulled down by 300 Ω to V_{SS}” to TSEC1_GTX_CLK and TSEC2_GTX_CLK. • In Section 19.1, “Package Parameters for the MPC8313E TEPBGAII,” replaced "5.5 Sn/0.5 Cu/4 Ag" with "Sn/3.5 Ag." • Added foot note 3 in Table 65 stating “The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.” • In Table 72: – Added AD = 266 and D = 266. – Added “C = 2.2” in “Revision level” column. – Added Note 4. • Changed resitor from 1.0 Ω to 10 Ω in Figure 58. • Replaced LCCR with LCRR throughout. • Added high-speed to USB Phy description.
3	01/2009	• Table 72, in column aa, changed to AG = 400 MHz.
2.2	12/2008	• Made cross-references active for sections, figures, and tables.
2.1	12/2008	• Added Figure 2, after Table 2 and renumbered the following figures.

Table 73. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
2	10/2008	• Added Note “The information in this document is accurate for revision 1.0, and 2.x and later. See Section 24.1, “Part Numbers Fully Addressed by this Document,” before Section 1, “Overview.” • Added part numbering details for all the silicon revisions in Table 74. • Changed V_{IH} from 2.7 V to 2.4 V in Table 7. • Added a row for V_{IH} level for Rev 2.x or later in Table 45. • Added a column for maximum power dissipation in low power mode for Rev 2.x or later silicon in Table 6. • Added a column for Power Nos for Rev 2.x or later silicon and added a row for 400 MHz in Table 4. • Removed footnote, “These are preliminary estimates.” from Table 4. • Added Table 21 for DDR AC Specs on Rev 2.x or later silicon. • Added Section 9, “High-Speed Serial Interfaces (HSSI).” • Added $\overline{\text{LFWE}}$, LFCLE, LFALE, $\overline{\text{LOE}}$, $\overline{\text{LFRE}}$, $\overline{\text{LFWP}}$, $\overline{\text{LGTA}}$, LUPWAIT, and $\overline{\text{LFRB}}$ in Table 63. • In Table 39, added note 2: “This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)” • Removed mentions of SGMII (SGMII has separate specs) from Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics.” • Corrected Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics,” to state that RGMII/RTBI interfaces only operate at 2.5 V, not 3.3 V. • Added ZQ package to ordering information In Table 74 and Section 19.1, “Package Parameters for the MPC8313E TEPBGAII” (applicable to both silicon rev. 1.0 and 2.1) • Removed footnotes 5 and 6 from Table 1 (left over when the PCI undershoot/overshoot voltages and maximum AC waveforms were removed from Section 2.1.2, “Power Supply Voltage Specification”). • Removed SD_PLL_TPD (T2) and SD_PLL_TPA_ANA (R4) from Table 63. • Added Section 8.3, “SGMII Interface Electrical Characteristics.” Removed Section 8.5.3 SGMII DC Electrical Characteristics. • Removed “HRESET negation to SRESET negation (output)” spec and changed “HRESET/SRESET assertion (output)” spec to “HRESET assertion (output)” in Table 10. • Clarified POR configuration signal specs to “Time for the device to turn off POR configuration signal drivers with respect to the assertion of HRESET” and “Time for the device to turn on POR configuration signal drivers with respect to the negation of HRESET” in Table 10. • Added Section 24.2, “Part Marking,” and Figure 62.

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