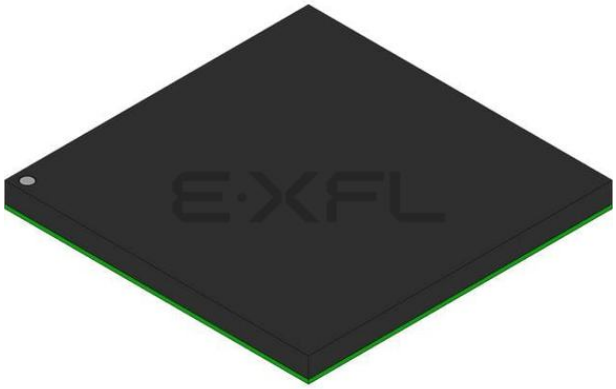

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300c3 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 333MHz |
| Co-Processors/DSP | Security; SEC 2.2 |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | USB 2.0 + PHY (1) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | Cryptography |
| Package / Case | 516-BBGA Exposed Pad |
| Supplier Device Package | 516-TEPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8313eczqaffb |

## 1.6 USB Dual-Role Controller

The MPC8313E USB controller includes the following features:

- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Compatible with *Universal Serial Bus Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI + low pin interface (ULPI) or on-chip USB 2.0 full-speed/high-speed PHY

## 1.7 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8313E eTSECs include the following features:

- Two RGMII/SGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3®, 802.3u®, 802.3x®, 802.3z®, 802.3au®, and 802.3ab®
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status
- Three-speed support (10/100/1000 Mbps)
- On-chip high-speed serial interface to external SGMII PHY interface
- Support for IEEE Std 1588™
- Support for two full-duplex FIFO interface modes
- Multiple PHY interface configuration
- TCP/IP acceleration and QoS features available
- IP v4 and IP v6 header recognition on receive
- IP v4 header checksum verification and generation
- TCP and UDP checksum verification and generation
- Per-packet configurable acceleration
- Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2®, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
- Transmission from up to eight physical queues.
- Reception to up to eight physical queues

- Full and half-duplex Ethernet support (1000 Mbps supports only full-duplex):
  - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE 802.1 virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision
  - CRC generation and verification of inbound/outbound packets
  - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
  - Exact match on primary and virtual 48-bit unicast addresses
    - VRRP and HSRP support for seamless router fail-over
  - Up to 16 exact-match MAC addresses supported
  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status

## 1.8 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model supports 5 external and 34 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

## 1.9 Power Management Controller (PMC)

The MPC8313E power management controller includes the following features:

- Provides power management when the device is used in both host and agent modes
- Supports PCI power management 1.2 D0, D1, D2, D3hot, and D3cold states
- On-chip split power supply controlled through external power switch for minimum standby power
- Support for PME generation in PCI agent mode, PME detection in PCI host mode
- Supports wake-up from Ethernet (Magic Packet), USB, GPIO, and PCI (PME input as host)

## 1.10 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the MPC8313E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

## 1.11 DMA Controller, Dual $I^2C$, DUART, Local Bus Controller, and Timers

The MPC8313E provides an integrated four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Supports misaligned transfers

There are two $I^2C$ controllers. These synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. The 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8313E local bus controller (LBC) port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The three user programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM or UPM controller. The FCM provides a glueless interface to parallel-bus NAND Flash E2PROM devices. The FCM contains three basic configuration register groups—BR*n*, OR*n*, and FMR. Both may exist in the same system. The local bus can operate at up to 66 MHz.

The MPC8313E system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

# 2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8313E. The MPC8313E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

## 4.2 AC Electrical Characteristics

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the system clock input (SYS_CLK_IN/PCI_CLK) AC timing specifications for the MPC8313E.

**Table 8. SYS_CLK_IN AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| SYS_CLK_IN/PCI_CLK frequency | $f_{SYS\_CLK\_IN}$ | 24 | — | 66.67 | MHz | 1 |
| SYS_CLK_IN/PCI_CLK cycle time | $t_{SYS\_CLK\_IN}$ | 15 | — | — | ns | — |
| SYS_CLK_IN rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | 0.8 | 4 | ns | 2 |
| PCI_CLK rise and fall time | $t_{PCH}$, $t_{PCL}$ | 0.6 | 0.8 | 1.2 | ns | 2 |
| SYS_CLK_IN/PCI_CLK duty cycle | $t_{KHK}/t_{SYS\_CLK\_IN}$ | 40 | — | 60 | % | 3 |
| SYS_CLK_IN/PCI_CLK jitter | — | — | — | ±150 | ps | 4, 5 |

**Notes:**
1. **Caution:** The system, core, security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN/PCI_CLK are measured at 0.4 and 2.4 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.

# 5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8313E.

## 5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins.

**Table 9. RESET Pins DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 2.1 | $NV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le NV_{DD}$ | — | ±5 | μA |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |

## 6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

**Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Rev. 1.0 Silicon**

| Parameter | Symbol [1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| MCK[*n*] cycle time, MCK[*n*]/$\overline{\text{MCK}}$[*n*] crossing | $t_{MCK}$ | 6 | 10 | ns | 2 |
| ADDR/CMD output setup with respect to MCK<br>333 MHz<br>266 MHz | $t_{DDKHAS}$ | <br>2.1<br>2.5 | <br>—<br>— | ns | 3 |
| ADDR/CMD output hold with respect to MCK<br>333 MHz<br>266 MHz | $t_{DDKHAX}$ | <br>2.4<br>3.15 | <br>—<br>— | ns | 3 |
| $\overline{\text{MCS}}$[*n*] output setup with respect to MCK<br>333 MHz<br>266 MHz | $t_{DDKHCS}$ | <br>2.4<br>3.15 | <br>—<br>— | ns | 3 |
| $\overline{\text{MCS}}$[*n*] output hold with respect to MCK<br>333 MHz<br>266 MHz | $t_{DDKHCX}$ | <br>2.4<br>3.15 | <br>—<br>— | ns | 3 |
| MCK to MDQS Skew | $t_{DDKHMH}$ | –0.6 | 0.6 | ns | 4 |
| MDQ//MDM output setup with respect to MDQS<br>333 MHz<br>266 MHz | $t_{DDKHDS}$, $t_{DDKLDS}$ | <br>800<br>900 | <br>—<br>— | ps | 5 |
| MDQ//MDM output hold with respect to MDQS<br>333 MHz<br>266 MHz | $t_{DDKHDX}$, $t_{DDKLDX}$ | <br>900<br>1100 | <br>—<br>— | ps | 5 |
| MDQS preamble start | $t_{DDKHMP}$ | $-0.5 \times t_{MCK} - 0.6$ | $-0.5 \times t_{MCK} + 0.6$ | ns | 6 |
| MDQS epilogue end | $t_{DDKHME}$ | –0.6 | 0.6 | ns | 6 |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that $t_{DDKHMH}$ follows the symbol conventions described in note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that $t_{DDKHMP}$ follows the symbol conventions described in note 1.

This figure shows the MII receive AC timing diagram.

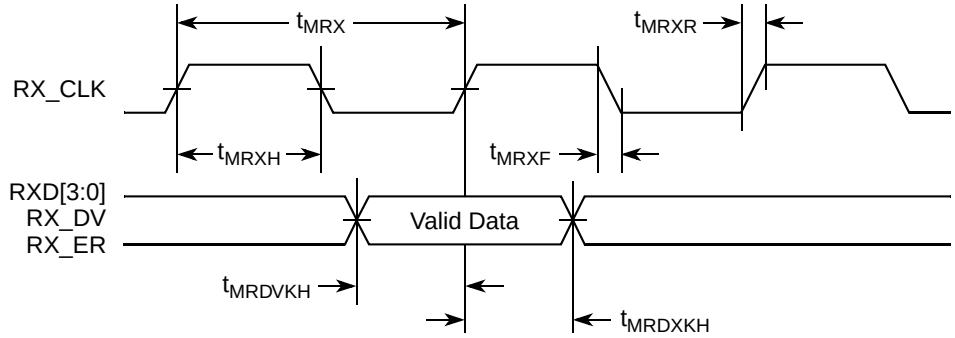


**Figure 10. MII Receive AC Timing Diagram RMII AC Timing Specifications**

### 8.2.1.3 RMII Transmit AC Timing Specifications

This table provides the RMII transmit AC timing specifications.

**Table 28. RMII Transmit AC Timing Specifications**

At recommended operating conditions with $NV_{DD}$ of 3.3 V ± 0.3 V.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| REF_CLK clock | $t_{RMX}$ | — | 20 | — | ns |
| REF_CLK duty cycle | $t_{RMXH}/t_{RMX}$ | 35 | — | 65 | % |
| REF_CLK to RMII data TXD[1:0], TX_EN delay | $t_{RMTKHDX}$ | 2 | — | 10 | ns |
| REF_CLK data clock rise $V_{IL}$(min) to $V_{IH}$(max) | $t_{RMXR}$ | 1.0 | — | 4.0 | ns |
| REF_CLK data clock fall $V_{IH}$(max) to $V_{IL}$(min) | $t_{RMXF}$ | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time $t_{RMX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{RMX}$ represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

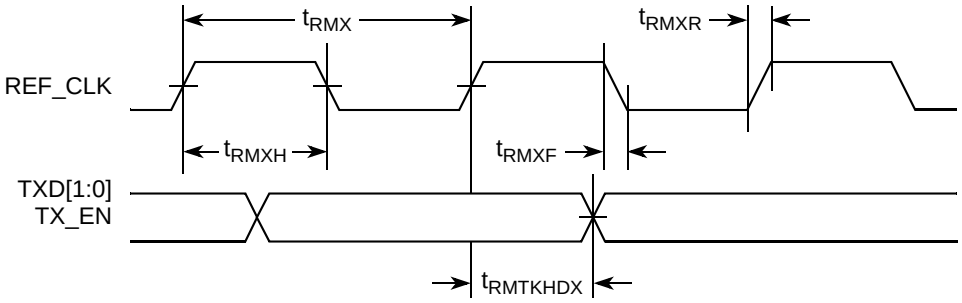


**Figure 11. RMII Transmit AC Timing Diagram**

## 8.2.2 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

**Table 30. RGMII and RTBI AC Timing Specifications**

At recommended operating conditions with $LV_{DDA}/LV_{DDB}$ of 2.5 V ± 5%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Data to clock output skew (at transmitter) | $t_{SKRGT}$ | –0.5 | — | 0.5 | ns |
| Data to clock input skew (at receiver) [2] | $t_{SKRGT}$ | 1.0 | — | 2.6 | ns |
| Clock cycle duration [3] | $t_{RGT}$ | 7.2 | 8.0 | 8.8 | ns |
| Duty cycle for 1000Base-T [4, 5] | $t_{RGTH}/t_{RGT}$ | 45 | 50 | 55 | % |
| Duty cycle for 10BASE-T and 100BASE-TX [3, 5] | $t_{RGTH}/t_{RGT}$ | 40 | 50 | 60 | % |
| Rise time (20%–80%) | $t_{RGTR}$ | — | — | 0.75 | ns |
| Fall time (20%–80%) | $t_{RGTF}$ | — | — | 0.75 | ns |
| GTX_CLK125 reference clock period | $t_{G12}$ [6] | — | 8.0 | — | ns |
| GTX_CLK125 reference clock duty cycle | $t_{G125H}/t_{G125}$ | 47 | — | 53 | % |

**Note:**

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of $t_{RGT}$ represents the RTBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, $t_{RGT}$ scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three $t_{RGT}$ of the lowest speed transitioned between.
5. Duty cycle reference is $LV_{DDA}/2$ or $LV_{DDB}/2$.
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
7. The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

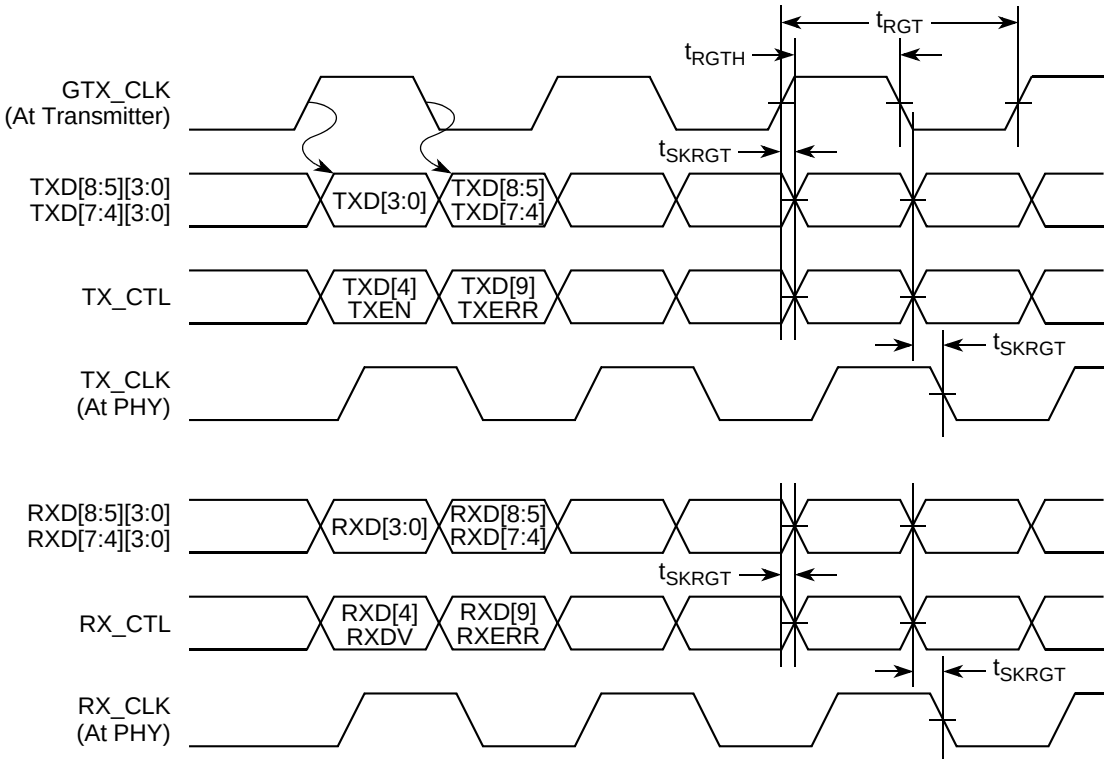


**Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams**

## 8.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-coupled serial link from the dedicated SerDes interface of MPC8313E as shown in Figure 15, where $C_{TX}$ is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features a 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XCOREVSS. The reference circuit of the SerDes transmitter and receiver is shown in Figure 33.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in Section 22.5, "Connection Recommendations," as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the TSEC_GTX_CLK125 clock is not required for this port. Instead, the SerDes reference clock is required on SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ pins.

### 8.3.1 DC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 9, "High-Speed Serial Interfaces (HSSI)."

**Table 37. MII Management DC Electrical Characteristics When Powered at 3.3 V (continued)**

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $NV_{IN}$ symbol referenced in Table 1 and Table 2.

## 8.5.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

**Table 38. MII Management AC Timing Specifications**

At recommended operating conditions with $NV_{DD}$ is 3.3 V ± 0.3V

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| MDC frequency | $f_{MDC}$ | — | 2.5 | — | MHz | 2 |
| MDC period | $t_{MDC}$ | — | 400 | — | ns | |
| MDC clock pulse width high | $t_{MDCH}$ | 32 | — | — | ns | |
| MDC to MDIO delay | $t_{MDKHDX}$ | 10 | — | 170 | ns | |
| MDIO to MDC setup time | $t_{MDDVKH}$ | 5 | — | — | ns | |
| MDIO to MDC hold time | $t_{MDDXKH}$ | 0 | — | — | ns | |
| MDC rise time | $t_{MDCR}$ | — | — | 10 | ns | |
| MDC fall time | $t_{MDHF}$ | — | — | 10 | ns | |

**Notes:**
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)

This figure shows the MII management AC timing diagram.

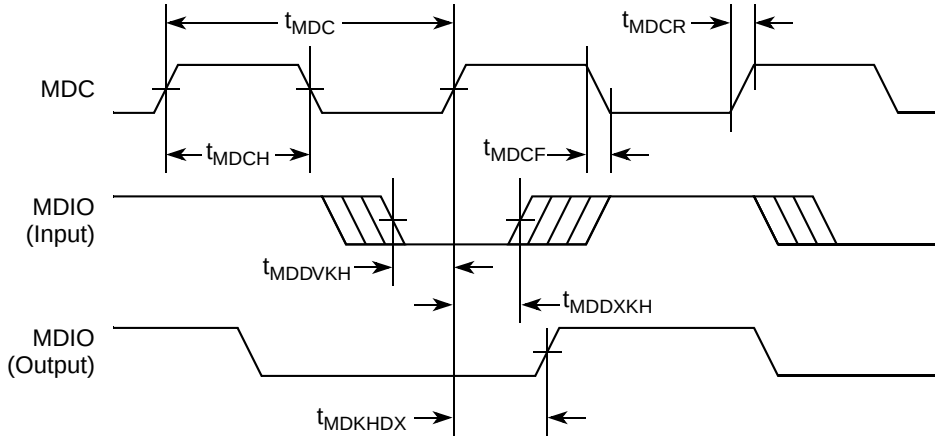


**Figure 21. MII Management Interface Timing Diagram**

The common mode voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out}$ = ($V_{TXn}$ + $V_{\overline{TXn}}$)/2 = (A + B)/2, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It's also referred as the DC offset in some occasion.

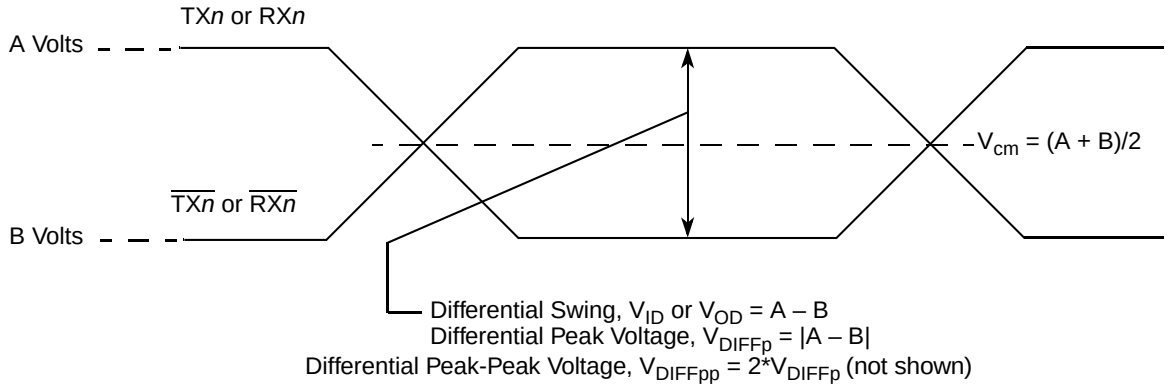


**Figure 22. Differential Voltage Definitions for Transmitter or Receiver**

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing ($V_{OD}$) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 and –500 mV, in other words, $V_{OD}$ is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage ($V_{DIFFp}$) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

## 9.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks input is SD_REF_CLK and $\overline{SD\_REF\_CLK}$ for SGMII interface.

The following sections describe the SerDes reference clock requirements and some application information.

### 9.2.1 SerDes Reference Clock Receiver Characteristics

Figure 23 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $XCOREV_{DD}$ are specified in Table 1 and Table 2.
- SerDes reference clock receiver reference circuit structure:

### 9.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low-phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters for SGMII protocol.

**Table 39. SerDes Reference Clock Common AC Parameters**

At recommended operating conditions with $XV_{DD\_SRDS1}$ or $XV_{DD\_SRDS2}$ = 1.0 V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Rising edge rate | Rise edge rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Falling edge rate | Fall edge rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Differential input high voltage | $V_{IH}$ | +200 | — | mV | 2 |
| Differential input low voltage | $V_{IL}$ | — | –200 | mV | 2 |
| Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn\_REF\_CLK}}$) matching | Rise-fall matching | — | 20 | % | 1, 4 |

**Notes:**
1. Measurement taken from single-ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 31.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point, where SD*n*_REF_CLK rising meets $\overline{\text{SD}n\text{\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK should be compared to the fall edge rate of $\overline{\text{SD}n\text{\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 32.

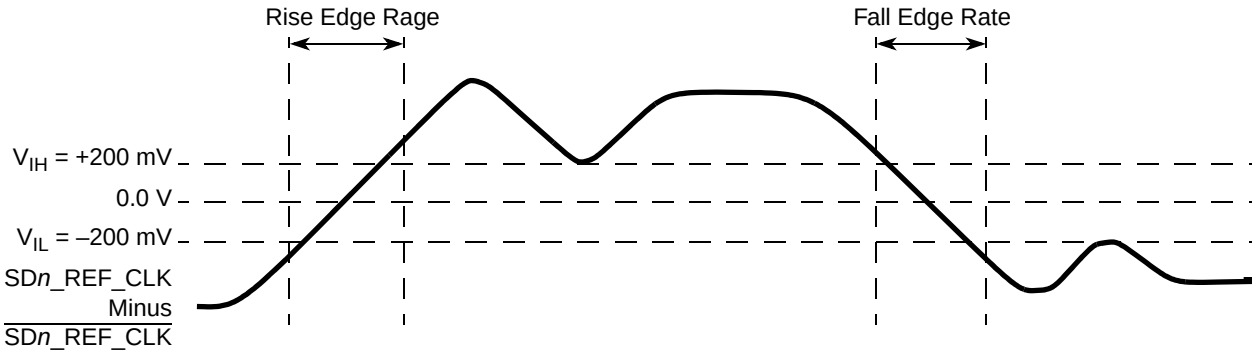


**Figure 31. Differential Measurement Points for Rise and Fall Time**

# 10 USB

## 10.1 USB Dual-Role Controllers

This section provides the AC and DC electrical specifications for the USB interface.

### 10.1.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the USB interface.

**Table 40. USB DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2.0 | $LV_{DDB}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage, $I_{OH}$ = –100 μA | $V_{OH}$ | $LV_{DDB}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 μA | $V_{OL}$ | — | 0.2 | V |

### 10.1.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface.

**Table 41. USB General Timing Parameters (ULPI Mode Only)**

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| USB clock cycle time | $t_{USCK}$ | 15 | — | ns | |
| Input setup to USB clock—all inputs | $t_{USIVKH}$ | 4 | — | ns | |
| input hold to USB clock—all inputs | $t_{USIXKH}$ | 1 | — | ns | |
| USB clock to output valid—all outputs | $t_{USKHOV}$ | — | 7 | ns | |
| Output hold from USB clock—all outputs | $t_{USKHOX}$ | 2 | — | ns | |

**Note**:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{USIXKH}$ symbolizes USB timing (USB) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, $t_{USKHOX}$ symbolizes us timing (USB) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

The following two figures provide the AC test load and signals for the USB, respectively.

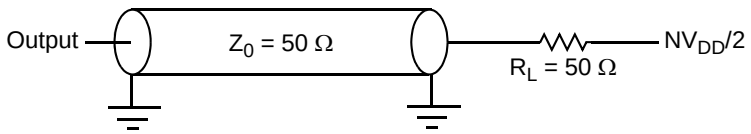


**Figure 34. USB AC Test Load**

This table provides the DC electrical characteristics for the GPIO when the GPIO pins are operating from a 2.5-V supply.

**Table 56. GPIO (When Operating at 2.5 V) DC Electrical Characteristics[1]**

| Parameters | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage 2.5 V | $NV_{DD}$ | — | | 2.37 | 2.63 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –1.0 mA | $NV_{DD}$ = min | 2.00 | $NV_{DD}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 1.0 mA | $NV_{DD}$ = min | $V_{SS}$ – 0.3 | 0.40 | V |
| Input high voltage | $V_{IH}$ | — | $NV_{DD}$ = min | 1.7 | $NV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | $NV_{DD}$ = min | –0.3 | 0.70 | V |
| Input high current | $I_{IH}$ | $V_{IN}$ = $NV_{DD}$ | | — | 10 | μA |
| Input low current | $I_{IL}$ | $V_{IN}$ = $V_{SS}$ | | –15 | — | μA |

**Note:**

1. This specification only applies to GPIO pins that are operating from a 2.5-V supply. See Table 62 for the power supply listed for the individual GPIO signal

## 16.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

**Table 57. GPIO Input AC Timing Specifications[1]**

| Characteristic | Symbol[2] | Min | Unit |
|---|---|---|---|
| GPIO inputs—minimum pulse width | $t_{PIWID}$ | 20 | ns |

**Notes:**

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least $t_{PIWID}$ ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

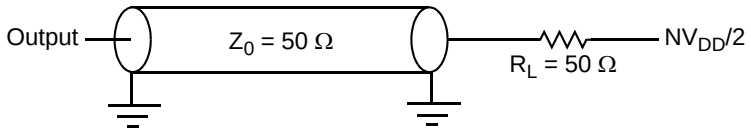


**Figure 52. GPIO AC Test Load**

**Table 62. MPC8313E TEPBGAII Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| $\overline{\text{MEMC\_MCS0}}$ | D10 | O | $GV_{DD}$ | — |
| $\overline{\text{MEMC\_MCS1}}$ | A10 | O | $GV_{DD}$ | — |
| MEMC_MCKE | B14 | O | $GV_{DD}$ | 3 |
| MEMC_MCK | A13 | O | $GV_{DD}$ | — |
| $\overline{\text{MEMC\_MCK}}$ | A14 | O | $GV_{DD}$ | — |
| MEMC_MODT0 | B23 | O | $GV_{DD}$ | — |
| MEMC_MODT1 | C23 | O | $GV_{DD}$ | — |
| **Local Bus Controller Interface** | | | | |
| LAD0 | K25 | I/O | $LV_{DD}$ | 11 |
| LAD1 | K24 | I/O | $LV_{DD}$ | 11 |
| LAD2 | K23 | I/O | $LV_{DD}$ | 11 |
| LAD3 | K22 | I/O | $LV_{DD}$ | 11 |
| LAD4 | J25 | I/O | $LV_{DD}$ | 11 |
| LAD5 | J24 | I/O | $LV_{DD}$ | 11 |
| LAD6 | J23 | I/O | $LV_{DD}$ | 11 |
| LAD7 | J22 | I/O | $LV_{DD}$ | 11 |
| LAD8 | H24 | I/O | $LV_{DD}$ | 11 |
| LAD9 | F26 | I/O | $LV_{DD}$ | 11 |
| LAD10 | G24 | I/O | $LV_{DD}$ | 11 |
| LAD11 | F25 | I/O | $LV_{DD}$ | 11 |
| LAD12 | E25 | I/O | $LV_{DD}$ | 11 |
| LAD13 | F24 | I/O | $LV_{DD}$ | 11 |
| LAD14 | G22 | I/O | $LV_{DD}$ | 11 |
| LAD15 | F23 | I/O | $LV_{DD}$ | 11 |
| LA16 | AC25 | O | $LV_{DD}$ | 11 |
| LA17 | AC26 | O | $LV_{DD}$ | 11 |
| LA18 | AB22 | O | $LV_{DD}$ | 11 |
| LA19 | AB23 | O | $LV_{DD}$ | 11 |
| LA20 | AB24 | O | $LV_{DD}$ | 11 |
| LA21 | AB25 | O | $LV_{DD}$ | 11 |
| LA22 | AB26 | O | $LV_{DD}$ | 11 |
| LA23 | E22 | O | $LV_{DD}$ | 11 |

**Table 62. MPC8313E TEPBGAII Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| **SPI** | | | | |
| SPIMOSI/GTM1_TIN3/GTM2_TIN4/GPIO28/LSRCID4 | H1 | I/O | $NV_{DD}$ | — |
| SPIMISO/$\overline{\text{GTM1\_TGATE3}}$/$\overline{\text{GTM2\_TGATE4}}$/GPIO29/ LDVAL | H3 | I/O | $NV_{DD}$ | — |
| SPICLK/$\overline{\text{GTM1\_TOUT3}}$/GPIO30 | G1 | I/O | $NV_{DD}$ | — |
| SPISEL/GPIO31 | G3 | I/O | $NV_{DD}$ | — |
| **Power and Ground Supplies** | | | | |
| $AV_{DD1}$ | F14 | Power for e300 core APLL (1.0 V) | — | — |
| $AV_{DD2}$ | P21 | Power for system APLL (1.0 V) | — | — |
| $GV_{DD}$ | A2,A3,A4,A24,A25,B3, B4,B5,B12,B13,B20,B21, B24,B25,B26,D1,D2,D8, D9,D16,D17 | Power for DDR1 and DDR2 DRAM I/O voltage (1.8/2.5 V) | — | — |
| $LV_{DD}$ | D24,D25,G23,H23,R23, T23,W25,Y25,AA22,AC23 | Power for local bus (3.3 V) | — | — |
| $LV_{DDA}$ | W2,Y2 | Power for eTSEC2 (2.5 V, 3.3 V) | — | — |
| $LV_{DDB}$ | AC8,AC9,AE4,AE5 | Power for eTSEC1/ USB DR (2.5 V, 3.3 V) | — | — |
| $MV_{REF}$ | C14,D14 | Reference voltage signal for DDR | — | — |
| $NV_{DD}$ | G4,H4,L2,M2,AC16,AC17, AD25,AD26,AE12,AE13, AE20,AE21,AE24,AE25, AE26,AF24,AF25 | Standard I/O voltage (3.3 V) | — | — |
| $V_{DD}$ | K11,K12,K13,K14,K15, K16,L10,L17,M10,M17, N10,N17,U12,U13, | Power for core (1.0 V) | — | — |
| $V_{DDC}$ | F6,F10,F19,K6,K10,K17, K21,P6,P10,P17,R10,R17, T10,T17,U10,U11,U14, U15,U16,U17,W6,W21, AA6,AA10,AA14,AA19 | Internal core logic constant power (1.0 V) | — | — |

**Table 65. System PLL Multiplication Factors (continued)**

| RCWL[SPMF] | System PLL Multiplication Factor |
|---|---|
| 0100 | × 4 |
| 0101 | × 5 |
| 0110 | × 6 |
| 0111–1111 | Reserved |

**Note:**
1. If RCWL[DDRCM] and RCWL[LBCM] are both cleared, the system PLL VCO frequency = (CSB frequency) × (System PLL VCO Divider).
2. If either RCWL[DDRCM] or RCWL[LBCM] are set, the system PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO Divider).
3. The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz

As described in Section 20, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (SYS_CLK_IN or PCI_SYNC_IN) and the internal coherent system bus clock (*csb_clk*). This table shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN/PCI_SYNC_IN ratios.

**Table 66. CSB Frequency Options**

| CFG_CLKIN_DIV at Reset[1] | SPMF | *csb_clk* :Input Clock Ratio[2] | Input Clock Frequency (MHz)[2] | | | |
|---|---|---|---|---|---|---|
| | | | 24 | 25 | 33.33 | 66.67 |
| | | | *csb_clk* Frequency (MHz) | | | |
| High | 0010 | 2:1 | | | | 133 |
| High | 0011 | 3:1 | | | 100 | |
| High | 0100 | 4:1 | | 100 | 133 | |
| High | 0101 | 5:1 | 120 | 125 | 167 | |
| High | 0110 | 6:1 | 144 | 150 | | |
| Low | 0010 | 2:1 | | | | 133 |
| Low | 0011 | 3:1 | | | 100 | |
| Low | 0100 | 4:11 | | 100 | 133 | |
| Low | 0101 | 5:1 | 120 | 125 | 167 | |
| Low | 0110 | 6:1 | 144 | 150 | | |

1 CFG_CLKIN_DIV select the ratio between SYS_CLK_IN and PCI_SYNC_OUT.

2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

**Table 69. Package Thermal Characteristics for TEPBGAII (continued)**

| Characteristic | Board Type | Symbol | TEPBGA II | Unit | Note |
|---|---|---|---|---|---|
| Junction-to-case | — | $R_{\theta JC}$ | 8 | °C/W | 5 |
| Junction-to-package top | Natural convection | $\Psi_{JT}$ | 7 | °C/W | 6 |

**Note:**

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

## 21.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

### 21.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, $T_J$, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_J$ = junction temperature (°C)
$T_A$ = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$P_D$ = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

### 21.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter

Heat sink Vendors include the following list:

| | |
|---|---|
| Aavid Thermalloy<br>80 Commercial St.<br>Concord, NH 03301<br>Internet: www.aavidthermalloy.com | 603-224-9988 |
| Alpha Novatech<br>473 Sapena Ct. #12<br>Santa Clara, CA 95054<br>Internet: www.alphanovatech.com | 408-749-7601 |
| International Electronic Research Corporation (IERC)<br>413 North Moss St.<br>Burbank, CA 91502<br>Internet: www.ctscorp.com | 818-842-7277 |
| Millennium Electronics (MEI)<br>Loroco Sites<br>671 East Brokaw Road<br>San Jose, CA 95112<br>Internet: www.mei-thermal.com | 408-436-8770 |
| Tyco Electronics<br>Chip Coolers™<br>P.O. Box 3668<br>Harrisburg, PA 17105<br>Internet: www.chipcoolers.com | 800-522-6752 |
| Wakefield Engineering<br>33 Bridge St.<br>Pelham, NH 03076<br>Internet: www.wakefield.com | 603-635-2800 |

Interface material vendors include the following:

| | |
|---|---|
| Chomerics, Inc.<br>77 Dragon Ct.<br>Woburn, MA 01801<br>Internet: www.chomerics.com | 781-935-4850 |
| Dow-Corning Corporation<br>Corporate Center<br>PO BOX 994<br>Midland, MI 48686-0994<br>Internet: www.dowcorning.com | 800-248-2481 |
| Shin-Etsu MicroSi, Inc.<br>10028 S. 51st St.<br>Phoenix, AZ 85044<br>Internet: www.microsi.com | 888-642-7674 |
| The Bergquist Company<br>18930 West 78th St.<br>Chanhassen, MN 55317<br>Internet: www.bergquistcompany.com | 800-347-4572 |

- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

## 22.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to $NV_{DD}$, $GV_{DD}$, $LV_{DD}$, $LV_{DDA}$, or $LV_{DDB}$ as required. Unused active high inputs should be connected to $V_{SS}$. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external $V_{DD}$, $NV_{DD}$, $GV_{DD}$, $LV_{DD}$, $LV_{DDA}$, $LV_{DDB}$, and $V_{SS}$ pins of the device.

## 22.6 Output Buffer DC Impedance

The MPC8313E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for $I^2C$).

To measure $Z_0$ for the single-ended drivers, an external resistor is connected from the chip pad to $NV_{DD}$ or $V_{SS}$. Then, the value of each resistor is varied until the pad voltage is $NV_{DD}/2$ (see Figure 60). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open), and $R_P$ is trimmed until the voltage at the pad equals $NV_{DD}/2$. $R_P$ then becomes the resistance of the pull-up devices. $R_P$ and $R_N$ are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

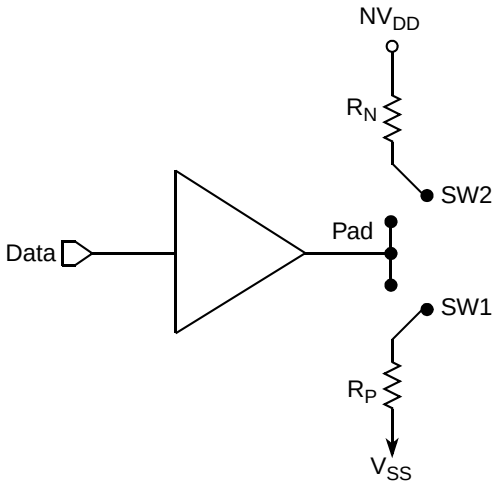


**Figure 60. Driver Impedance Measurement**

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value $R_{term}$. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

**Table 73. Document Revision History (continued)**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 1 | 3/2008 | • Replaced OVDD with $NV_{DD}$ everywhere<br>• Added XCOREVDD and XPADVDD to Table 1<br>• Moved VDD and VDDC to the top of the table before SerDes supplies in Table 2<br>• In Table 2 split DDR row into two from total current requirement of 425 mA. One for DDR1 (131 mA) and other for DDR2 (140 mA).<br>• In Table 2 corrected current requirement numbers for $NV_{DD}$ from 27 mA to 74 mA, $LV_{DD}$ from 60 mA to 16 mA, $LV_{DDA}$ from 85 mA to 22 mA and $LV_{DDB}$ from 85 mA to 44 mA.<br>• In Table 2 corrected Vdd and Vddc current requirements from 560 mA and 454 mA to 469 and 377 mA, respectively. Corrected Avdd1 and Avdd2 current requirements from 10 mA to 2–3 mA, and XCOREVDD from 100 mA to 170 mA.<br>• In Table 2, added row stating junction temperature range of 0 to 105°C. Added footnote 2 stating GPIO pins may operate from 2.5-V supply as well when configured for different functionality.<br>• In Section 2.1.2, “Power Supply Voltage Specification,” added a note describing the purpose of Table 2.<br>• In Section 3, “Power Characteristics,” added a note describing the purpose of Table 5.<br>• Rewrote Section 2.2, “Power Sequencing,” and added Figure 3.<br>• In Table 4, added “but do include core, USB PLL, and a portion of SerDes digital power...” to Note 1.<br>• In Table 4 corrected “Typical power” to “Maximum power” in note 2 and added a note for Typical Power.<br>• In Table 4 removed 266-MHz row as 266-MHz core parts are not offered.<br>• In Table 5, moved Local bus typical power dissipation under LVdd.<br>• Added Table 6 to show the low power mode power dissipation for D3warm mode.<br>• In Table 8 corrected SYS_CLK_IN frequency range from 25–66 MHz to 24–66.67 MHz.<br>• Added Section 8.4, “eTSEC IEEE 1588 AC Specifications”<br>• In Table 42 changed minimum value of USB input hold $t_{USIXKH}$ from 0 to 1ns<br>• Added Table 43 and Table 44 showing USB clock in specifications<br>• In Table 46, added rows for $t_{LALEHOV}$, $t_{LALETOT1}$, $t_{LALETOT2}$, and $t_{LALETOT3}$ parameters. Added Figure 40.<br>• In Table 50, removed row for rise time ($t_{I2CR}$). Removed minimum value of $t_{I2CF}$. Added note 5 stating that the device does not follow the I2C-BUS Specifications version 2.1 regarding the $t_{I2CF}$ AC parameter.<br>• In Table 56, added a note stating: “This specification only applies to GPIO pins that are operating from a 3.3-V supply. See Table 63 for the power supply listed for the individual GPIO signal.” [<br>• Added Table 57 to show DC characteristics for GPIO pins supplied by a 2.5-V supply. Same as eTSEC DC characteristics when operating at 2.5 V.<br>• In Section 20, “Clocking,” corrected the sentence “When the device is configured as a PCI agent device, PCI_SYNC_IN is the primary input clock.” to state “When the device is configured as a PCI agent device, PCI_CLK is the primary input clock.”<br>• Added “Value is decided by RCWLR[COREPLL]” to note 1 of Figure 57<br>• Added paragraph and Figure 59 to Section 22.2, “PLL Power Supply Filtering.”<br>• Added Section 22.4, “SerDes Block Power Supply Decoupling Recommendations<br>• Removed the two figures on PCI undershoot/overshoot voltages and maximum AC waveforms from Section 2.1.2, “Power Supply Voltage Specification,” |