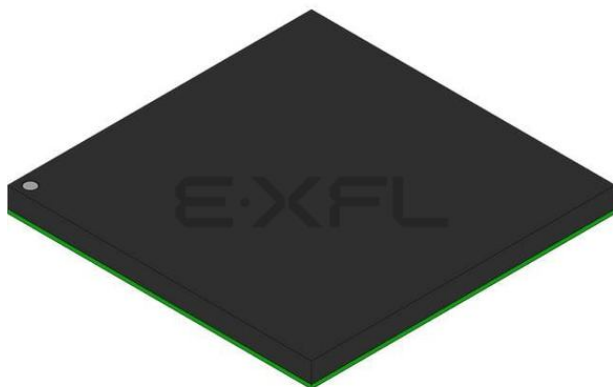




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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8313eczqaaffc

Table 5. MPC8313E Typical I/O Power Dissipation (continued)

Interface	Parameter	GV _{DD} (1.8 V)	GV _{DD} (2.5 V)	NV _{DD} (3.3 V)	LV _{DDA} / LV _{DDB} (3.3 V)	LV _{DDA} / LV _{DDB} (2.5 V)	LV _{DD} (3.3 V)	Unit	Comments
USBDR controller load = 20 pF	60 MHz	—	—	—	0.078	—	—	W	—
Other I/O	—	—	—	0.015	—	—	—	W	—

This table shows the estimated core power dissipation of the MPC8313E while transitioning into the D3 warm low-power state.

Table 6. MPC8313E Low-Power Modes Power Dissipation¹

333-MHz Core, 167-MHz CSB ²	Rev. 1.0 ³	Rev. 2.x or Later ³	Unit
D3 warm	400	425	mW

Note:

1. All interfaces are enabled. For further power savings, disable the clocks to unused blocks.
2. The interfaces are run at the following frequencies: DDR: 333 MHz, eLBC 83 MHz, PCI 33 MHz, eTSEC1 and TSEC2: 167 MHz, SEC: 167 MHz, USB: 167 MHz. See the SCCR register for more information.
3. This is maximum power in D3 Warm based on a voltage of 1.05 V and a junction temperature of 105°C.

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8313E.

4.1 DC Electrical Characteristics

This table provides the system clock input (SYS_CLK_IN/PCI_SYNC_IN) DC timing specifications for the MPC8313E.

Table 7. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V _{IH}	2.4	NV _{DD} + 0.3	V
Input low voltage	—	V _{IL}	−0.3	0.4	V
SYS_CLK_IN input current	0 V ≤ V _{IN} ≤ NV _{DD}	I _{IN}	—	±10	μA
PCI_SYNC_IN input current	0 V ≤ V _{IN} ≤ 0.5 V or NV _{DD} − 0.5 V ≤ V _{IN} ≤ NV _{DD}	I _{IN}	—	±10	μA
PCI_SYNC_IN input current	0.5 V ≤ V _{IN} ≤ NV _{DD} − 0.5 V	I _{IN}	—	±50	μA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the system clock input (SYS_CLK_IN/PCI_CLK) AC timing specifications for the MPC8313E.

Table 8. SYS_CLK_IN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYS_CLK_IN/PCI_CLK frequency	$f_{\text{SYS_CLK_IN}}$	24	—	66.67	MHz	1
SYS_CLK_IN/PCI_CLK cycle time	$t_{\text{SYS_CLK_IN}}$	15	—	—	ns	—
SYS_CLK_IN rise and fall time	$t_{\text{KH}}, t_{\text{KL}}$	0.6	0.8	4	ns	2
PCI_CLK rise and fall time	$t_{\text{PCH}}, t_{\text{PCL}}$	0.6	0.8	1.2	ns	2
SYS_CLK_IN/PCI_CLK duty cycle	$t_{\text{KHK}}/t_{\text{SYS_CLK_IN}}$	40	—	60	%	3
SYS_CLK_IN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

1. **Caution:** The system, core, security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN/PCI_CLK are measured at 0.4 and 2.4 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8313E.

5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins.

Table 9. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	$NV_{\text{DD}} + 0.3$	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{\text{IN}} \leq NV_{\text{DD}}$	—	±5	μA
Output high voltage	V_{OH}	$I_{\text{OH}} = -8.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{\text{OL}} = 8.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{\text{OL}} = 3.2 \text{ mA}$	—	0.4	V

5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications.

Table 10. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{\text{PCI_SYNC_IN}}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock and power applied to SYS_CLK_IN when the device is in PCI host mode	32	—	$t_{\text{SYS_CLK_IN}}$	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock and power applied to PCI_SYNC_IN when the device is in PCI agent mode	32	—	$t_{\text{PCI_SYNC_IN}}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{\text{PCI_SYNC_IN}}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	$t_{\text{SYS_CLK_IN}}$	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{\text{PCI_SYNC_IN}}$	1
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR configuration signal drivers with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to turn on POR configuration signal drivers with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{\text{PCI_SYNC_IN}}$	1, 3

Notes:

1. $t_{\text{PCI_SYNC_IN}}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is in PCI host mode the primary clock is applied to the SYS_CLK_IN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV.
2. $t_{\text{SYS_CLK_IN}}$ is the clock period of the input clock applied to SYS_CLK_IN. It is only valid when the device is in PCI host mode.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

This table provides the PLL lock times.

Table 11. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface. Note that DDR SDRAM is $\text{GV}_{\text{DD}}(\text{typ}) = 2.5 \text{ V}$ and DDR2 SDRAM is $\text{GV}_{\text{DD}}(\text{typ}) = 1.8 \text{ V}$.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) when $GV_{DD}(typ) = 1.8\text{ V}$.

Table 12. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 1.8\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.125$	V	—
Output leakage current	I_{OZ}	-9.9	9.9	μA	4
Output high current ($V_{OUT} = 1.420\text{ V}$)	I_{OH}	-13.4	—	mA	—
Output low current ($V_{OUT} = 0.280\text{ V}$)	I_{OL}	13.4	—	mA	—

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail should track variations in the DC level of MV_{REF} .
4. Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

This table provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8\text{ V}$.

Table 13. DDR2 SDRAM Capacitance for $GV_{DD}(typ) = 1.8\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 1.8\text{ V} \pm 0.090\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 14. DDR SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 2.5\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	2.3	2.7	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.15$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.15$	V	—

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Silicon Rev 2.x or Later

Parameter	Symbol ¹	Min	Max	Unit	Note
MCK[n] cycle time, MCK[n]/MCK[n] crossing	t_{MCK}	6	10	ns	2
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz	t_{DDKHAS}	2.1 2.5	— —	ns	3
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz	t_{DDKHAX}	2.0 2.7	— —	ns	3
MCS[n] output setup with respect to MCK 333 MHz 266 MHz	t_{DDKHCS}	2.1 3.15	— —	ns	3
MCS[n] output hold with respect to MCK 333 MHz 266 MHz	$t_{DDKHCSX}$	2.0 2.7	— —	ns	3
MCK to MDQS Skew	t_{DDKMHM}	−0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS 333 MHz 266 MHz	t_{DDKHDS} , t_{DDKLDS}	800 900	— —	ps	5
MDQ//MDM output hold with respect to MDQS 333 MHz 266 MHz	t_{DDKHDX} , t_{DDKLDX}	750 1000	— —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	−0.6	0.6	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/MCK referenced measurements are made from the crossing of the two signals ± 0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ//MDM/MDQS.
4. Note that t_{DDKMHM} follows the symbol conventions described in note 1. For example, t_{DDKMHM} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKMHM} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*, for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

8.2.1.4 RMII Receive AC Timing Specifications

This table provides the RMII receive AC timing specifications.

Table 29. RMII Receive AC Timing Specifications

At recommended operating conditions with NV_{DD} of $3.3\text{ V} \pm 0.3\text{ V}$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{RMXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first three letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This table provides the AC test load.

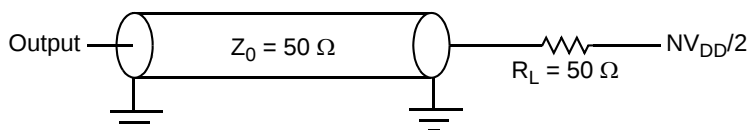


Figure 12. AC Test Load

This table shows the RMII receive AC timing diagram.

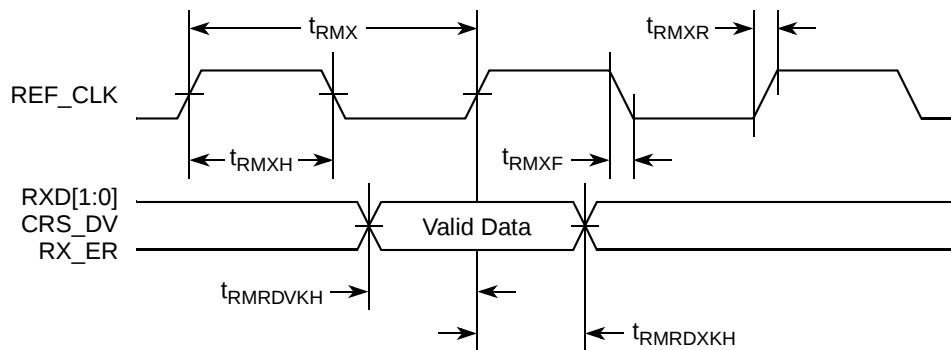


Figure 13. RMII Receive AC Timing Diagram

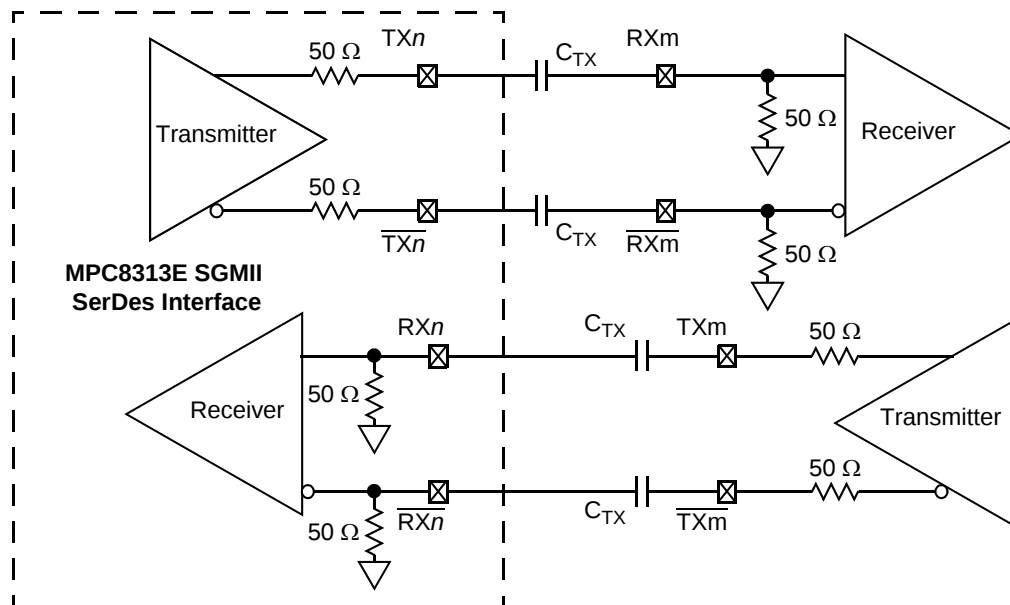


Figure 15. 4-Wire AC-Coupled SGMII Serial Link Connection Example

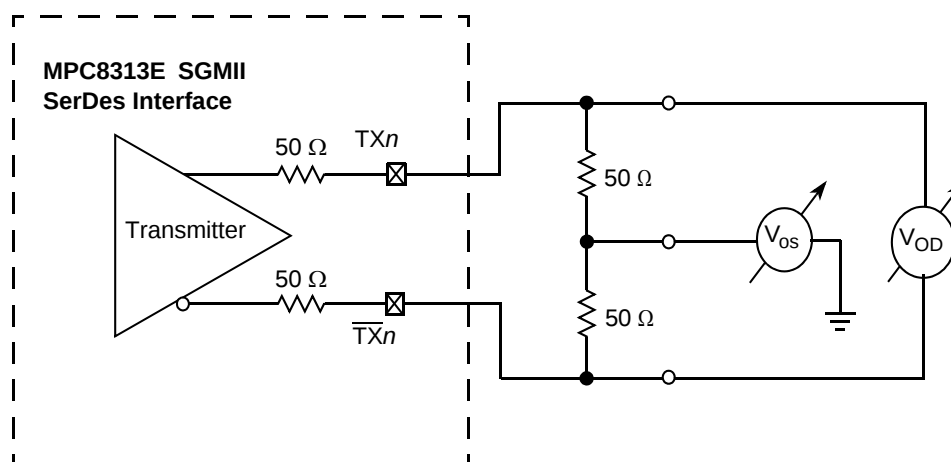


Figure 16. SGMII Transmitter DC Measurement Circuit

Table 33. SGMII DC Receiver Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	XCOREV _{DD}	0.95	1.0	1.05	V	
DC Input voltage range		N/A				1
Input differential voltage	V _{RX_DIFFp-p}	100	—	1200	mV	2
Loss of signal threshold	V _{LOS}	30	—	100	mV	
Input AC common mode voltage	V _{CM_ACP-p}	—	—	100	mV	3
Receiver differential input impedance	Z _{RX_DIFF}	80	100	120	Ω	
Receiver common mode input impedance	Z _{RX_CM}	20	—	35	Ω	

Table 35. SGMII Receive AC Timing Specifications (continued)

At recommended operating conditions with $XCOREV_{DD} = 1.0\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Total jitter tolerance	JT	0.65	—	—	UI p-p	1
Bit error ratio	BER	—	—	10^{-12}		
Unit interval	UI	799.92	800	800.08	ps	2
AC coupling capacitor	C_{TX}	5	—	200	nF	3

Notes:

1. Measured at receiver.
2. Each UI is $800\text{ ps} \pm 100\text{ ppm}$.
3. The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.

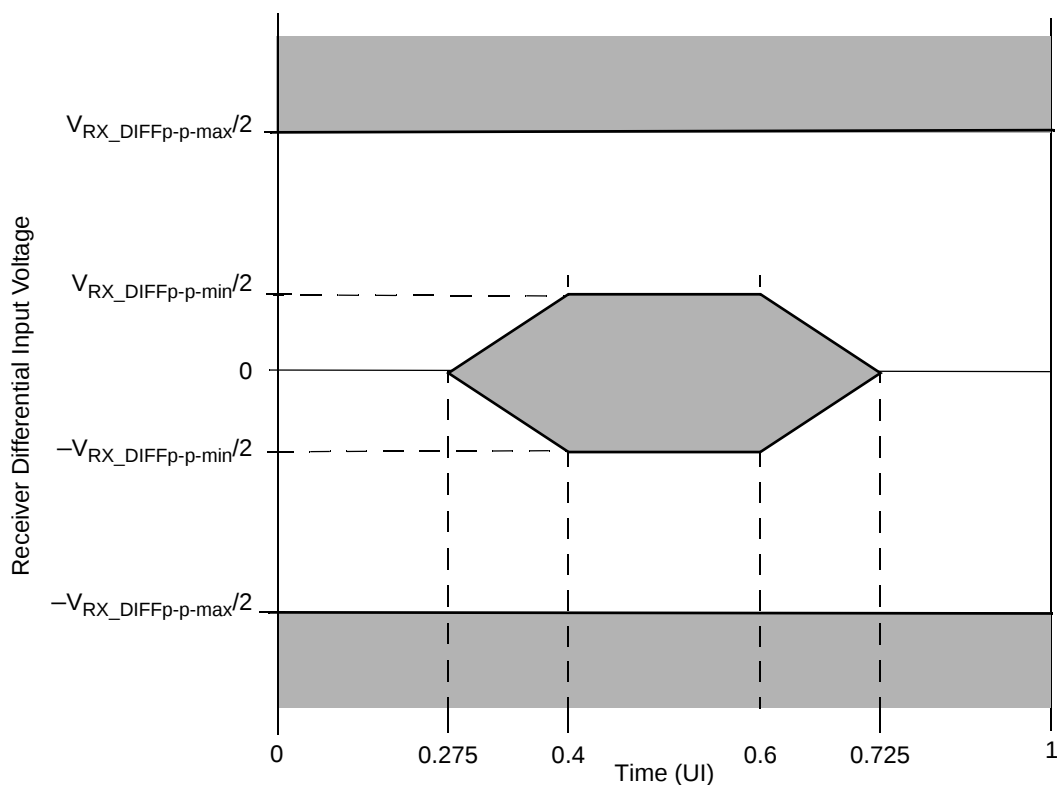


Figure 17. SGMII Receiver Input Compliance Mask

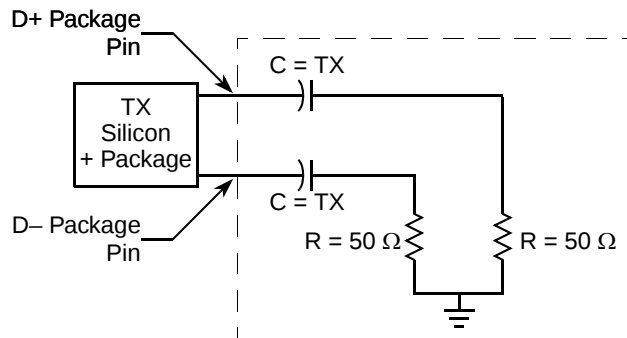
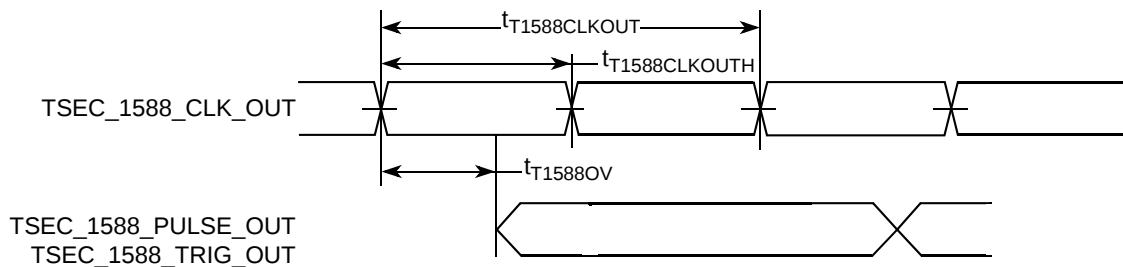


Figure 18. SGMII AC Test/Measurement Load

8.4 eTSEC IEEE 1588 AC Specifications

This figure provides the data and command output timing diagram.



Note: The output delay is count starting rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is count starting falling edge.

Figure 19. eTSEC IEEE 1588 Output AC Timing

This figure provides the data and command input timing diagram.

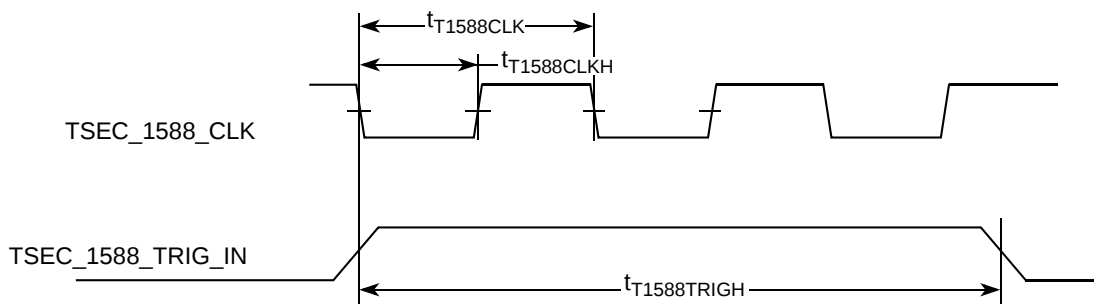


Figure 20. eTSEC IEEE 1588 Input AC Timing

This table lists the IEEE 1588 AC timing specifications.

Table 36. eTSEC IEEE 1588 AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of $3.3\text{ V} \pm 5\%$.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.8	—	$T_{RX_CLK} \times 9$	ns	1, 3
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	

Table 45. Local Bus General Timing Parameters (continued)

Parameter	Symbol ¹	Min	Max	Unit	Note
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- Notes:**
1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1).
 2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
 3. All signals are measured from $\text{NV}_{\text{DD}}/2$ of the rising/falling edge of LCLK0 to $0.4 \times \text{NV}_{\text{DD}}$ of the signal in question for 3.3-V signaling levels.
 4. Input timings are measured at the pin.
 5. t_{LBOTOT1} and t_{LALETOT1} should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
 6. t_{LBOTOT2} and t_{LALETOT2} should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
 7. t_{LBOTOT3} and t_{LALETOT3} should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.
 8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This figure provides the AC test load for the local bus.

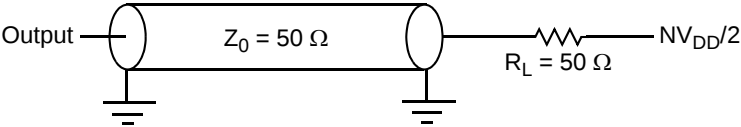


Figure 36. Local Bus AC Test Load

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE Std 1149.1 (JTAG) interface.

Table 46. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	$NV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	$I_{OH} = -8.0$ mA	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2$ mA	—	0.4	V

12.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std 1149.1 (JTAG) interface. This table provides the JTAG AC timing specifications as defined in [Figure 41](#) through [Figure 45](#).

Table 47. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)¹

At recommended operating conditions (see [Table 2](#)).

Parameter	Symbol ²	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times:				ns	
Boundary-scan data TMS, TDI	t_{JTDVKH} t_{JTIVKH}	4 4	— —		4
Input hold times:				ns	
Boundary-scan data TMS, TDI	t_{JTDXKH} t_{JTIXKH}	10 10	— —		4
Valid times:				ns	
Boundary-scan data TDO	t_{JTKLDV} t_{JTKLOV}	2 2	11 11		5
Output hold times:				ns	
Boundary-scan data TDO	t_{JTKLDX} t_{JTKLOX}	2 2	— —		5

Table 47. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)¹ (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Max	Unit	Note
JTAG external clock to output high impedance:					
Boundary-scan data	t_{JTKLDZ}	2	19	ns	5, 6
TDO	t_{JTKLOZ}	2	9		

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50- Ω load (see Figure 34). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVXH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDVXH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK} .
5. Non-JTAG signal output timing with respect to t_{TCLK} .
6. Guaranteed by design and characterization.

This figure provides the AC test load for TDO and the boundary-scan outputs.

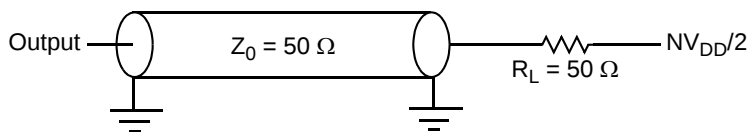


Figure 41. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

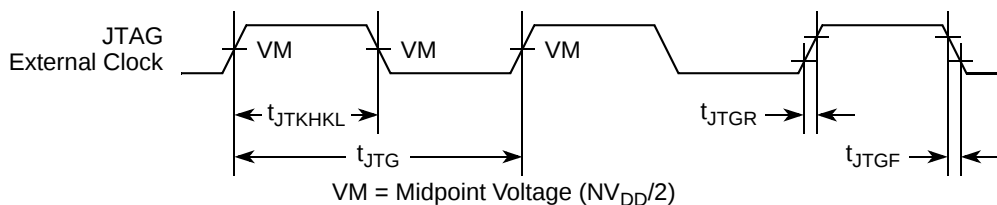


Figure 42. JTAG Clock Input Timing Diagram

This figure provides the $\overline{TRST}$ timing diagram.

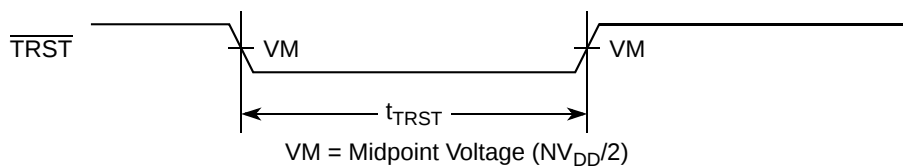


Figure 43. $\overline{TRST}$ Timing Diagram

This figure provides the boundary-scan timing diagram.

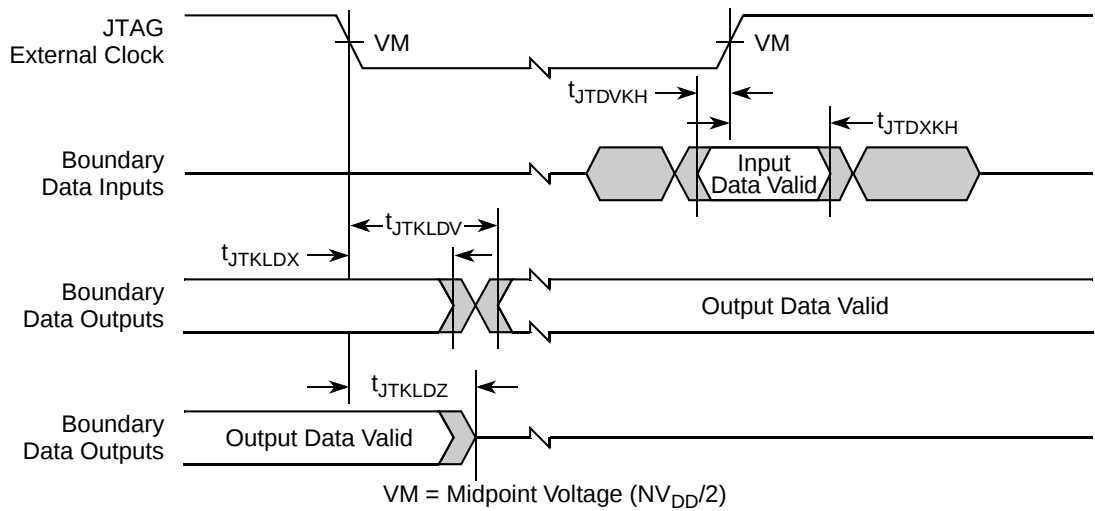


Figure 44. Boundary-Scan Timing Diagram

This figure provides the test access port timing diagram.

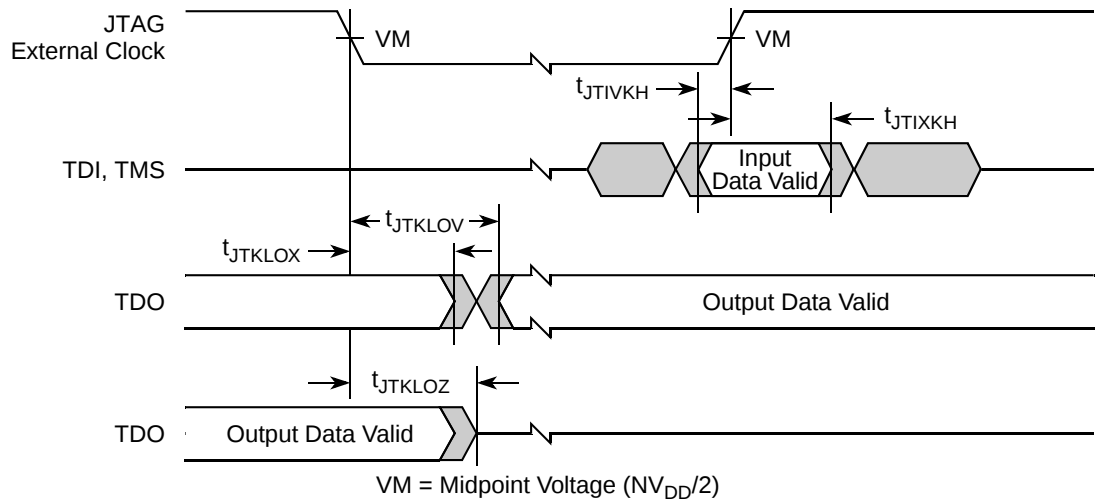


Figure 45. Test Access Port Timing Diagram

This table provides the DC electrical characteristics for the GPIO when the GPIO pins are operating from a 2.5-V supply.

Table 56. GPIO (When Operating at 2.5 V) DC Electrical Characteristics¹

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	NV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$	$NV_{DD} = \text{min}$	2.00	$NV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$	$NV_{DD} = \text{min}$	$V_{SS} - 0.3$	0.40	V
Input high voltage	V_{IH}	—	$NV_{DD} = \text{min}$	1.7	$NV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	$NV_{DD} = \text{min}$	-0.3	0.70	V
Input high current	I_{IH}	$V_{IN} = NV_{DD}$		—	10	μA
Input low current	I_{IL}	$V_{IN} = V_{SS}$		-15	—	μA

Note:

1. This specification only applies to GPIO pins that are operating from a 2.5-V supply. See [Table 62](#) for the power supply listed for the individual GPIO signal

16.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 57. GPIO Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

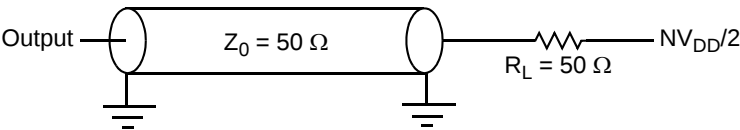


Figure 52. GPIO AC Test Load

Table 60. SPI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	$NV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	$0\text{ V} \leq V_{IN} \leq NV_{DD}$	—	±5	μA

18.2 SPI AC Timing Specifications

This table and provide the SPI input and output AC timing specifications.

Table 61. SPI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
SPI outputs—master mode (internal clock) delay	$t_{NIKH OV}$	0.5	6	ns
SPI outputs—slave mode (external clock) delay	$t_{NEKH OV}$	2	8	ns
SPI inputs—master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Note:

- Output specifications are measured from the 50% level of the rising edge of SYS_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{NIKH OV}$ symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

This figure provides the AC test load for the SPI.

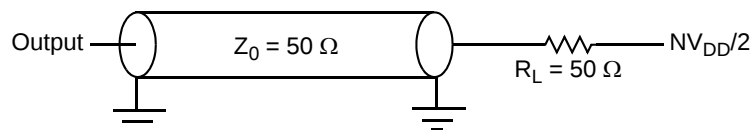


Figure 53. SPI AC Test Load

Figure 54 and Figure 55 represent the AC timing from Table 61. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Table 62. MPC8313E TEPBGAI Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_AD6	AD19	I/O	NV _{DD}	—
PCI_AD7	AD20	I/O	NV _{DD}	—
PCI_AD8	AC18	I/O	NV _{DD}	—
PCI_AD9	AD18	I/O	NV _{DD}	—
PCI_AD10	AB18	I/O	NV _{DD}	—
PCI_AD11	AE19	I/O	NV _{DD}	—
PCI_AD12	AB17	I/O	NV _{DD}	—
PCI_AD13	AE18	I/O	NV _{DD}	—
PCI_AD14	AD17	I/O	NV _{DD}	—
PCI_AD15	AF19	I/O	NV _{DD}	—
PCI_AD16	AB14	I/O	NV _{DD}	—
PCI_AD17	AF15	I/O	NV _{DD}	—
PCI_AD18	AD14	I/O	NV _{DD}	—
PCI_AD19	AE14	I/O	NV _{DD}	—
PCI_AD20	AF12	I/O	NV _{DD}	—
PCI_AD21	AE11	I/O	NV _{DD}	—
PCI_AD22	AD12	I/O	NV _{DD}	—
PCI_AD23	AB13	I/O	NV _{DD}	—
PCI_AD24	AF9	I/O	NV _{DD}	—
PCI_AD25	AD11	I/O	NV _{DD}	—
PCI_AD26	AE10	I/O	NV _{DD}	—
PCI_AD27	AB12	I/O	NV _{DD}	—
PCI_AD28	AD10	I/O	NV _{DD}	—
PCI_AD29	AC10	I/O	NV _{DD}	—
PCI_AD30	AF10	I/O	NV _{DD}	—
PCI_AD31	AF8	I/O	NV _{DD}	—
PCI_C/ $\overline{\text{BE0}}$	AC19	I/O	NV _{DD}	—
PCI_C/ $\overline{\text{BE1}}$	AB15	I/O	NV _{DD}	—
PCI_C/ $\overline{\text{BE2}}$	AF14	I/O	NV _{DD}	—
PCI_C/ $\overline{\text{BE3}}$	AF11	I/O	NV _{DD}	—
PCI_PAR	AD16	I/O	NV _{DD}	—
$\overline{\text{PCI_FRAME}}$	AF16	I/O	NV _{DD}	5

Table 69. Package Thermal Characteristics for TEPBGAI (continued)

Characteristic	Board Type	Symbol	TEPBGA II	Unit	Note
Junction-to-case	—	$R_{\theta JC}$	8	°C/W	5
Junction-to-package top	Natural convection	Ψ_{JT}	7	°C/W	6

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

21.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

21.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

21.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter

23.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the MPC8313E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 72. Part Numbering Nomenclature

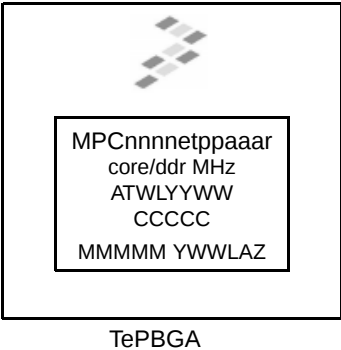
MPC	nnnn	e	t	pp	aa	a	x
Product Code	Part Identifier	Encryption Acceleration	Temperature Range ³	Package ^{1, 4}	e300 core Frequency ²	DDR Frequency	Revision Level
MPC	8313	Blank = Not included E = included	Blank = 0° to 105°C C = -40° to 105°C	ZQ = PB TEPBGAII VR = PB free TEPBGAII	AD = 266 MHz AF = 333 MHz AG = 400 MHz	D = 266 MHz F = 333 MHz	Blank = 1.0 A = 2.0 B = 2.1 C = 2.2

Note:

1. See [Section 19, "Package and Pin Listings,"](#) for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
3. Contact local Freescale office on availability of parts with °C temperature range.
4. ZQ package was available for Rev 1.0. For Rev 2.x, only VR package is available.

23.2 Part Marking

Parts are marked as shown in this figure.



Notes:

- MPCnnnnnetppaaar is the orderable part number.
- ATWLYYWW is the standard assembly, test, year, and work week codes.
- CCCCC is the country code.
- MMMMM is the mask number.

Figure 62. Part Marking for TEPBGAII Device

Table 73. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
1	3/2008	- Replaced OVDD with NV_{DD} everywhere - Added XCOREVDD and XPADVDD to Table 1 - Moved VDD and VDDC to the top of the table before SerDes supplies in Table 2 - In Table 2 split DDR row into two from total current requirement of 425 mA. One for DDR1 (131 mA) and other for DDR2 (140 mA). - In Table 2 corrected current requirement numbers for NV_{DD} from 27 mA to 74 mA, LV_{DD} from 60 mA to 16 mA, LV_{DDA} from 85 mA to 22 mA and LV_{DDB} from 85 mA to 44 mA. - In Table 2 corrected Vdd and Vddc current requirements from 560 mA and 454 mA to 469 and 377 mA, respectively. Corrected Avdd1 and Avdd2 current requirements from 10 mA to 2–3 mA, and XCOREVDD from 100 mA to 170 mA. - In Table 2, added row stating junction temperature range of 0 to 105°C. Added footnote 2 stating GPIO pins may operate from 2.5-V supply as well when configured for different functionality. - In Section 2.1.2, “Power Supply Voltage Specification,” added a note describing the purpose of Table 2. - In Section 3, “Power Characteristics,” added a note describing the purpose of Table 5. - Rewrote Section 2.2, “Power Sequencing,” and added Figure 3. - In Table 4, added “but do include core, USB PLL, and a portion of SerDes digital power...” to Note 1. - In Table 4 corrected “Typical power” to “Maximum power” in note 2 and added a note for Typical Power. - In Table 4 removed 266-MHz row as 266-MHz core parts are not offered. - In Table 5, moved Local bus typical power dissipation under LVdd. - Added Table 6 to show the low power mode power dissipation for D3warm mode. - In Table 8 corrected SYS_CLK_IN frequency range from 25–66 MHz to 24–66.67 MHz. - Added Section 8.4, “eTSEC IEEE 1588 AC Specifications” - In Table 42 changed minimum value of USB input hold t_{USIXKH} from 0 to 1ns - Added Table 43 and Table 44 showing USB clock in specifications - In Table 46, added rows for t_{LALEHOV}, t_{LALETOT1}, t_{LALETOT2}, and t_{LALETOT3} parameters. Added Figure 40. - In Table 50, removed row for rise time (t_{I2CR}). Removed minimum value of t_{I2CF}. Added note 5 stating that the device does not follow the I2C-BUS Specifications version 2.1 regarding the t_{I2CF} AC parameter. - In Table 56, added a note stating: “This specification only applies to GPIO pins that are operating from a 3.3-V supply. See Table 63 for the power supply listed for the individual GPIO signal.” [- Added Table 57 to show DC characteristics for GPIO pins supplied by a 2.5-V supply. Same as eTSEC DC characteristics when operating at 2.5 V. - In Section 20, “Clocking,” corrected the sentence “When the device is configured as a PCI agent device, PCI_SYNC_IN is the primary input clock.” to state “When the device is configured as a PCI agent device, PCI_CLK is the primary input clock.” - Added “Value is decided by RCWLR[COREPLL]” to note 1 of Figure 57 - Added paragraph and Figure 59 to Section 22.2, “PLL Power Supply Filtering.” - Added Section 22.4, “SerDes Block Power Supply Decoupling Recommendations - Removed the two figures on PCI undershoot/overshoot voltages and maximum AC waveforms from Section 2.1.2, “Power Supply Voltage Specification,”

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