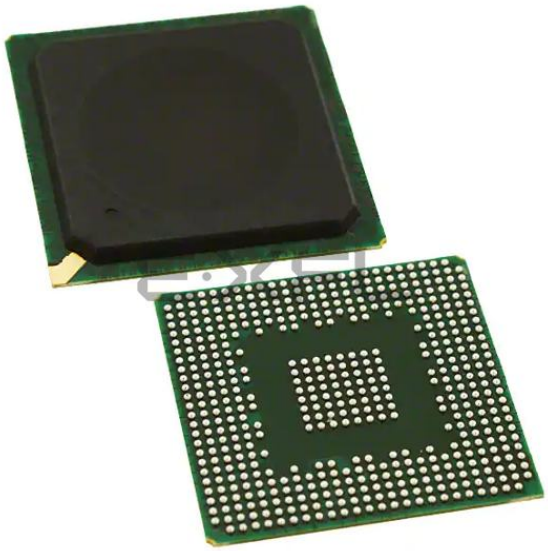

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8313eczqagdc

1.6 USB Dual-Role Controller

The MPC8313E USB controller includes the following features:

- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Compatible with *Universal Serial Bus Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI + low pin interface (ULPI) or on-chip USB 2.0 full-speed/high-speed PHY

1.7 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8313E eTSECs include the following features:

- Two RGMII/SGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3®, 802.3u®, 802.3x®, 802.3z®, 802.3au®, and 802.3ab®
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status
- Three-speed support (10/100/1000 Mbps)
- On-chip high-speed serial interface to external SGMII PHY interface
- Support for IEEE Std 1588™
- Support for two full-duplex FIFO interface modes
- Multiple PHY interface configuration
- TCP/IP acceleration and QoS features available
- IP v4 and IP v6 header recognition on receive
- IP v4 header checksum verification and generation
- TCP and UDP checksum verification and generation
- Per-packet configurable acceleration
- Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2®, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
- Transmission from up to eight physical queues.
- Reception to up to eight physical queues

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Silicon Rev 2.x or Later

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK[*n*] cycle time, MCK[*n*]/$\overline{\text{MCK}}$[*n*] crossing	t_{MCK}	6	10	ns	2
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz	t_{DDKHAS}	 2.1 2.5	 — —	ns	3
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz	t_{DDKHAX}	 2.0 2.7	 — —	ns	3
$\overline{\text{MCS}}$[*n*] output setup with respect to MCK 333 MHz 266 MHz	t_{DDKHCS}	 2.1 3.15	 — —	ns	3
$\overline{\text{MCS}}$[*n*] output hold with respect to MCK 333 MHz 266 MHz	t_{DDKHCX}	 2.0 2.7	 — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS 333 MHz 266 MHz	t_{DDKHDS}, t_{DDKLDS}	 800 900	 — —	ps	5
MDQ//MDM output hold with respect to MDQS 333 MHz 266 MHz	t_{DDKHDX}, t_{DDKLDX}	 750 1000	 — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

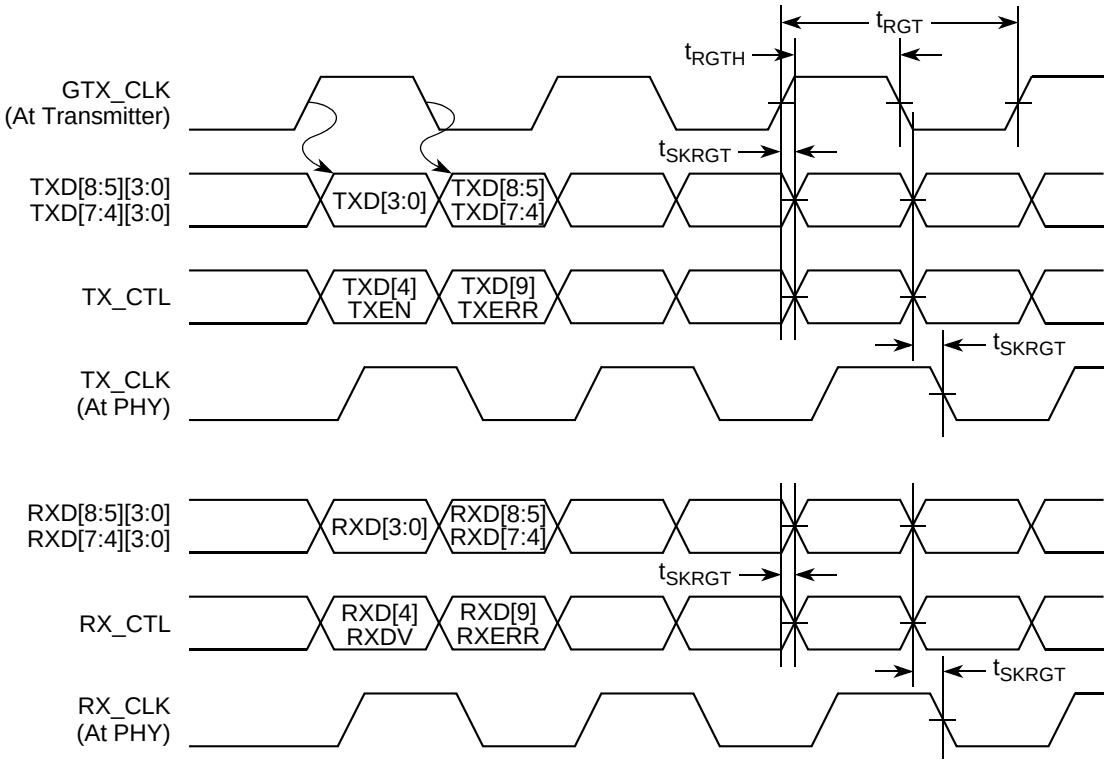


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-coupled serial link from the dedicated SerDes interface of MPC8313E as shown in Figure 15, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features a 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XCOREVSS. The reference circuit of the SerDes transmitter and receiver is shown in Figure 33.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in Section 22.5, "Connection Recommendations," as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the TSEC_GTX_CLK125 clock is not required for this port. Instead, the SerDes reference clock is required on SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ pins.

8.3.1 DC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 9, "High-Speed Serial Interfaces (HSSI)."

Table 33. SGMII DC Receiver Electrical Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Common mode input voltage	V_{CM}	—	$V_{xcorevss}$	—	V	4

Notes:
1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak to peak input differential voltage
3. $V_{CM\_ACp\text{-}p}$ is also referred to as peak to peak AC common mode voltage.
4. On-chip termination to $XCOREV_{SS}$.

8.3.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (TX[*n*] and $\overline{\text{TX}}$[*n*]) or at the receiver inputs (RX[*n*] and $\overline{\text{RX}}$[*n*]) as depicted in Figure 18, respectively.

8.3.4.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 34. SGMII Transmit AC Timing Specifications

At recommended operating conditions with $XCOREV_{DD}$ = 1.0 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter	JD	—	—	0.17	UI p-p	
Total jitter	JT	—	—	0.35	UI p-p	
Unit interval	UI	799.92	800	800.08	ps	1
V_{OD} fall time (80%–20%)	tfall	50	—	120	ps	
V_{OD} rise time (20%–80%)	t_{rise}	50	—	120	ps	

Note:
1. Each UI is 800 ps ± 100 ppm.

8.3.4.2 SGMII Receive AC Timing Specifications

This table provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 17 shows the SGMII receiver input compliance mask eye diagram.

Table 35. SGMII Receive AC Timing Specifications

At recommended operating conditions with $XCOREV_{DD}$ = 1.0 V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic jitter tolerance	JD	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	JDR	0.55	—	—	UI p-p	1
Sinusoidal jitter tolerance	JSIN	0.1	—	—	UI p-p	1

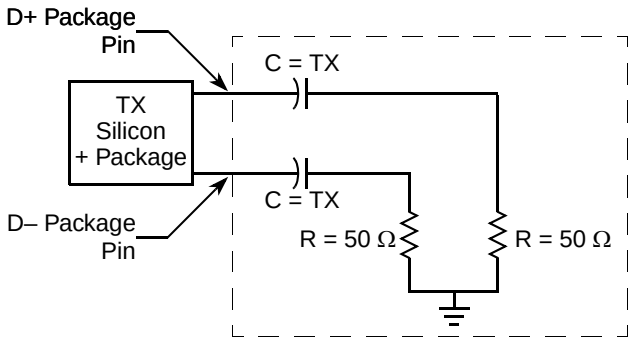
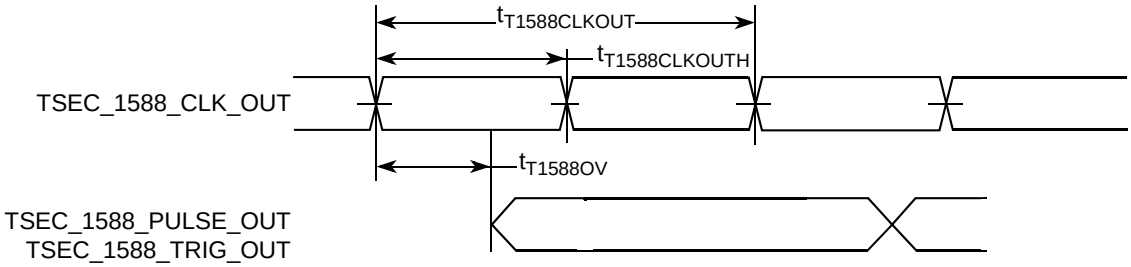


Figure 18. SGMII AC Test/Measurement Load

8.4 eTSEC IEEE 1588 AC Specifications

This figure provides the data and command output timing diagram.



Note: The output delay is count starting rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is count starting falling edge.

Figure 19. eTSEC IEEE 1588 Output AC Timing

This figure provides the data and command input timing diagram.

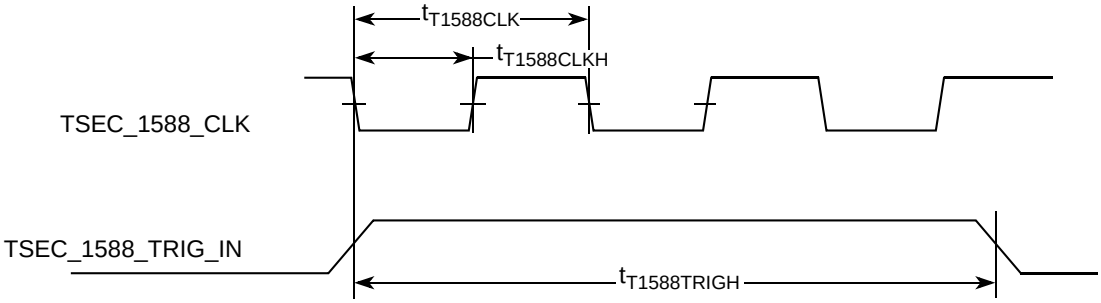


Figure 20. eTSEC IEEE 1588 Input AC Timing

This table lists the IEEE 1588 AC timing specifications.

Table 36. eTSEC IEEE 1588 AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.8	—	$T_{RX\_CLK} \times 9$	ns	1, 3
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	

assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC coupling. Its value could be ranged from 140 to 240 Ω depending on the clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8313E SerDes3 reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Consult with the clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

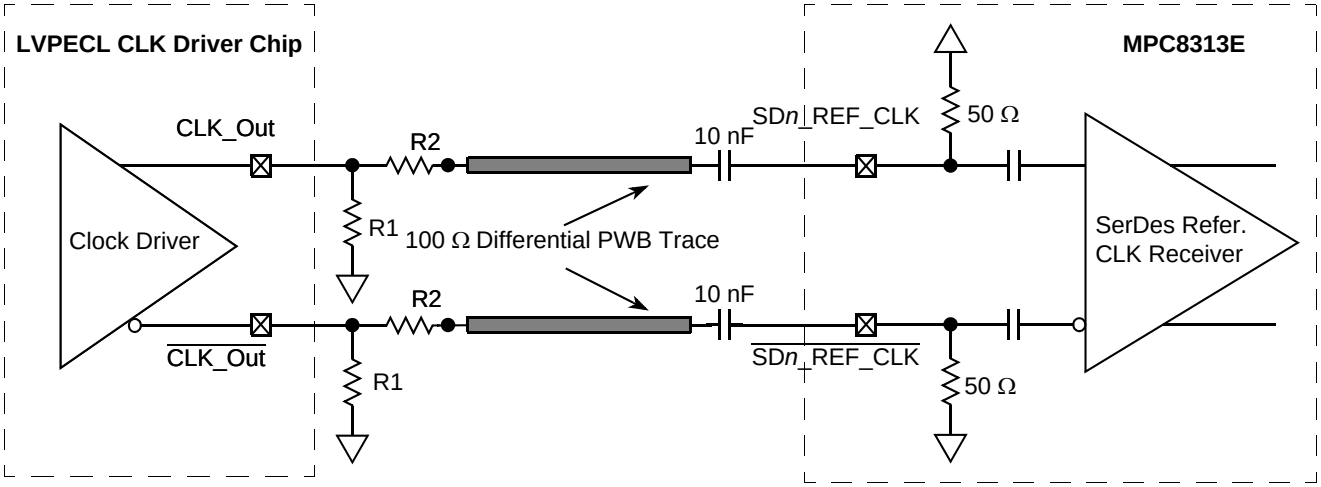


Figure 29. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with the MPC8313E SerDes reference clock input's DC requirement.

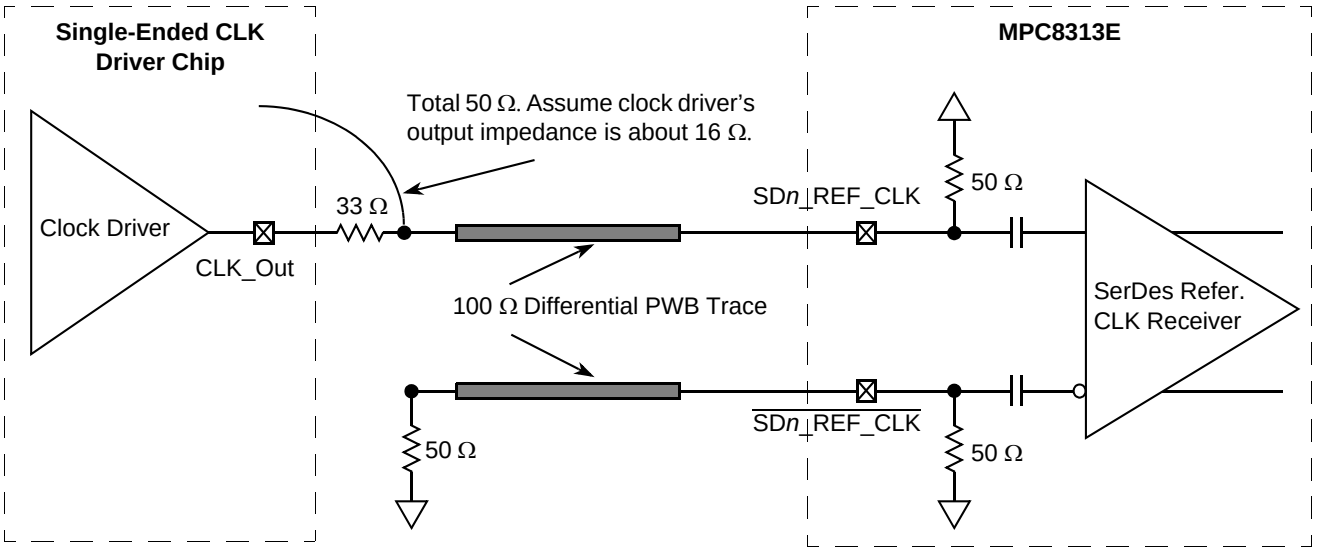


Figure 30. Single-Ended Connection (Reference Only)

9.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low-phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters for SGMII protocol.

Table 39. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD_SRDS1} or XV_{DD_SRDS2} = 1.0 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
Rising edge rate	Rise edge rate	1.0	4.0	V/ns	2, 3
Falling edge rate	Fall edge rate	1.0	4.0	V/ns	2, 3
Differential input high voltage	V_{IH}	+200	—	mV	2
Differential input low voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn\_REF\_CLK}}$) matching	Rise-fall matching	—	20	%	1, 4

Notes:
1. Measurement taken from single-ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 31.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point, where SD*n*_REF_CLK rising meets $\overline{\text{SD}n\text{\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK should be compared to the fall edge rate of $\overline{\text{SD}n\text{\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 32.

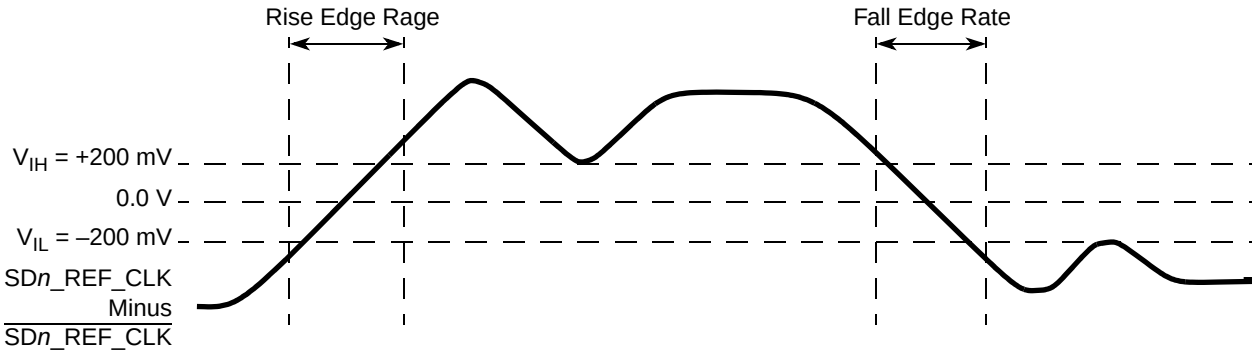


Figure 31. Differential Measurement Points for Rise and Fall Time

11 Enhanced Local Bus

This section describes the DC and AC electrical specifications for the local bus interface.

11.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface.

Table 44. Local Bus DC Electrical Characteristics at 3.3 V

Parameter	Symbol	Min	Max	Unit
High-level input voltage for Rev 1.0	V_{IH}	2.0	LV_{DD} + 0.3	V
High-level input voltage for Rev 2.x or later	V_{IH}	2.1	LV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current, (V_{IN}[1] = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	±5	μA
High-level output voltage, (LV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	LV_{DD} – 0.2	—	V
Low-level output voltage, (LV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.2	V

Note: The parameters stated in above table are valid for all revisions unless explicitly mentioned.

11.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface.

Table 45. Local Bus General Timing Parameters

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
LALE output rise to LCLK negative edge	$t_{LALEHOV}$	—	3.0	ns	
LALE output fall to LCLK negative edge	$t_{LALETOT1}$	–1.5	—	ns	5
LALE output fall to LCLK negative edge	$t_{LALETOT2}$	–5.0	—	ns	6
LALE output fall to LCLK negative edge	$t_{LALETOT3}$	–4.5	—	ns	7
Local bus clock to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD	t_{LBKHOZ}	—	4	ns	8

13 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interface.

13.1 I^2C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interface.

Table 48. I^2C DC Electrical Characteristics

At recommended operating conditions with NV_{DD} of 3.3 V ± 0.3 V.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage level	V_{IH}	$0.7 \times NV_{DD}$	$NV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times NV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times NV_{DD}$	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	
Input current, ($0 V \le V_{IN} \le NV_{DD}$)	I_{IN}	—	± 5	μA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if NV_{DD} is switched off.

13.2 I^2C AC Electrical Specifications

This table provides the AC timing parameters for the I^2C interface.

Table 49. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 48).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns

Table 51. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol[1]	Min	Max	Unit	Note
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

This table shows the PCI AC timing specifications at 33 MHz.

Table 52. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol[1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

This figure provides the AC test load for PCI.

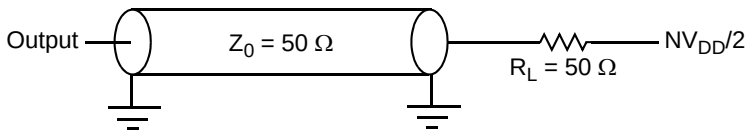
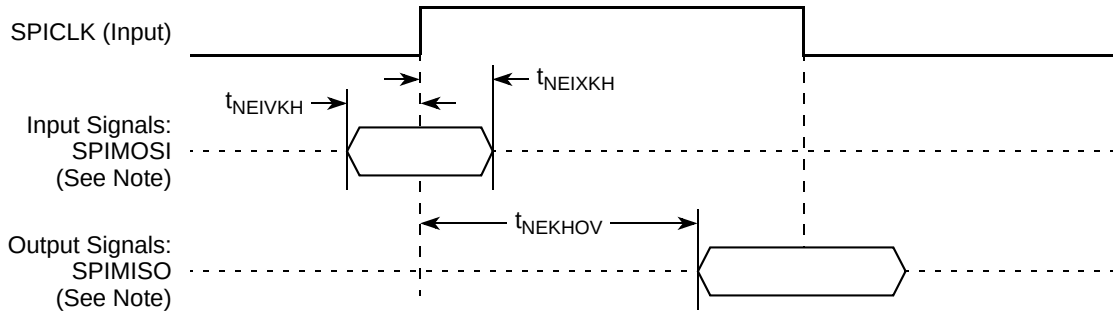


Figure 48. PCI AC Test Load

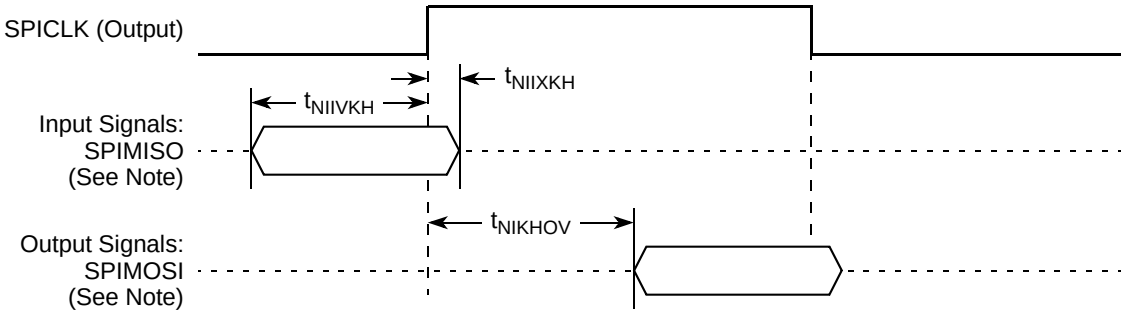
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 54. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 55. SPI AC Timing in Master Mode (Internal Clock) Diagram

19 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8313E is available in a thermally enhanced plastic ball grid array (TEPBGAII), see Section 19.1, "Package Parameters for the MPC8313E TEPBGAII," and Section 19.2, "Mechanical Dimensions of the MPC8313E TEPBGAII," for information on the TEPBGAII.

19.1 Package Parameters for the MPC8313E TEPBGAII

The package parameters are as provided in the following list. The package type is 27 mm × 27 mm, 516 TEPBGAII.

Package outline	27 mm × 27 mm
Interconnects	516
Pitch	1.00 mm
Module height (typical)	2.25 mm
Solder Balls	96.5 Sn/3.5 Ag(VR package) , 62 Sn/36 Pb/2 Ag (ZQ package) Ball diameter (typical)
0.6 mm	

19.3 Pinout Listings

This table provides the pin-out listing for the MPC8313E, TEPBGAII package.

Table 62. MPC8313E TEPBGAII Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Note
DDR Memory Controller Interface				
MEMC_MDQ0	A8	I/O	GV_{DD}	—
MEMC_MDQ1	A9	I/O	GV_{DD}	—
MEMC_MDQ2	C10	I/O	GV_{DD}	—
MEMC_MDQ3	C9	I/O	GV_{DD}	—
MEMC_MDQ4	E9	I/O	GV_{DD}	—
MEMC_MDQ5	E11	I/O	GV_{DD}	—
MEMC_MDQ6	E10	I/O	GV_{DD}	—
MEMC_MDQ7	C8	I/O	GV_{DD}	—
MEMC_MDQ8	E8	I/O	GV_{DD}	—
MEMC_MDQ9	A6	I/O	GV_{DD}	—
MEMC_MDQ10	B6	I/O	GV_{DD}	—
MEMC_MDQ11	C6	I/O	GV_{DD}	—
MEMC_MDQ12	C7	I/O	GV_{DD}	—
MEMC_MDQ13	D7	I/O	GV_{DD}	—
MEMC_MDQ14	D6	I/O	GV_{DD}	—
MEMC_MDQ15	A5	I/O	GV_{DD}	—
MEMC_MDQ16	A19	I/O	GV_{DD}	—
MEMC_MDQ17	D18	I/O	GV_{DD}	—
MEMC_MDQ18	A17	I/O	GV_{DD}	—
MEMC_MDQ19	E17	I/O	GV_{DD}	—
MEMC_MDQ20	E16	I/O	GV_{DD}	—
MEMC_MDQ21	C18	I/O	GV_{DD}	—
MEMC_MDQ22	D19	I/O	GV_{DD}	—
MEMC_MDQ23	C19	I/O	GV_{DD}	—
MEMC_MDQ24	E19	I/O	GV_{DD}	—
MEMC_MDQ25	A22	I/O	GV_{DD}	—
MEMC_MDQ26	C21	I/O	GV_{DD}	—
MEMC_MDQ27	C20	I/O	GV_{DD}	—
MEMC_MDQ28	A21	I/O	GV_{DD}	—

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LA14/TSEC_1588_TRIG1	L24	O	LV_{DD}	8
LA15/TSEC_1588_ALARM2	K26	O	LV_{DD}	8
DUART				
UART_SOUT1/MSRCID0	N2	O	NV_{DD}	—
UART_SIN1/MSRCID1	M5	I/O	NV_{DD}	—
$\overline{\text{UART\_CTS1}}$/GPIO8/MSRCID2	M1	I/O	NV_{DD}	—
$\overline{\text{UART\_RTS1}}$/GPIO9/MSRCID3	K1	I/O	NV_{DD}	—
UART_SOUT2/MSRCID4/TSEC_1588_CLK	M3	O	NV_{DD}	8
UART_SIN2/MDVAL/TSEC_1588_GCLK	L1	I/O	NV_{DD}	8
$\overline{\text{UART\_CTS2}}$/TSEC_1588_PP1	L5	I/O	NV_{DD}	8
$\overline{\text{UART\_RTS2}}$/TSEC_1588_PP2	L3	I/O	NV_{DD}	8
I^2C interface				
IIC1_SDA/$\overline{\text{CKSTOP\_OUT}}$/TSEC_1588_TRIG1	J4	I/O	NV_{DD}	2, 8
IIC1_SCL/$\overline{\text{CKSTOP\_IN}}$/TSEC_1588_ALARM2	J2	I/O	NV_{DD}	2, 8
IIC2_SDA/PMC_PWR_OK/GPIO10	J3	I/O	NV_{DD}	2
IIC2_SCL/GPIO11	H5	I/O	NV_{DD}	2
Interrupts				
$\overline{\text{MCP\_OUT}}$	G5	O	NV_{DD}	2
$\overline{\text{IRQ0}}$/$\overline{\text{MCP\_IN}}$	K5	I	NV_{DD}	—
$\overline{\text{IRQ1}}$	K4	I	NV_{DD}	—
$\overline{\text{IRQ2}}$	K2	I	NV_{DD}	—
$\overline{\text{IRQ3}}$/$\overline{\text{CKSTOP\_OUT}}$	K3	I/O	NV_{DD}	—
$\overline{\text{IRQ4}}$/$\overline{\text{CKSTOP\_IN}}$/GPIO12	J1	I/O	NV_{DD}	—
Configuration				
$\overline{\text{CFG\_CLKIN\_DIV}}$	D5	I	NV_{DD}	—
EXT_PWR_CTRL	J5	O	NV_{DD}	—
CFG_LBIU_MUX_EN	R24	I	NV_{DD}	—
JTAG				
TCK	E1	I	NV_{DD}	—
TDI	E2	I	NV_{DD}	4
TDO	E3	O	NV_{DD}	3

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TMS	E4	I	NV_{DD}	4
$\overline{\text{TRST}}$	E5	I	NV_{DD}	4
TEST				
TEST_MODE	F4	I	NV_{DD}	6
DEBUG				
$\overline{\text{QUIESCE}}$	F5	O	NV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	F2	I/O	NV_{DD}	1
$\overline{\text{PORESET}}$	F3	I	NV_{DD}	—
$\overline{\text{SRESET}}$	F1	I	NV_{DD}	—
Clocks				
SYS_CR_CLK_IN	U26	I	NV_{DD}	—
SYS_CR_CLK_OUT	U25	O	NV_{DD}	—
SYS_CLK_IN	U23	I	NV_{DD}	—
USB_CR_CLK_IN	T26	I	NV_{DD}	—
USB_CR_CLK_OUT	R26	O	NV_{DD}	—
USB_CLK_IN	T22	I	NV_{DD}	—
PCI_SYNC_OUT	U24	O	NV_{DD}	3
RTC_PIT_CLOCK	R22	I	NV_{DD}	—
PCI_SYNC_IN	T24	I	NV_{DD}	—
MISC				
THERM0	N1	I	NV_{DD}	7
THERM1	N3	I	NV_{DD}	7
PCI				
$\overline{\text{PCI\_INTA}}$	AF7	O	NV_{DD}	—
$\overline{\text{PCI\_RESET\_OUT}}$	AB11	O	NV_{DD}	—
PCI_AD0	AB20	I/O	NV_{DD}	—
PCI_AD1	AF23	I/O	NV_{DD}	—
PCI_AD2	AF22	I/O	NV_{DD}	—
PCI_AD3	AB19	I/O	NV_{DD}	—
PCI_AD4	AE22	I/O	NV_{DD}	—
PCI_AD5	AF21	I/O	NV_{DD}	—

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

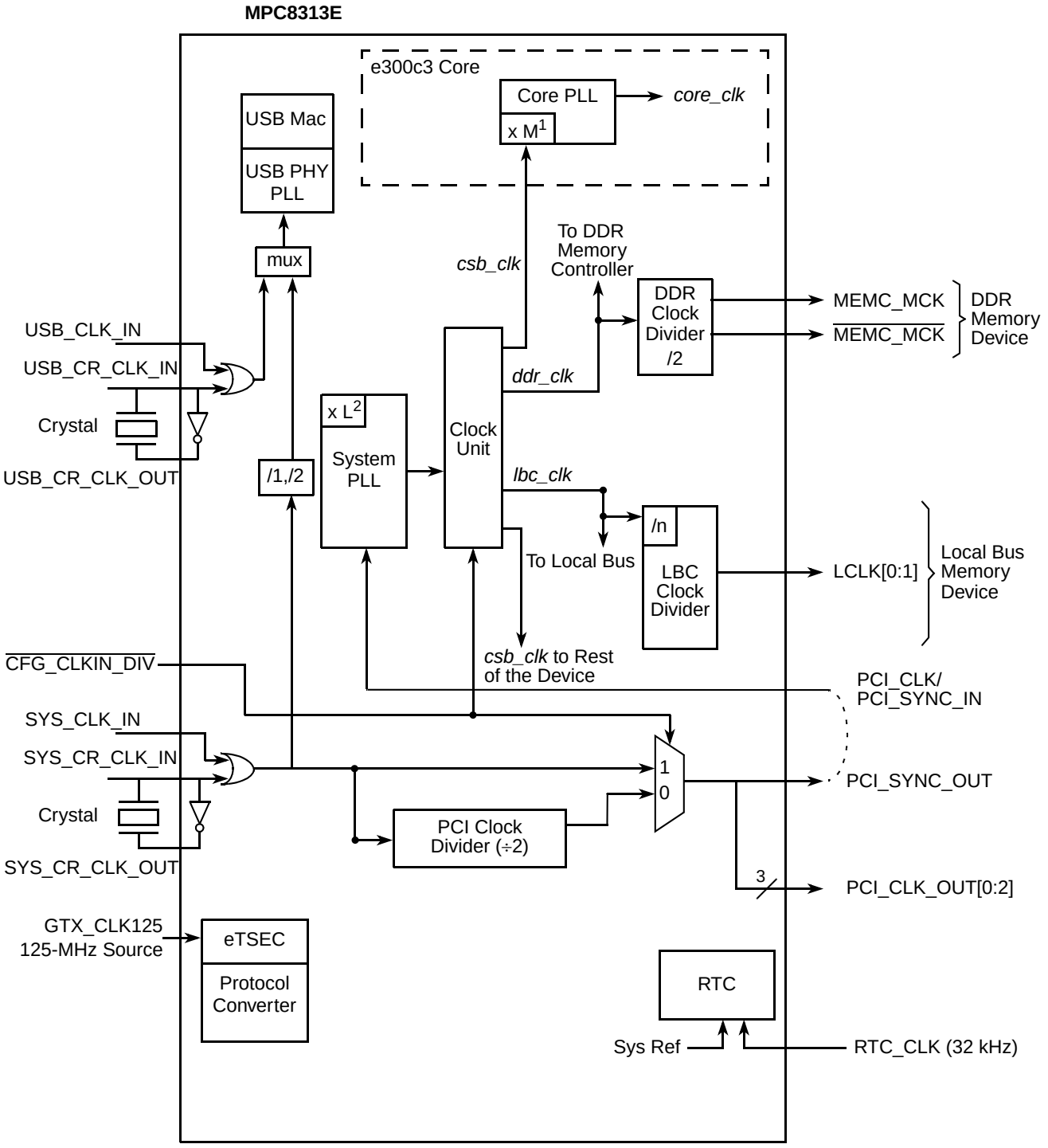
Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_AD6	AD19	I/O	NV_{DD}	—
PCI_AD7	AD20	I/O	NV_{DD}	—
PCI_AD8	AC18	I/O	NV_{DD}	—
PCI_AD9	AD18	I/O	NV_{DD}	—
PCI_AD10	AB18	I/O	NV_{DD}	—
PCI_AD11	AE19	I/O	NV_{DD}	—
PCI_AD12	AB17	I/O	NV_{DD}	—
PCI_AD13	AE18	I/O	NV_{DD}	—
PCI_AD14	AD17	I/O	NV_{DD}	—
PCI_AD15	AF19	I/O	NV_{DD}	—
PCI_AD16	AB14	I/O	NV_{DD}	—
PCI_AD17	AF15	I/O	NV_{DD}	—
PCI_AD18	AD14	I/O	NV_{DD}	—
PCI_AD19	AE14	I/O	NV_{DD}	—
PCI_AD20	AF12	I/O	NV_{DD}	—
PCI_AD21	AE11	I/O	NV_{DD}	—
PCI_AD22	AD12	I/O	NV_{DD}	—
PCI_AD23	AB13	I/O	NV_{DD}	—
PCI_AD24	AF9	I/O	NV_{DD}	—
PCI_AD25	AD11	I/O	NV_{DD}	—
PCI_AD26	AE10	I/O	NV_{DD}	—
PCI_AD27	AB12	I/O	NV_{DD}	—
PCI_AD28	AD10	I/O	NV_{DD}	—
PCI_AD29	AC10	I/O	NV_{DD}	—
PCI_AD30	AF10	I/O	NV_{DD}	—
PCI_AD31	AF8	I/O	NV_{DD}	—
PCI_C/$\overline{BE0}$	AC19	I/O	NV_{DD}	—
PCI_C/$\overline{BE1}$	AB15	I/O	NV_{DD}	—
PCI_C/$\overline{BE2}$	AF14	I/O	NV_{DD}	—
PCI_C/$\overline{BE3}$	AF11	I/O	NV_{DD}	—
PCI_PAR	AD16	I/O	NV_{DD}	—
$\overline{PCI\_FRAME}$	AF16	I/O	NV_{DD}	5

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
RXB	R1	I		—
$\overline{\text{RXB}}$	P1	I		—
SD_IMP_CAL_RX	V5	I		200 Ω ± 10% to GND
$\overline{\text{SD\_REF\_CLK}}$	T5	I		—
SD_REF_CLK	T4	I		—
SD_PLL_TPD	T2	O		—
SD_IMP_CAL_TX	N5	I		100 Ω ± 10% to GND
SDAVDD	R5	I/O		—
SD_PLL_TPA_ANA	R4	O		—
SDAVSS	R3	I/O		—
USB PHY				
USB_DP	P26	I/O		—
USB_DM	N26	I/O		—
USB_VBUS	P24	I/O		—
USB_TPA	L26	I/O		—
USB_RBIAS	M24	I/O		—
USB_PLL_PWR3	M26	I/O		—
USB_PLL_GND	N24	I/O		—
USB_PLL_PWR1	N25	I/O		—
USB_VSSA_BIAS	M25	I/O		—
USB_VDDA_BIAS	M22	I/O		—
USB_VSSA	N22	I/O		—
USB_VDDA	P22	I/O		—
GTM/USB				
USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2/LSRCID0	AD23	I/O	NV_{DD}	—
USBDR_PWRFAULT/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$/ LSRCID1	AE23	I/O	NV_{DD}	—
USBDR_PCTL0/$\overline{\text{GTM1\_TOUT1}}$/LSRCID2	AC22	O	NV_{DD}	—
USBDR_PCTL1/LBC_PM_REF_10/LSRCID3	AB21	O	NV_{DD}	—

20 Clocking

This figure shows the internal distribution of clocks within the MPC8313E.



1 Multiplication factor M = 1, 1.5, 2, 2.5, and 3. Value is decided by RCWLR[COREPLL].
2 Multiplication factor L = 2, 3, 4, 5, and 6. Value is decided by RCWLR[SPMF].

Figure 57. MPC8313E Clock Subsystem

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)
T_B = board temperature at the package perimeter (°C)
$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51–8
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

21.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)
T_T = thermocouple temperature on top of package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

21.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to- ambient thermal resistance (°C/W)

22.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1}, AV_{DD2}, and $SDAV_{DD}$, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 58, one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

This figure shows the PLL power supply filter circuits.

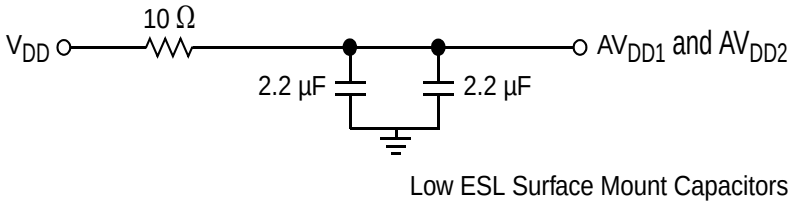
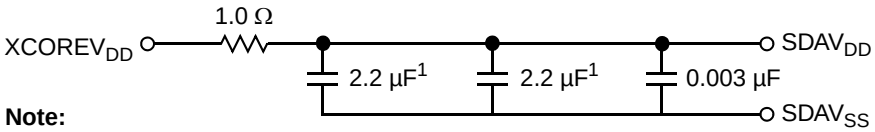


Figure 58. PLL Power Supply Filter Circuit

The $SDAV_{DD}$ signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit like the one shown in Figure 59. For maximum effectiveness, the filter circuit should be placed as closely as possible to the $SDAV_{DD}$ ball to ensure it filters out as much noise as possible. The ground connection should be near the $SDAV_{DD}$ ball. The 0.003-µF capacitor is closest to the ball, followed by the two 2.2-µF capacitors, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from traces from $SDAV_{DD}$ to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.



Note:
1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 59. SerDes PLL Power Supply Filter Circuit

Note the following:

- $SDAV_{DD}$ should be a filtered version of $XCOREV_{DD}$.

24 Revision History

This table summarizes a revision history for this document.

Table 73. Document Revision History

Rev. Number	Date	Substantive Change(s)
4	11/2011	• In Table 2, added following notes: – Note 3: Min temperature is specified with T_A; Max temperature is specified with T_J – Note 4: All Power rails must be connected and power applied to the MPC8313 even if the IP interfaces are not used. – Note 5: All I/O pins should be interfaced with peripherals operating at same voltage level. – Note 6: This voltage is the input to the filter discussed in Section 22.2, “PLL Power Supply Filtering.” and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter • Decoupled PCI_CLK and SYS_CLK_IN rise and fall times in Table 8. Relaxed maximum rise/fall time of SYS_CLK_IN to 4ns. • Added a note in Table 27 stating “The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm." • In Table 30: – Changed max value of t_{skrgt} in “Data to clock input skew (at receiver)” row from 2.8 to 2.6. – Added Note 7, stating that, “The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm.” • Added a note stating “eTSEC should be interfaced with peripheral operating at same voltage level” in Section 8.1.1, “TSEC DC Electrical Characteristics.” • TSEC1_MDC and TSEC_MDIO are powered at 3.3V by NVDD. Replaced LVDDA/LVDDB with NVDD and removed instances of 2.5V at several places in Section 8.5, “Ethernet Management Interface Electrical Characteristics.” • In Table 43, changed min/max values of t_{CLK_TOL} from 0.05 to 0.005. • In Table 62: – Added Note 2 for LGPL4 in showing LGPL4 as open-drain. – Removed Note 2 from TSEC1_MDIO. – Added Note 10: This pin has an internal pull-up. – Added Note 11: This pin has an internal pull-down. – Added Note 12: “In MII mode, GTX_CLK should be pulled down by 300 Ω to V_{SS}” to TSEC1_GTX_CLK and TSEC2_GTX_CLK. • In Section 19.1, “Package Parameters for the MPC8313E TEPBGAII,” replaced "5.5 Sn/0.5 Cu/4 Ag" with "Sn/3.5 Ag." • Added foot note 3 in Table 65 stating “The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.” • In Table 72: – Added AD = 266 and D = 266. – Added “C = 2.2” in “Revision level” column. – Added Note 4. • Changed resitor from 1.0 Ω to 10 Ω in Figure 58. • Replaced LCCR with LCRR throughout. • Added high-speed to USB Phy description.
3	01/2009	• Table 72, in column aa, changed to AG = 400 MHz.
2.2	12/2008	• Made cross-references active for sections, figures, and tables.
2.1	12/2008	• Added Figure 2, after Table 2 and renumbered the following figures.