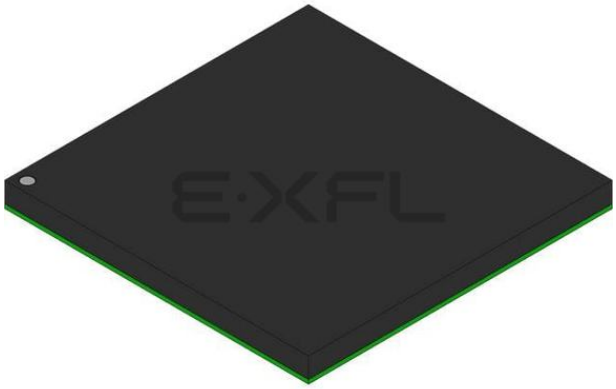

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300c3 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 267MHz |
| Co-Processors/DSP | Security; SEC 2.2 |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | USB 2.0 + PHY (1) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography |
| Package / Case | 516-BBGA Exposed Pad |
| Supplier Device Package | 516-TEPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8313evraddb |

## 1.6 USB Dual-Role Controller

The MPC8313E USB controller includes the following features:

- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Compatible with *Universal Serial Bus Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI + low pin interface (ULPI) or on-chip USB 2.0 full-speed/high-speed PHY

## 1.7 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8313E eTSECs include the following features:

- Two RGMII/SGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3®, 802.3u®, 802.3x®, 802.3z®, 802.3au®, and 802.3ab®
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status
- Three-speed support (10/100/1000 Mbps)
- On-chip high-speed serial interface to external SGMII PHY interface
- Support for IEEE Std 1588™
- Support for two full-duplex FIFO interface modes
- Multiple PHY interface configuration
- TCP/IP acceleration and QoS features available
- IP v4 and IP v6 header recognition on receive
- IP v4 header checksum verification and generation
- TCP and UDP checksum verification and generation
- Per-packet configurable acceleration
- Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2®, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
- Transmission from up to eight physical queues.
- Reception to up to eight physical queues

### 9.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low-phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters for SGMII protocol.

**Table 39. SerDes Reference Clock Common AC Parameters**

At recommended operating conditions with $XV_{DD\_SRDS1}$ or $XV_{DD\_SRDS2}$ = 1.0 V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Rising edge rate | Rise edge rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Falling edge rate | Fall edge rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Differential input high voltage | $V_{IH}$ | +200 | — | mV | 2 |
| Differential input low voltage | $V_{IL}$ | — | –200 | mV | 2 |
| Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn\_REF\_CLK}}$) matching | Rise-fall matching | — | 20 | % | 1, 4 |

**Notes:**
1. Measurement taken from single-ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 31.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point, where SD*n*_REF_CLK rising meets $\overline{\text{SD}n\text{\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK should be compared to the fall edge rate of $\overline{\text{SD}n\text{\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 32.

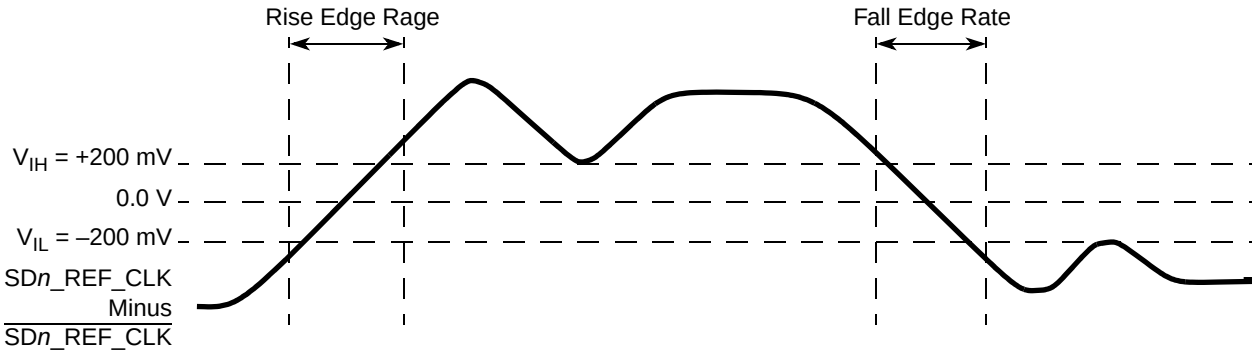



**Figure 31. Differential Measurement Points for Rise and Fall Time**

**Table 45. Local Bus General Timing Parameters (continued)**

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|

**Notes**:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one (1).
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $NV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times NV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ and $t_{LALETOT1}$ should be used when RCWH[LALE] is not set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ and $t_{LALETOT2}$ should be used when RCWH[LALE] is set and the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ and $t_{LALETOT3}$ should be used when RCWH[LALE] is set and the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This figure provides the AC test load for the local bus.

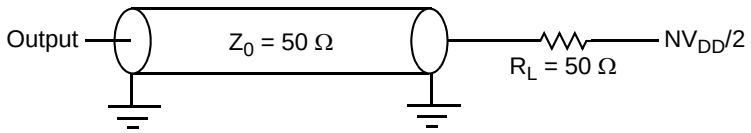



**Figure 36. Local Bus AC Test Load**

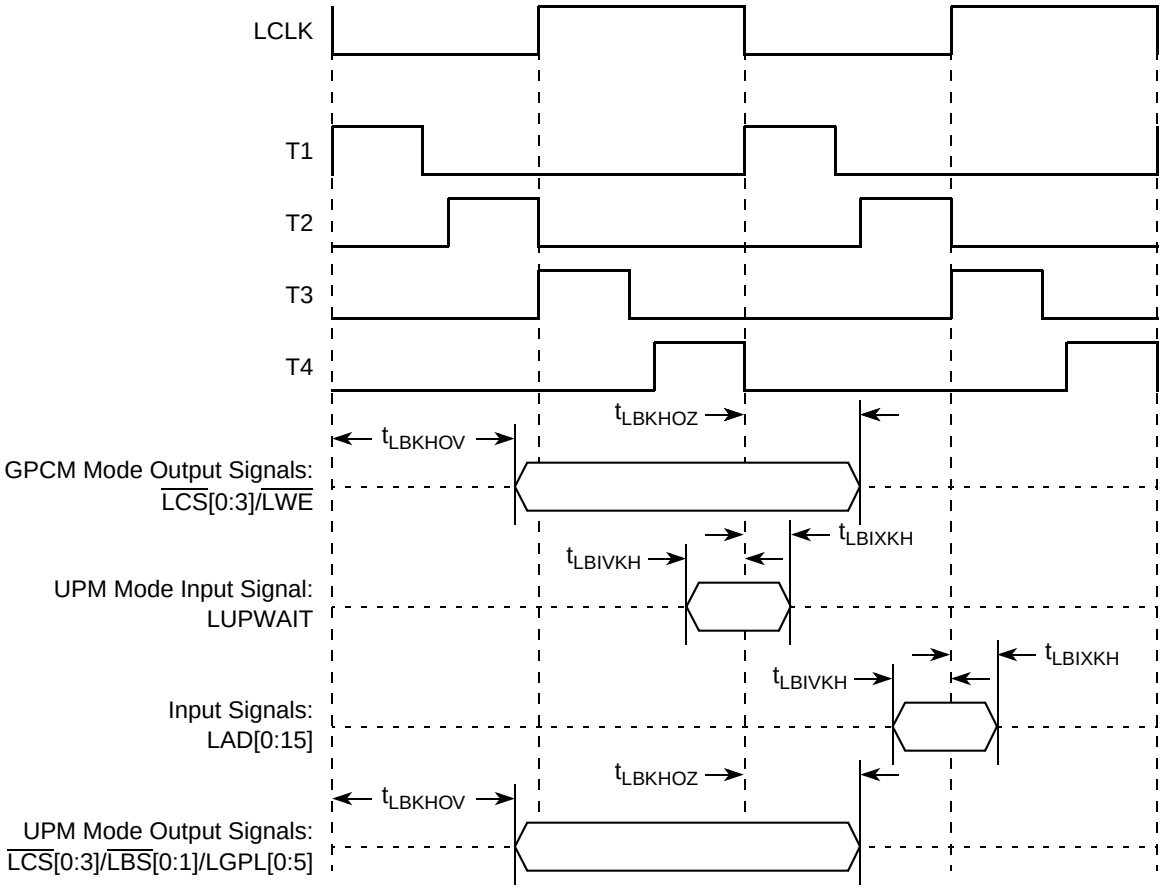



**Figure 39. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4**

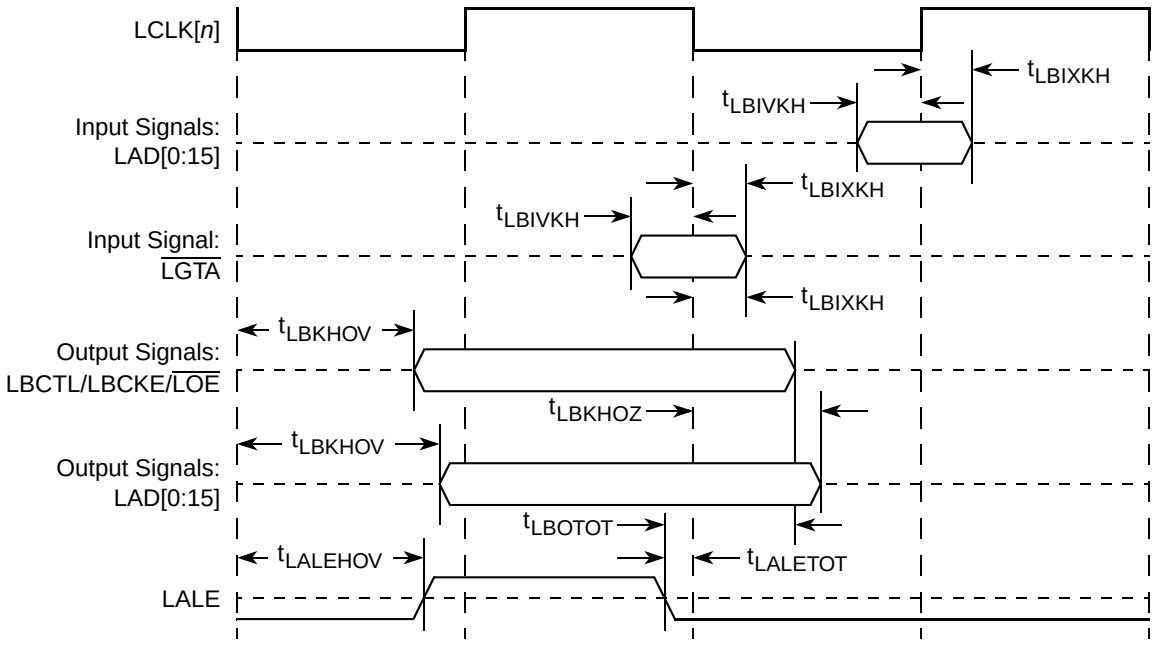



**Figure 40. Local Bus Signals, LALE with Respect to LCLK**

# 12 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

## 12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE Std 1149.1 (JTAG) interface.

**Table 46. JTAG Interface DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 2.1 | $NV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | — | ±5 | μA |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |

## 12.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std 1149.1 (JTAG) interface. This table provides the JTAG AC timing specifications as defined in Figure 41 through Figure 45.

**Table 47. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)[1]**

At recommended operating conditions (see Table 2).

| Parameter | Symbol[2] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | |
| JTAG external clock pulse width measured at 1.4 V | $t_{JTKHKL}$ | 15 | — | ns | |
| JTAG external clock rise and fall times | $t_{JTGR}$ & $t_{JTGF}$ | 0 | 2 | ns | |
| $\overline{TRST}$ assert time | $t_{TRST}$ | 25 | — | ns | 3 |
| Input setup times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDVKH}$<br>$t_{JTIVKH}$ | <br>4<br>4 | <br>—<br>— | ns | 4 |
| Input hold times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDXKH}$<br>$t_{JTIXKH}$ | <br>10<br>10 | <br>—<br>— | ns | 4 |
| Valid times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDV}$<br>$t_{JTKLOV}$ | <br>2<br>2 | <br>11<br>11 | ns | 5 |
| Output hold times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | <br>2<br>2 | <br>—<br>— | ns | 5 |

# 13 $I^2C$

This section describes the DC and AC electrical characteristics for the $I^2C$ interface.

## 13.1 $I^2C$ DC Electrical Characteristics

This table provides the DC electrical characteristics for the $I^2C$ interface.

**Table 48. $I^2C$ DC Electrical Characteristics**

At recommended operating conditions with $NV_{DD}$ of 3.3 V ± 0.3 V.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input high voltage level | $V_{IH}$ | $0.7 \times NV_{DD}$ | $NV_{DD} + 0.3$ | V | |
| Input low voltage level | $V_{IL}$ | –0.3 | $0.3 \times NV_{DD}$ | V | |
| Low level output voltage | $V_{OL}$ | 0 | $0.2 \times NV_{DD}$ | V | 1 |
| Output fall time from $V_{IH}$(min) to $V_{IL}$(max) with a bus capacitance from 10 to 400 pF | $t_{I2KLKV}$ | $20 + 0.1 \times C_B$ | 250 | ns | 2 |
| Pulse width of spikes which must be suppressed by the input filter | $t_{I2KHKL}$ | 0 | 50 | ns | 3 |
| Capacitance for each I/O pin | $C_I$ | — | 10 | pF | |
| Input current, ($0 V \le V_{IN} \le NV_{DD}$) | $I_{IN}$ | — | ± 5 | μA | 4 |

**Notes:**
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. $C_B$ = capacitance of one bus line in pF.
3. Refer to the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if $NV_{DD}$ is switched off.

## 13.2 $I^2C$ AC Electrical Specifications

This table provides the AC timing parameters for the $I^2C$ interface.

**Table 49. $I^2C$ AC Electrical Specifications**

All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 48).

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| SCL clock frequency | $f_{I2C}$ | 0 | 400 | kHz |
| Low period of the SCL clock | $t_{I2CL}$ | 1.3 | — | μs |
| High period of the SCL clock | $t_{I2CH}$ | 0.6 | — | μs |
| Setup time for a repeated START condition | $t_{I2SVKH}$ | 0.6 | — | μs |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | $t_{I2SXKL}$ | 0.6 | — | μs |
| Data setup time | $t_{I2DVKH}$ | 100 | — | ns |

**Table 49. I²C AC Electrical Specifications (continued)**

All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 48).

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| Data hold time:<br>CBUS compatible masters<br>I²C bus devices | $t_{I2DXKL}$ | <br>—<br>0[2] | <br>—<br>0.9[3] | µs |
| Fall time of both SDA and SCL signals[5] | $t_{I2CF}$ | — | 300 | ns |
| Setup time for STOP condition | $t_{I2PVKH}$ | 0.6 | — | µs |
| Bus free time between a STOP and START condition | $t_{I2KHDX}$ | 1.3 | — | µs |
| Noise margin at the LOW level for each connected device (including hysteresis) | $V_{NL}$ | $0.1 \times NV_{DD}$ | — | V |
| Noise margin at the HIGH level for each connected device (including hysteresis) | $V_{NH}$ | $0.2 \times NV_{DD}$ | — | V |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{I2DVKH}$ symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{I2SXKL}$ symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the $t_{I2C}$ clock reference (K) going to the low (L) state or hold time. Also, $t_{I2PVKH}$ symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The MPC8313E provides a hold time of at least 300 ns for the SDA signal (referred to the $V_{IHmin}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{I2DVKH}$ has only to be met if the device does not stretch the LOW period ($t_{I2CL}$) of the SCL signal.
4. $C_B$ = capacitance of one bus line in pF.
5. The MPC8313E does not follow the *I²C-BUS Specifications, Version 2.1,* regarding the $t_{I2CF}$ AC parameter.

This figure provides the AC test load for the I²C.

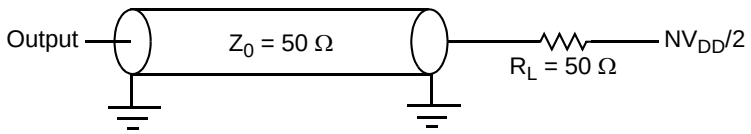



**Figure 46. I²C AC Test Load**

This figure shows the PCI input AC timing conditions.

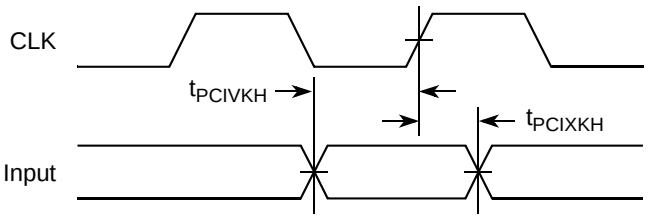



**Figure 49. PCI Input AC Timing Measurement Conditions**

This figure shows the PCI output AC timing conditions.

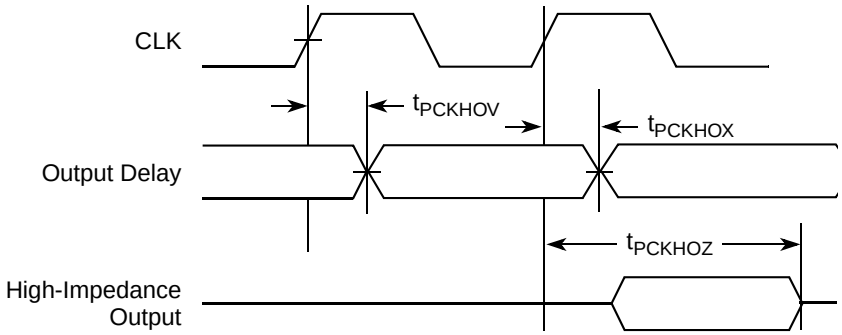



**Figure 50. PCI Output AC Timing Measurement Condition**

# 15 Timers

This section describes the DC and AC electrical specifications for the timers.

## 15.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the MPC8313E timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

**Table 53. Timers DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |
| Input high voltage | $V_{IH}$ | — | 2.1 | $NV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le NV_{DD}$ | — | ±5 | μA |

This table provides the DC electrical characteristics for the GPIO when the GPIO pins are operating from a 2.5-V supply.

**Table 56. GPIO (When Operating at 2.5 V) DC Electrical Characteristics[1]**

| Parameters | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage 2.5 V | $NV_{DD}$ | — | | 2.37 | 2.63 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –1.0 mA | $NV_{DD}$ = min | 2.00 | $NV_{DD}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 1.0 mA | $NV_{DD}$ = min | $V_{SS}$ – 0.3 | 0.40 | V |
| Input high voltage | $V_{IH}$ | — | $NV_{DD}$ = min | 1.7 | $NV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | $NV_{DD}$ = min | –0.3 | 0.70 | V |
| Input high current | $I_{IH}$ | $V_{IN}$ = $NV_{DD}$ | | — | 10 | μA |
| Input low current | $I_{IL}$ | $V_{IN}$ = $V_{SS}$ | | –15 | — | μA |

**Note:**

1. This specification only applies to GPIO pins that are operating from a 2.5-V supply. See Table 62 for the power supply listed for the individual GPIO signal

## 16.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

**Table 57. GPIO Input AC Timing Specifications[1]**

| Characteristic | Symbol[2] | Min | Unit |
|---|---|---|---|
| GPIO inputs—minimum pulse width | $t_{PIWID}$ | 20 | ns |

**Notes:**

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least $t_{PIWID}$ ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

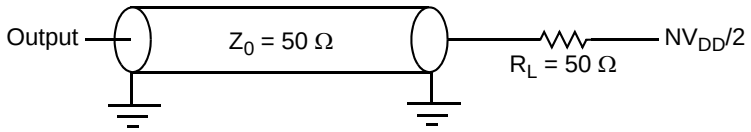



**Figure 52. GPIO AC Test Load**

**Table 62. MPC8313E TEPBGAII Pinout Listing (continued)**

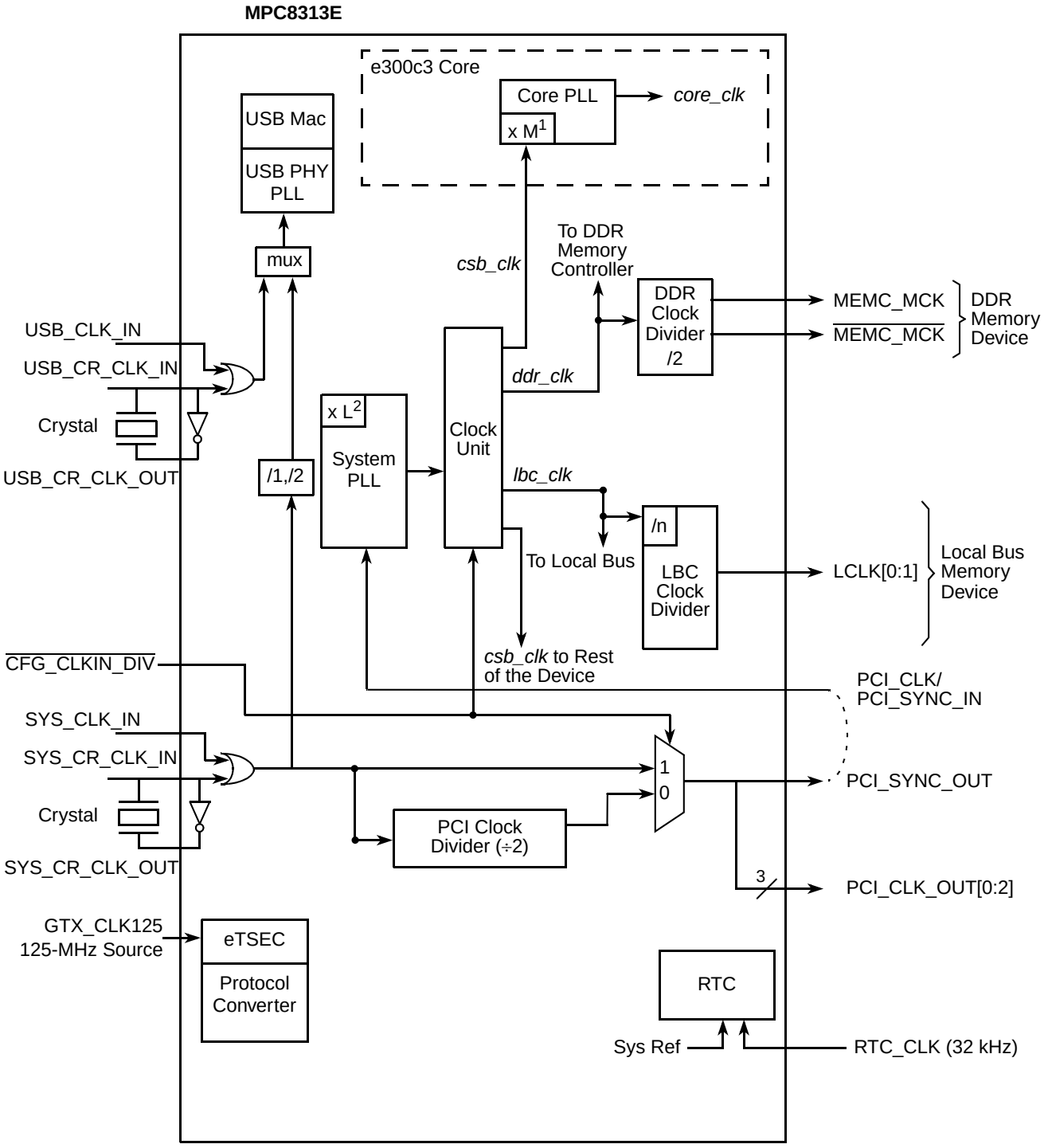
| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| MEMC_MDQ29 | A20 | I/O | $GV_{DD}$ | — |
| MEMC_MDQ30 | C22 | I/O | $GV_{DD}$ | — |
| MEMC_MDQ31 | B22 | I/O | $GV_{DD}$ | — |
| MEMC_MDM0 | B7 | O | $GV_{DD}$ | — |
| MEMC_MDM1 | E6 | O | $GV_{DD}$ | — |
| MEMC_MDM2 | E18 | O | $GV_{DD}$ | — |
| MEMC_MDM3 | E20 | O | $GV_{DD}$ | — |
| MEMC_MDQS0 | A7 | I/O | $GV_{DD}$ | — |
| MEMC_MDQS1 | E7 | I/O | $GV_{DD}$ | — |
| MEMC_MDQS2 | B19 | I/O | $GV_{DD}$ | — |
| MEMC_MDQS3 | A23 | I/O | $GV_{DD}$ | — |
| MEMC_MBA0 | D15 | O | $GV_{DD}$ | — |
| MEMC_MBA1 | A18 | O | $GV_{DD}$ | — |
| MEMC_MBA2 | A15 | O | $GV_{DD}$ | — |
| MEMC_MA0 | E12 | O | $GV_{DD}$ | — |
| MEMC_MA1 | D11 | O | $GV_{DD}$ | — |
| MEMC_MA2 | B11 | O | $GV_{DD}$ | — |
| MEMC_MA3 | A11 | O | $GV_{DD}$ | — |
| MEMC_MA4 | A12 | O | $GV_{DD}$ | — |
| MEMC_MA5 | E13 | O | $GV_{DD}$ | — |
| MEMC_MA6 | C12 | O | $GV_{DD}$ | — |
| MEMC_MA7 | E14 | O | $GV_{DD}$ | — |
| MEMC_MA8 | B15 | O | $GV_{DD}$ | — |
| MEMC_MA9 | C17 | O | $GV_{DD}$ | — |
| MEMC_MA10 | C13 | O | $GV_{DD}$ | — |
| MEMC_MA11 | A16 | O | $GV_{DD}$ | — |
| MEMC_MA12 | C15 | O | $GV_{DD}$ | — |
| MEMC_MA13 | C16 | O | $GV_{DD}$ | — |
| MEMC_MA14 | E15 | O | $GV_{DD}$ | — |
| $\overline{\text{MEMC\_MWE}}$ | B18 | O | $GV_{DD}$ | — |
| $\overline{\text{MEMC\_MRAS}}$ | C11 | O | $GV_{DD}$ | — |
| $\overline{\text{MEMC\_MCAS}}$ | B10 | O | $GV_{DD}$ | — |

**Table 62. MPC8313E TEPBGAII Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| TMS | E4 | I | $NV_{DD}$ | 4 |
| $\overline{\text{TRST}}$ | E5 | I | $NV_{DD}$ | 4 |
| **TEST** | | | | |
| TEST_MODE | F4 | I | $NV_{DD}$ | 6 |
| **DEBUG** | | | | |
| $\overline{\text{QUIESCE}}$ | F5 | O | $NV_{DD}$ | — |
| **System Control** | | | | |
| $\overline{\text{HRESET}}$ | F2 | I/O | $NV_{DD}$ | 1 |
| $\overline{\text{PORESET}}$ | F3 | I | $NV_{DD}$ | — |
| $\overline{\text{SRESET}}$ | F1 | I | $NV_{DD}$ | — |
| **Clocks** | | | | |
| SYS_CR_CLK_IN | U26 | I | $NV_{DD}$ | — |
| SYS_CR_CLK_OUT | U25 | O | $NV_{DD}$ | — |
| SYS_CLK_IN | U23 | I | $NV_{DD}$ | — |
| USB_CR_CLK_IN | T26 | I | $NV_{DD}$ | — |
| USB_CR_CLK_OUT | R26 | O | $NV_{DD}$ | — |
| USB_CLK_IN | T22 | I | $NV_{DD}$ | — |
| PCI_SYNC_OUT | U24 | O | $NV_{DD}$ | 3 |
| RTC_PIT_CLOCK | R22 | I | $NV_{DD}$ | — |
| PCI_SYNC_IN | T24 | I | $NV_{DD}$ | — |
| **MISC** | | | | |
| THERM0 | N1 | I | $NV_{DD}$ | 7 |
| THERM1 | N3 | I | $NV_{DD}$ | 7 |
| **PCI** | | | | |
| $\overline{\text{PCI\_INTA}}$ | AF7 | O | $NV_{DD}$ | — |
| $\overline{\text{PCI\_RESET\_OUT}}$ | AB11 | O | $NV_{DD}$ | — |
| PCI_AD0 | AB20 | I/O | $NV_{DD}$ | — |
| PCI_AD1 | AF23 | I/O | $NV_{DD}$ | — |
| PCI_AD2 | AF22 | I/O | $NV_{DD}$ | — |
| PCI_AD3 | AB19 | I/O | $NV_{DD}$ | — |
| PCI_AD4 | AE22 | I/O | $NV_{DD}$ | — |
| PCI_AD5 | AF21 | I/O | $NV_{DD}$ | — |

# 20 Clocking

This figure shows the internal distribution of clocks within the MPC8313E.




1 Multiplication factor M = 1, 1.5, 2, 2.5, and 3. Value is decided by RCWLR[COREPLL].
2 Multiplication factor L = 2, 3, 4, 5, and 6. Value is decided by RCWLR[SPMF].

**Figure 57. MPC8313E Clock Subsystem**

**Table 63. Configurable Clock Units**

| Unit | Default Frequency | Options |
|---|---|---|
| TSEC1 | *csb_clk* | Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3 |
| TSEC2 | *csb_clk* | Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3 |
| Security Core, $I^2C$, SAP, TPR | *csb_clk* | Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3 |
| USB DR | *csb_clk* | Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3 |
| PCI and DMA complex | *csb_clk* | Off, *csb_clk* |

This table provides the operating frequencies for the MPC8313E TEPBGAII under recommended operating conditions (see Table 2).

**Table 64. Operating Frequencies for TEPBGAII**

| Characteristic[1] | Maximum Operating Frequency | Unit |
|---|---|---|
| e300 core frequency (*core_clk*) | 333 | MHz |
| Coherent system bus frequency (*csb_clk*) | 167 | MHz |
| DDR1/2 memory bus frequency (MCK)[2] | 167 | MHz |
| Local bus frequency (LCLK*n*)[3] | 66 | MHz |
| PCI input frequency (SYS_CLK_IN or PCI_CLK) | 66 | MHz |

**Note:**

1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK[0:1], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM] and SCCR[USBDRCM] must be programmed such that the maximum internal operating frequency of the security core and USB modules do not exceed their respective value listed in this table.
2. The DDR data rate is 2x the DDR memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbc_clk* frequency (depending on LCRR[CLKDIV]), which is in turn, 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

## 20.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. This table shows the multiplication factor encodings for the system PLL.

**Table 65. System PLL Multiplication Factors**

| RCWL[SPMF] | System PLL Multiplication Factor |
|---|---|
| 0000 | Reserved |
| 0001 | Reserved |
| 0010 | × 2 |
| 0011 | × 3 |

## 20.3 Example Clock Frequency Combinations

This table shows several possible frequency combinations that can be selected based on the indicated input reference frequencies, with RCWLR[LBCM] = 0 and RCWLR[DDRCM] =1, such that the LBC operates with a frequency equal to the frequency of *csb_clk* and the DDR controller operates at twice the frequency of *csb_clk*.

**Table 68. System Clock Frequencies**

| | | | | | | LBC(lbc_clk) | | | | e300 Core(core_clk) | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SYS_ CLK_IN/ PCI_CLK | SPMF[1] | VCOD[2] | VCO[3] | CSB (*csb_clk*)[4] | DDR (ddr_clk) | /2 | /4 | /8 | USB ref[5] | × 1 | × 1.5 | × 2 | × 2.5 | × 3 |
| 25.0 | 6 | 2 | 600.0 | 150.0 | 300.0 | — | 37.5 | 18.8 | Note[6] | 150.0 | 225 | 300 | 375 | — |
| 25.0 | 5 | 2 | 500.0 | 125.0 | 250.0 | 62.5 | 31.25 | 15.6 | Note 6 | 125.0 | 188 | 250 | 313 | 375 |
| 33.3 | 5 | 2 | 666.0 | 166.5 | 333.0 | — | 41.63 | 20.8 | Note 6 | 166.5 | 250 | 333 | — | — |
| 33.3 | 4 | 2 | 532.8 | 133.2 | 266.4 | 66.6 | 33.3 | 16.7 | Note 6 | 133.2 | 200 | 266 | 333 | 400 |
| 48.0 | 3 | 2 | 576.0 | 144.0 | 288.0 | — | 36 | 18.0 | 48.0 | 144.0 | 216 | 288 | 360 | — |
| 66.7 | 2 | 2 | 533.4 | 133.3 | 266.7 | 66.7 | 33.34 | 16.7 | Note 6 | 133.3 | 200 | 267 | 333 | 400 |

**Note:**

1. System PLL multiplication factor.
2. System PLL VCO divider.
3. When considering operating frequencies, the valid core VCO operating range of 400–800 MHz must not be violated.
4. Due to erratum eTSEC40, *csb_clk* frequencies of less than 133 MHz do not support gigabit Ethernet data rates. The core frequency must be 333 MHz for gigabit Ethernet operation. This erratum will be fixed in revision 2 silicon.
5. Frequency of USB PLL input reference.
6. USB reference clock must be supplied from a separate source as it must be 24 or 48 MHz, the USB reference must be supplied from a separate external source using USB_CLK_IN.

# 21 Thermal

This section describes the thermal specifications of the MPC8313E.

## 21.1 Thermal Characteristics

This table provides the package thermal characteristics for the 516, 27 × 27 mm TEPBGAII.

**Table 69. Package Thermal Characteristics for TEPBGAII**

| Characteristic | Board Type | Symbol | TEPBGA II | Unit | Note |
|---|---|---|---|---|---|
| Junction-to-ambient natural convection | Single layer board (1s) | $R_{\theta JA}$ | 25 | °C/W | 1, 2 |
| Junction-to-ambient natural convection | Four layer board (2s2p) | $R_{\theta JA}$ | 18 | °C/W | 1, 2, 3 |
| Junction-to-ambient (@200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ | 20 | °C/W | 1, 3 |
| Junction-to-ambient (@200 ft/min) | Four layer board (2s2p) | $R_{\theta JMA}$ | 15 | °C/W | 1, 3 |
| Junction-to-board | — | $R_{\theta JB}$ | 10 | °C/W | 4 |

## 21.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

### 21.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction to case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

$T_J$ = junction temperature (°C)
$T_C$ = case temperature of the package
$R_{\theta JC}$ = junction-to-case thermal resistance
$P_D$ = power dissipation

# 22 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8313E SYS_CLK_IN

## 22.1 System Clocking

The MPC8313E includes three PLLs.

1. The platform PLL ($AV_{DD2}$) generates the platform clock from the externally supplied SYS_CLK_IN input in PCI host mode or SYS_CLK_IN/PCI_SYNC_IN in PCI agent mode. The frequency ratio between the platform and SYS_CLK_IN is selected using the platform PLL ratio configuration bits as described in Section 20.1, “System PLL Configuration.”
2. The e300 core PLL ($AV_{DD1}$) generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 20.2, “Core PLL Configuration.”
3. There is a PLL for the SerDes block.

## 22.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD1}$, $AV_{DD2}$, and $SDAV_{DD}$, respectively). The $AV_{DD}$ level should always be equivalent to $V_{DD}$, and preferably these voltages are derived directly from $V_{DD}$ through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 58, one to each of the five $AV_{DD}$ pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific $AV_{DD}$ pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the $AV_{DD}$ pin, which is on the periphery of package, without the inductance of vias.

This figure shows the PLL power supply filter circuits.

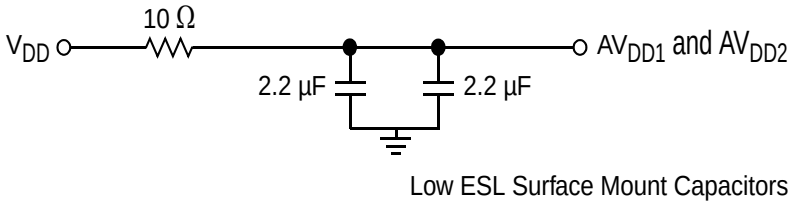
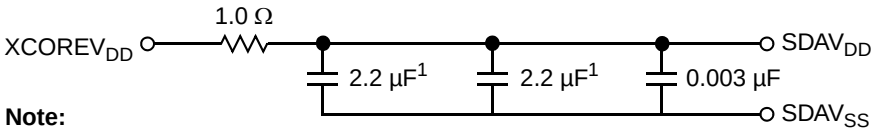



**Figure 58. PLL Power Supply Filter Circuit**

The $SDAV_{DD}$ signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit like the one shown in Figure 59. For maximum effectiveness, the filter circuit should be placed as closely as possible to the $SDAV_{DD}$ ball to ensure it filters out as much noise as possible. The ground connection should be near the $SDAV_{DD}$ ball. The 0.003-µF capacitor is closest to the ball, followed by the two 2.2-µF capacitors, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from traces from $SDAV_{DD}$ to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.

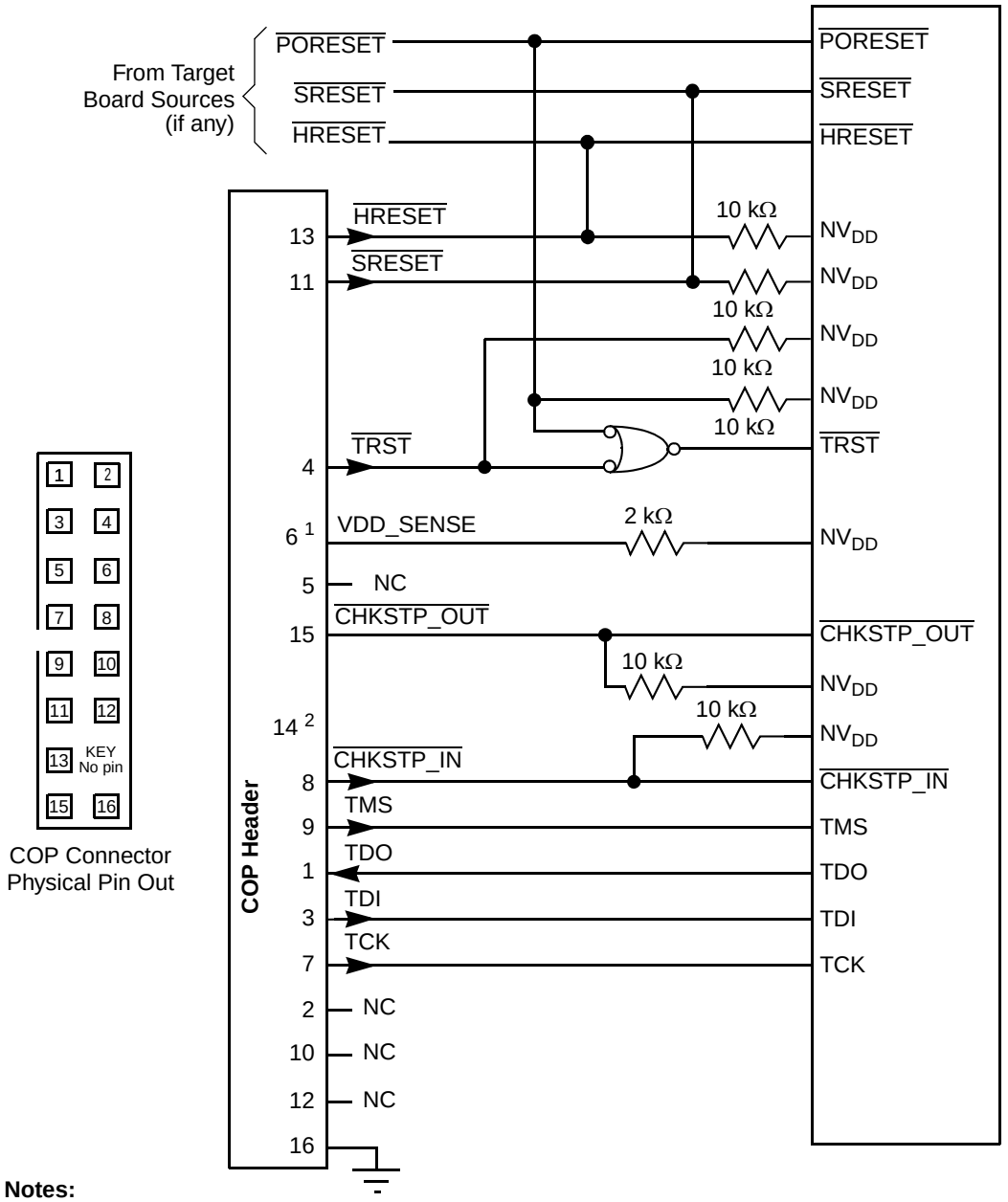



**Note:**
1. An 0805 sized capacitor is recommended for system initial bring-up.

**Figure 59. SerDes PLL Power Supply Filter Circuit**

Note the following:

- $SDAV_{DD}$ should be a filtered version of $XCOREV_{DD}$.




**Notes:**
1. Some systems require power to be fed from the application board into the debugger repeater card via the COP header. In this case the resistor value for VDD_SENSE should be around 20 Ω.
2. Key location; pin 14 is not physically present on the COP header.

**Figure 61. JTAG Interface Connection**

# 23 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 23.1, “Part Numbers Fully Addressed by this Document.”

# 24 Revision History

This table summarizes a revision history for this document.

**Table 73. Document Revision History**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 4 | 11/2011 | • In Table 2, added following notes:<br>– Note 3: Min temperature is specified with $T_A$; Max temperature is specified with $T_J$<br>– Note 4: All Power rails must be connected and power applied to the MPC8313 even if the IP interfaces are not used.<br>– Note 5: All I/O pins should be interfaced with peripherals operating at same voltage level.<br>– Note 6: This voltage is the input to the filter discussed in Section 22.2, “PLL Power Supply Filtering.” and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter<br>• Decoupled PCI_CLK and SYS_CLK_IN rise and fall times in Table 8. Relaxed maximum rise/fall time of SYS_CLK_IN to 4ns.<br>• Added a note in Table 27 stating “The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm."<br>• In Table 30:<br>– Changed max value of $t_{skrgt}$ in “Data to clock input skew (at receiver)” row from 2.8 to 2.6.<br>– Added Note 7, stating that, “The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm.”<br>• Added a note stating “eTSEC should be interfaced with peripheral operating at same voltage level” in Section 8.1.1, “TSEC DC Electrical Characteristics.”<br>• TSEC1_MDC and TSEC_MDIO are powered at 3.3V by NVDD. Replaced LVDDA/LVDDB with NVDD and removed instances of 2.5V at several places in Section 8.5, “Ethernet Management Interface Electrical Characteristics.”<br>• In Table 43, changed min/max values of $t_{CLK\_TOL}$ from 0.05 to 0.005.<br>• In Table 62:<br>– Added Note 2 for LGPL4 in showing LGPL4 as open-drain.<br>– Removed Note 2 from TSEC1_MDIO.<br>– Added Note 10: This pin has an internal pull-up.<br>– Added Note 11: This pin has an internal pull-down.<br>– Added Note 12: “In MII mode, GTX_CLK should be pulled down by 300 Ω to $V_{SS}$” to TSEC1_GTX_CLK and TSEC2_GTX_CLK.<br>• In Section 19.1, “Package Parameters for the MPC8313E TEPBGAII,” replaced "5.5 Sn/0.5 Cu/4 Ag" with "Sn/3.5 Ag."<br>• Added foot note 3 in Table 65 stating “The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.”<br>• In Table 72:<br>– Added AD = 266 and D = 266.<br>– Added “C = 2.2” in “Revision level” column.<br>– Added Note 4.<br>• Changed resitor from 1.0 Ω to 10 Ω in Figure 58.<br>• Replaced LCCR with LCRR throughout.<br>• Added high-speed to USB Phy description. |
| 3 | 01/2009 | • Table 72, in column aa, changed to AG = 400 MHz. |
| 2.2 | 12/2008 | • Made cross-references active for sections, figures, and tables. |
| 2.1 | 12/2008 | • Added Figure 2, after Table 2 and renumbered the following figures. |

**Table 73. Document Revision History (continued)**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 1 | 3/2008 | • In Table 63, added LBC_PM_REF_10 & LSRCID3 as muxed with USBDR_PCTL1<br>• In Table 63, added LSRCID2 as muxed with USBDR_PCTL0<br>• In Table 63, added LSRCID1 as muxed with USBDR_PWRFAULT<br>• In Table 63, added LSRCID0 as muxed with USBDR_DRIVE_VBUS<br>• In Table 63, moved T1, U2,& V2 from $V_{DD}$ to XCOREVDD.<br>• In Table 63, moved P2, R2, & T3 from $V_{SS}$ to XCOREVSS.<br>• In Table 63, moved P5, & U4 from $V_{DD}$ to XPADVDD.<br>• In Table 63, moved P3, & V4 from $V_{SS}$ to XPADVSS.<br>• In Table 63, removed “Double with pad” for $AV_{DD1}$ and $AV_{DD2}$ and moved $AV_{DD1}$ and $AV_{DD2}$ to Power and Ground Supplies section<br>• In Table 63, added impedance control requirements for SD_IMP_CAL_TX (100 ohms to GND) and SD_IMP_CAL_RX (200 ohms to GND).<br>• In Table 63, updated muxing in pinout to show new options for selecting IEEE 1588 functionality. Added footnote 8<br>• In Table 63, updated muxing in pinout to show new LBC ECC boot enable control muxed with eTSEC1_MDC<br>• Added pin type information for power supplies.<br>• Removed N1 and N3 from Vss section of Table 63. Added Therm0 and Therm1 (N1 and N3, respectively). Added note 7 to state: “Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.”<br>• In Table 65 corrected maximum frequency of Local Bus Frequency from “33–66” to 66 MHz<br>• In Table 65 corrected maximum frequency of PCI from “24–66” to 66 MHz<br>• Added “which is determined by RCWLR[COREPLL],” to the note in Section 20.2, “Core PLL Configuration” about the VCO divider.<br>• Added “(VCOD)” next to VCO divider column in Table 68. Added footnote stating that core_clk frequency must not exceed its maximum, so 2.5:1 and 3:1 *core_clk:csb_clk* ratios are invalid for certain *csb_clk* values.<br>• In Table 69, notes were confusing. Added note 3 for VCO column, note 4 for CSB (*csb_clk*) column, note 5 for USB ref column, and note 6 to replace “Note 1”. Clarified note 4 to explain erratum eTSEC40.<br>• In Table 69, updated note 6 to specify USB reference clock frequencies limited to 24 and 48 for rev. 2 silicon.<br>• Replaced Table 71 “Thermal Resistance for TEPBGAII with Heat Sink in Open Flow”.<br>• Removed last row of Table 19.<br>• Removed 200 MHz rows from Table 21 and Table 5.<br>• Changed VIH minimum spec from 2.0 to 2.1 for clock, PIC, JTAG, SPI, and reset pins in Table 9, Table 47, Table 54, Table 59, and Table 61.<br>• Added Figure 4 showing the DDR input timing diagram.<br>• In Table 19, removed “MDM” from the “MDQS-MDQ/MECC/MDM” text under the Parameter column for the tCISKEW parameter. MDM is an output signal and should be removed from the input AC timing spec table (tCISKEW).<br>• Added “and power” to rows 2 and 3 in Table 10<br>• Added the sentence “Once both the power supplies...” and PORESET to Section 2.2, “Power Sequencing,” and Figure 3.<br>• In Figure 35, corrected “USB0_CLK/USB1_CLK/DR_CLK” with “USBDR_CLK”<br>• In Table 42, clarified that AC specs are for ULPI only. |
| 0 | 6/2007 | Initial release. |

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Document Number: MPC8313EEC
Rev. 4
11/2011