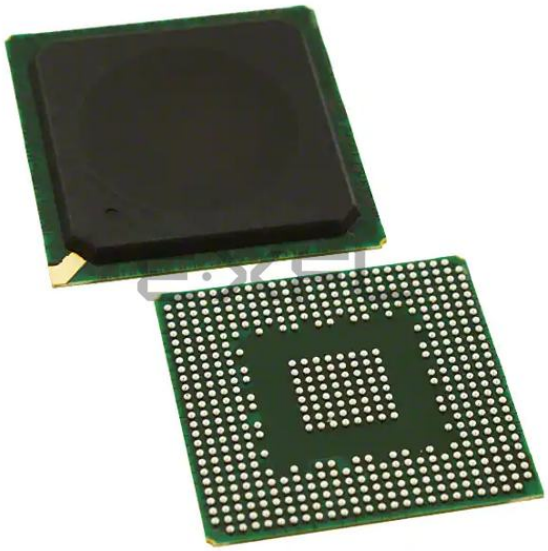

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300c3 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 333MHz |
| Co-Processors/DSP | Security; SEC 2.2 |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | USB 2.0 + PHY (1) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography |
| Package / Case | 516-BBGA Exposed Pad |
| Supplier Device Package | 516-TEPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8313evraff |

## 1.6 USB Dual-Role Controller

The MPC8313E USB controller includes the following features:

- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Compatible with *Universal Serial Bus Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI + low pin interface (ULPI) or on-chip USB 2.0 full-speed/high-speed PHY

## 1.7 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8313E eTSECs include the following features:

- Two RGMII/SGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3®, 802.3u®, 802.3x®, 802.3z®, 802.3au®, and 802.3ab®
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status
- Three-speed support (10/100/1000 Mbps)
- On-chip high-speed serial interface to external SGMII PHY interface
- Support for IEEE Std 1588™
- Support for two full-duplex FIFO interface modes
- Multiple PHY interface configuration
- TCP/IP acceleration and QoS features available
- IP v4 and IP v6 header recognition on receive
- IP v4 header checksum verification and generation
- TCP and UDP checksum verification and generation
- Per-packet configurable acceleration
- Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2®, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
- Transmission from up to eight physical queues.
- Reception to up to eight physical queues

## 1.10 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the MPC8313E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

## 1.11 DMA Controller, Dual $I^2C$, DUART, Local Bus Controller, and Timers

The MPC8313E provides an integrated four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Supports misaligned transfers

There are two $I^2C$ controllers. These synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. The 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8313E local bus controller (LBC) port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The three user programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM or UPM controller. The FCM provides a glueless interface to parallel-bus NAND Flash E2PROM devices. The FCM contains three basic configuration register groups—BR*n*, OR*n*, and FMR. Both may exist in the same system. The local bus can operate at up to 66 MHz.

The MPC8313E system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

# 2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8313E. The MPC8313E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

## 2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

### 2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings[1]**

| Characteristic | | Symbol | Max Value | Unit | Note |
|---|---|---|---|---|---|
| Core supply voltage | | $V_{DD}$ | –0.3 to 1.26 | V | — |
| PLL supply voltage | | $AV_{DD}$ | –0.3 to 1.26 | V | — |
| Core power supply for SerDes transceivers | | $XCOREV_{DD}$ | –0.3 to 1.26 | V | — |
| Pad power supply for SerDes transceivers | | $XPADV_{DD}$ | –0.3 to 1.26 | V | — |
| DDR and DDR2 DRAM I/O voltage | | $GV_{DD}$ | –0.3 to 2.75<br>–0.3 to 1.98 | V | — |
| PCI, local bus, DUART, system control and power management, $I^2C$, and JTAG I/O voltage | | $NV_{DD}/LV_{DD}$ | –0.3 to 3.6 | V | — |
| eTSEC, USB | | $LV_{DDA}/LV_{DDB}$ | –0.3 to 3.6 | V | — |
| Input voltage | DDR DRAM signals | $MV_{IN}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 5 |
| | DDR DRAM reference | $MV_{REF}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 5 |
| | Enhanced three-speed Ethernet signals | $LV_{IN}$ | –0.3 to ($LV_{DDA}$ + 0.3)<br>or<br>–0.3 to ($LV_{DDB}$ + 0.3) | V | 4, 5 |
| | Local bus, DUART, SYS_CLK_IN, system control, and power management, $I^2C$, and JTAG signals | $NV_{IN}$ | –0.3 to ($NV_{DD}$ + 0.3) | V | 3, 5 |
| | PCI | $NV_{IN}$ | –0.3 to ($NV_{DD}$ + 0.3) | V | 6 |
| Storage temperature range | | $T_{STG}$ | –55 to 150 | °C | — |

**Notes:**

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** $MV_{IN}$ must not exceed $GV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** $NV_{IN}$ must not exceed $NV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** $LV_{IN}$ must not exceed $LV_{DDA}/LV_{DDB}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

### 2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the MPC8313E. Note that the values in this table are the recommended and tested operating conditions. If a particular block is given a voltage falling within the range in the Recommended Value column, the MPC8313E is capable of delivering the amount of current listed in the Current Requirement column; this is the maximum current possible. Proper device operation outside of these conditions is not guaranteed.

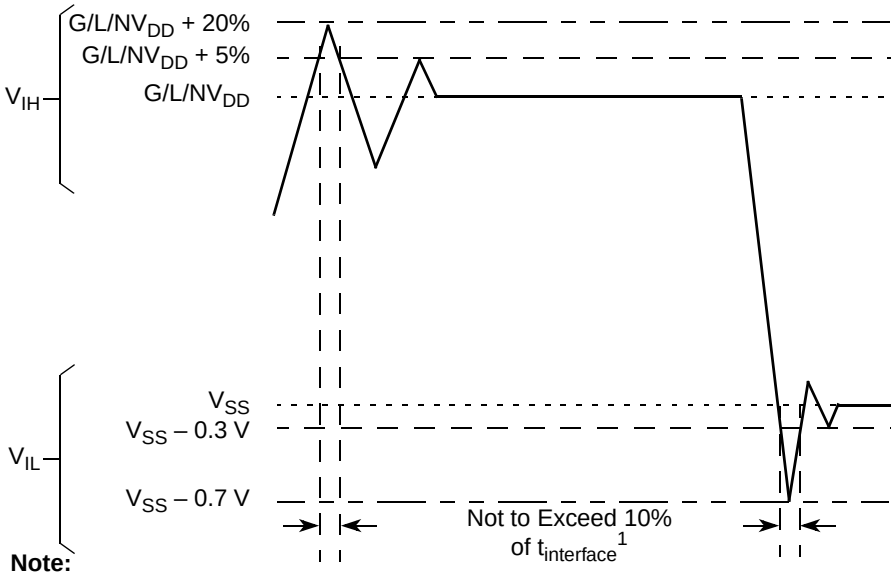
**Table 2. Recommended Operating Conditions (continued)**

| Characteristic | Symbol | Recommended Value[1] | Unit | Current Requirement |
|---|---|---|---|---|

**Note:**

1. $GV_{DD}$, $NV_{DD}$, $AV_{DD}$, and $V_{DD}$ must track each other and must vary in the same direction—either in the positive or negative direction.
2. Some GPIO pins may operate from a 2.5-V supply when configured for other functions.
3. Min temperature is specified with $T_A$; Max temperature is specified with $T_J$.
4. All Power rails must be connected and power applied to the MPC8313 even if the IP interfaces are not used.
5. All I/O pins should be interfaced with peripherals operating at same voltage level.
6. This voltage is the input to the filter discussed in Section 22.2, "PLL Power Supply Filtering" and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter.

This figure shows the undershoot and overshoot voltages at the interfaces of the MPC8313E.




**Note:**

1. Note that $t_{interface}$ refers to the clock period associated with the bus clock interface.

**Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}$/$NV_{DD}$/$LV_{DD}$**

## 2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths.

**Table 3. Output Drive Capability**

| Driver Type | Output Impedance (Ω) | Supply Voltage |
|---|---|---|
| Local bus interface utilities signals | 42 | $NV_{DD}$ = 3.3 V |
| PCI signals | 25 | |
| DDR signal | 18 | $GV_{DD}$ = 2.5 V |

## 5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications.

**Table 10. RESET Initialization Timing Specifications**

| Parameter/Condition | Min | Max | Unit | Note |
|---|---|---|---|---|
| Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow | 32 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Required assertion time of $\overline{\text{PORESET}}$ with stable clock and power applied to SYS_CLK_IN when the device is in PCI host mode | 32 | — | $t_{SYS\_CLK\_IN}$ | 2 |
| Required assertion time of $\overline{\text{PORESET}}$ with stable clock and power applied to PCI_SYNC_IN when the device is in PCI agent mode | 32 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| $\overline{\text{HRESET}}$ assertion (output) | 512 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3] and $\overline{\text{CFG\_CLK\_IN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode | 4 | — | $t_{SYS\_CLK\_IN}$ | 2 |
| Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode | 4 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$ | 0 | — | ns | — |
| Time for the device to turn off POR configuration signal drivers with respect to the assertion of $\overline{\text{HRESET}}$ | — | 4 | ns | 3 |
| Time for the device to turn on POR configuration signal drivers with respect to the negation of $\overline{\text{HRESET}}$ | 1 | — | $t_{PCI\_SYNC\_IN}$ | 1, 3 |

**Notes:**
1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the SYS_CLK_IN input, and PCI_SYNC_IN period depends on the value of $\overline{\text{CFG\_CLKIN\_DIV}}$.
2. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. It is only valid when the device is in PCI host mode.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$.

This table provides the PLL lock times.

**Table 11. PLL Lock Times**

| Parameter/Condition | Min | Max | Unit | Note |
|---|---|---|---|---|
| PLL lock times | — | 100 | μs | — |

# 6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface. Note that DDR SDRAM is $GV_{DD}$(typ) = 2.5 V and DDR2 SDRAM is $GV_{DD}$(typ) = 1.8 V.

**Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Silicon Rev 2.x or Later**

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| MCK[*n*] cycle time, MCK[*n*]/$\overline{\text{MCK}}$[*n*] crossing | $t_{MCK}$ | 6 | 10 | ns | 2 |
| ADDR/CMD output setup with respect to MCK<br>333 MHz<br>266 MHz | $t_{DDKHAS}$ | <br>2.1<br>2.5 | <br>—<br>— | ns | 3 |
| ADDR/CMD output hold with respect to MCK<br>333 MHz<br>266 MHz | $t_{DDKHAX}$ | <br>2.0<br>2.7 | <br>—<br>— | ns | 3 |
| $\overline{\text{MCS}}$[*n*] output setup with respect to MCK<br>333 MHz<br>266 MHz | $t_{DDKHCS}$ | <br>2.1<br>3.15 | <br>—<br>— | ns | 3 |
| $\overline{\text{MCS}}$[*n*] output hold with respect to MCK<br>333 MHz<br>266 MHz | $t_{DDKHCX}$ | <br>2.0<br>2.7 | <br>—<br>— | ns | 3 |
| MCK to MDQS Skew | $t_{DDKHMH}$ | –0.6 | 0.6 | ns | 4 |
| MDQ//MDM output setup with respect to MDQS<br>333 MHz<br>266 MHz | $t_{DDKHDS}$,<br>$t_{DDKLDS}$ | <br>800<br>900 | <br>—<br>— | ps | 5 |
| MDQ//MDM output hold with respect to MDQS<br>333 MHz<br>266 MHz | $t_{DDKHDX}$,<br>$t_{DDKLDX}$ | <br>750<br>1000 | <br>—<br>— | ps | 5 |
| MDQS preamble start | $t_{DDKHMP}$ | $-0.5 \times t_{MCK} - 0.6$ | $-0.5 \times t_{MCK} + 0.6$ | ns | 6 |
| MDQS epilogue end | $t_{DDKHME}$ | –0.6 | 0.6 | ns | 6 |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that $t_{DDKHMH}$ follows the symbol conventions described in note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that $t_{DDKHMP}$ follows the symbol conventions described in note 1.

**Table 37. MII Management DC Electrical Characteristics When Powered at 3.3 V (continued)**

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $NV_{IN}$ symbol referenced in Table 1 and Table 2.

## 8.5.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

**Table 38. MII Management AC Timing Specifications**

At recommended operating conditions with $NV_{DD}$ is 3.3 V ± 0.3V

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| MDC frequency | $f_{MDC}$ | — | 2.5 | — | MHz | 2 |
| MDC period | $t_{MDC}$ | — | 400 | — | ns | |
| MDC clock pulse width high | $t_{MDCH}$ | 32 | — | — | ns | |
| MDC to MDIO delay | $t_{MDKHDX}$ | 10 | — | 170 | ns | |
| MDIO to MDC setup time | $t_{MDDVKH}$ | 5 | — | — | ns | |
| MDIO to MDC hold time | $t_{MDDXKH}$ | 0 | — | — | ns | |
| MDC rise time | $t_{MDCR}$ | — | — | 10 | ns | |
| MDC fall time | $t_{MDHF}$ | — | — | 10 | ns | |

**Notes:**
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)

This figure shows the MII management AC timing diagram.

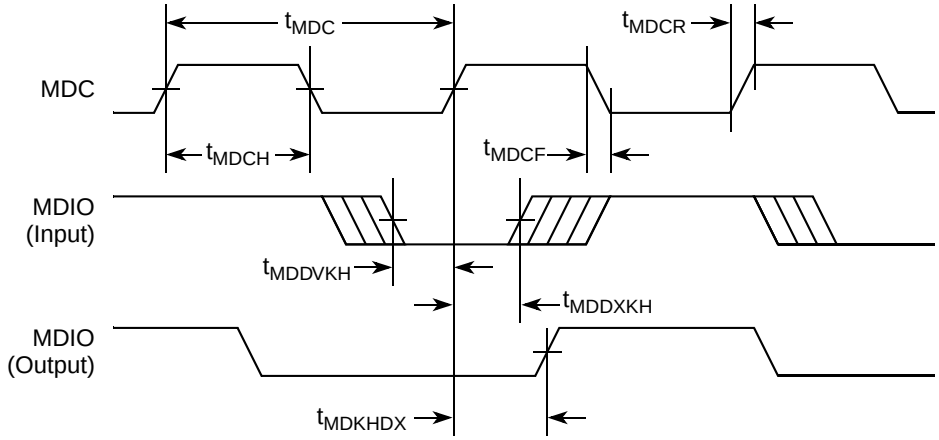



**Figure 21. MII Management Interface Timing Diagram**

— The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 23. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to $\text{XCOREV}_{SS}$ followed by on-chip AC coupling.

— The external reference clock driver must be able to drive this termination.

— The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range:
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above $\text{XCOREV}_{SS}$. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  — If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 Ω to $\text{XCOREV}_{SS}$ DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement. This requirement is described in detail in the following sections.

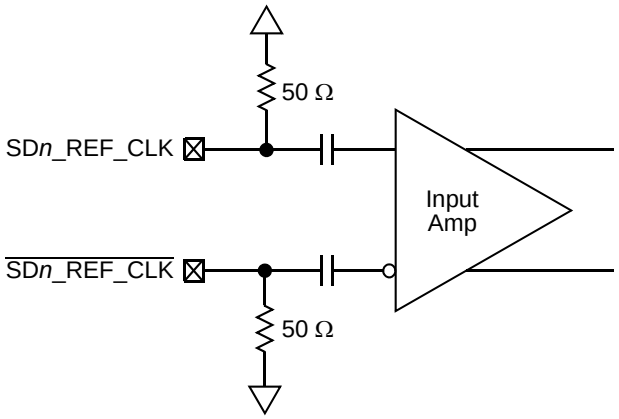



**Figure 23. Receiver of SerDes Reference Clocks**

## 9.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8313E SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- Differential mode
  — The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-to-peak (or between 200 and 800 mV differential peak). In other words, each signal wire

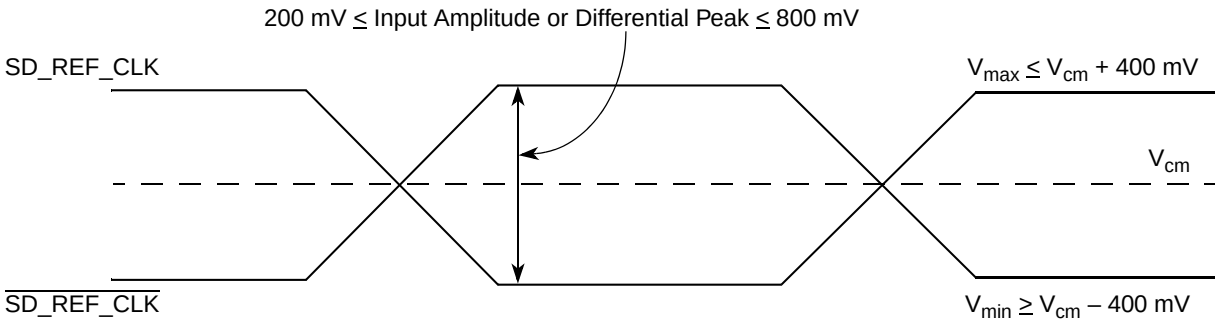



**Figure 25. Differential Reference Clock Input DC Requirements (External AC-Coupled)**

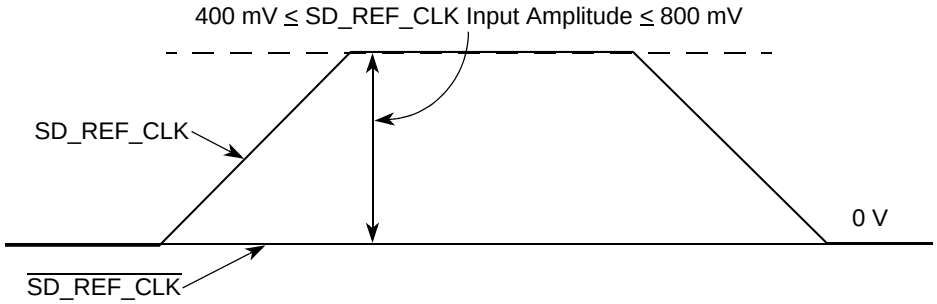



**Figure 26. Single-Ended Reference Clock Input DC Requirements**

### 9.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to $XCOREV_{SS}$, the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce a signal with too large of an amplitude and may need to be DC-biased at the clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC coupling.

**NOTE**

Figure 27 through Figure 30 are for conceptual reference only. Due to the fact that the clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is possible that the clock circuit reference designs provided by clock driver chip vendors are different from what is shown in the figures. They might also vary from one vendor to the other. Therefore, Freescale can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. It is recommended that the system designer contact the selected clock driver chip vendor for the optimal reference circuits for the MPC8313E SerDes reference clock receiver requirement provided in this document.

### 9.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low-phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters for SGMII protocol.

**Table 39. SerDes Reference Clock Common AC Parameters**

At recommended operating conditions with $XV_{DD\_SRDS1}$ or $XV_{DD\_SRDS2}$ = 1.0 V ± 5%.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Rising edge rate | Rise edge rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Falling edge rate | Fall edge rate | 1.0 | 4.0 | V/ns | 2, 3 |
| Differential input high voltage | $V_{IH}$ | +200 | — | mV | 2 |
| Differential input low voltage | $V_{IL}$ | — | –200 | mV | 2 |
| Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn\_REF\_CLK}}$) matching | Rise-fall matching | — | 20 | % | 1, 4 |

**Notes:**
1. Measurement taken from single-ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 31.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point, where SD*n*_REF_CLK rising meets $\overline{\text{SD}n\text{\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK should be compared to the fall edge rate of $\overline{\text{SD}n\text{\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 32.

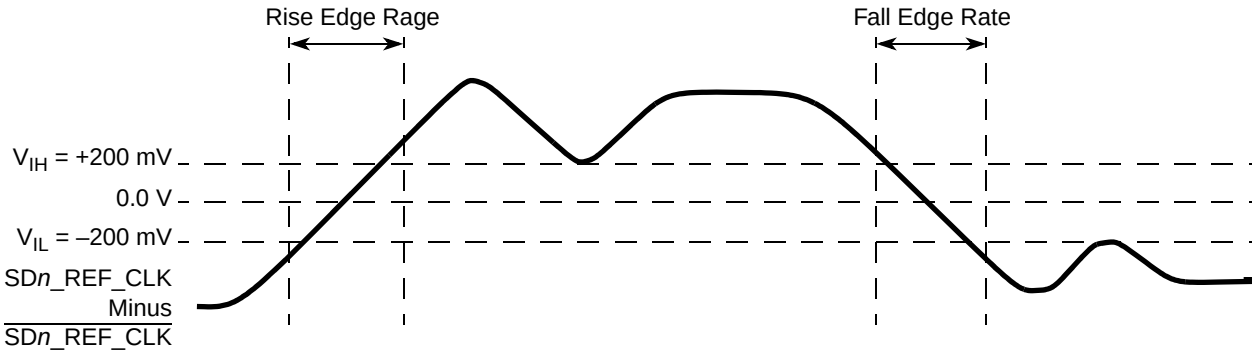



**Figure 31. Differential Measurement Points for Rise and Fall Time**

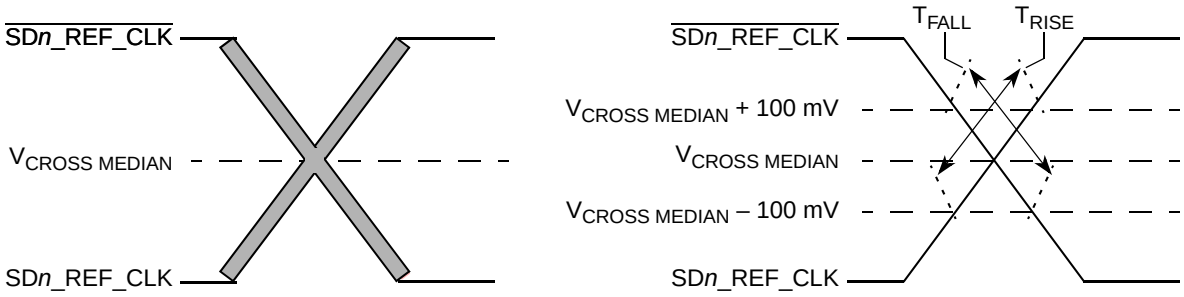



**Figure 32. Single-Ended Measurement Points for Rise and Fall Time Matching**

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. Refer to the following section for detailed information:

- Section 8.3.2, "AC Requirements for SGMII SD_REF_CLK and SD_REF_CLK"

#### 9.2.4.1 Spread Spectrum Clock

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

## 9.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for the SerDes data lane's transmitter and receiver.

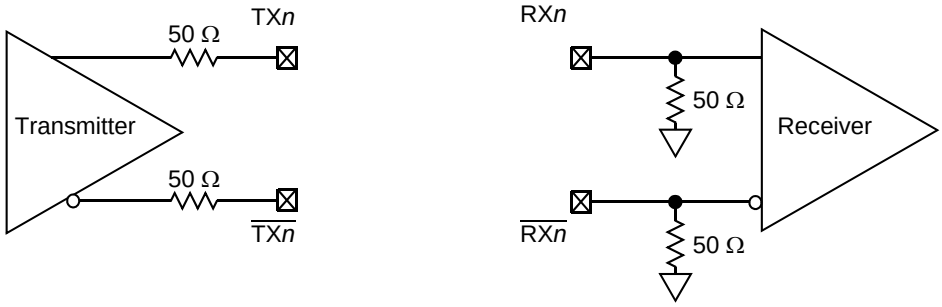



**Figure 33. SerDes Transmitter and Receiver Reference Circuits**

The SerDes data lane's DC and AC specifications are defined in the interface protocol section listed below (SGMII) based on the application usage:

- Section 8.3, "SGMII Interface Electrical Characteristics"

Please note that a external AC-coupling capacitor is required for the above serial transmission protocol with the capacitor value defined in the specifications of the protocol section.

# 11 Enhanced Local Bus

This section describes the DC and AC electrical specifications for the local bus interface.

## 11.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface.

**Table 44. Local Bus DC Electrical Characteristics at 3.3 V**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage for Rev 1.0 | $V_{IH}$ | 2.0 | $LV_{DD}$ + 0.3 | V |
| High-level input voltage for Rev 2.x or later | $V_{IH}$ | 2.1 | $LV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current, ($V_{IN}$[1] = 0 V or $V_{IN}$ = $LV_{DD}$) | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage, ($LV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | $LV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, ($LV_{DD}$ = min, $I_{OH}$ = 2 mA) | $V_{OL}$ | — | 0.2 | V |

**Note:** The parameters stated in above table are valid for all revisions unless explicitly mentioned.

## 11.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface.

**Table 45. Local Bus General Timing Parameters**

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 15 | — | ns | 2 |
| Input setup to local bus clock | $t_{LBIVKH}$ | 7 | — | ns | 3, 4 |
| Input hold from local bus clock | $t_{LBIXKH}$ | 1.0 | — | ns | 3, 4 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT1}$ | 1.5 | — | ns | 5 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT2}$ | 3 | — | ns | 6 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT3}$ | 2.5 | — | ns | 7 |
| LALE output rise to LCLK negative edge | $t_{LALEHOV}$ | — | 3.0 | ns | |
| LALE output fall to LCLK negative edge | $t_{LALETOT1}$ | –1.5 | — | ns | 5 |
| LALE output fall to LCLK negative edge | $t_{LALETOT2}$ | –5.0 | — | ns | 6 |
| LALE output fall to LCLK negative edge | $t_{LALETOT3}$ | –4.5 | — | ns | 7 |
| Local bus clock to output valid | $t_{LBKHOV}$ | — | 3 | ns | 3 |
| Local bus clock to output high impedance for LAD | $t_{LBKHOZ}$ | — | 4 | ns | 8 |

Figure 37 through Figure 40 show the local bus signals.

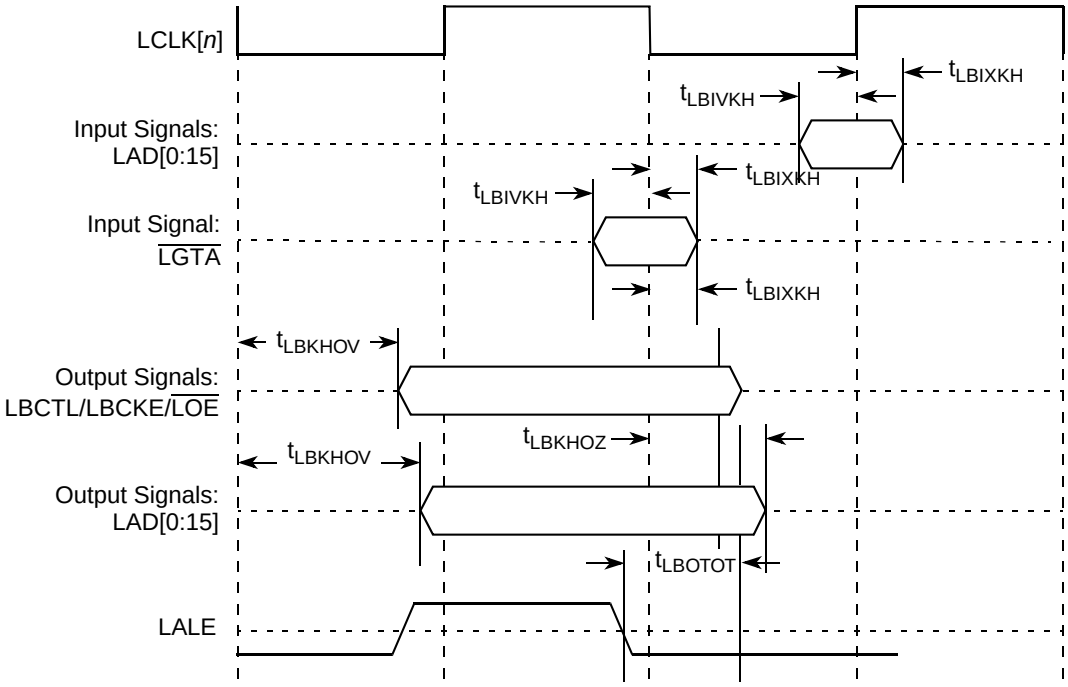



**Figure 37. Local Bus Signals, Non-Special Signals Only**

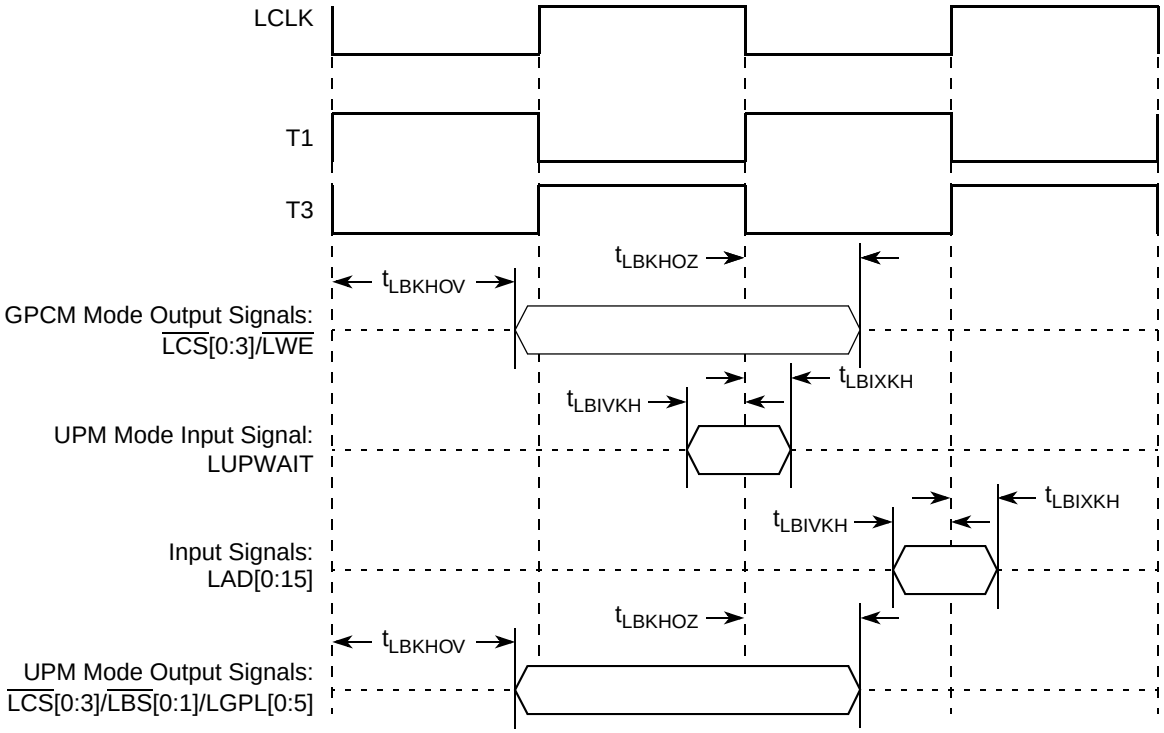



**Figure 38. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2**

This figure shows the AC timing diagram for the $I^2C$ bus.

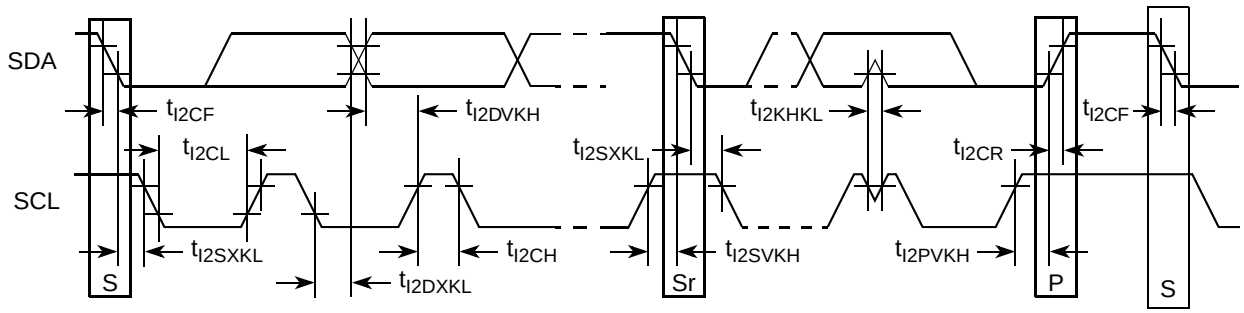



**Figure 47. $I^2C$ Bus AC Timing Diagram**

# 14 PCI

This section describes the DC and AC electrical specifications for the PCI bus.

## 14.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface.

**Table 50. PCI DC Electrical Characteristics[1]**

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | $V_{OUT} \geq V_{OH}$ (min) or | 0.5 × $NV_{DD}$ | $NV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | $V_{OUT} \leq V_{OL}$ (max) | –0.5 | 0.3 × $NV_{DD}$ | V |
| High-level output voltage | $V_{OH}$ | $NV_{DD}$ = min, $I_{OH}$ = –100 µA | 0.9 × $NV_{DD}$ | — | V |
| Low-level output voltage | $V_{OL}$ | $NV_{DD}$ = min, $I_{OL}$ = 100 µA | — | 0.1 × $NV_{DD}$ | V |
| Input current | $I_{IN}$ | 0 V ≤ $V_{IN}$ ≤ $NV_{DD}$ | — | ±5 | µA |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $NV_{IN}$ symbol referenced in Table 1 and Table 2.

## 14.2 PCI AC Electrical Specifications

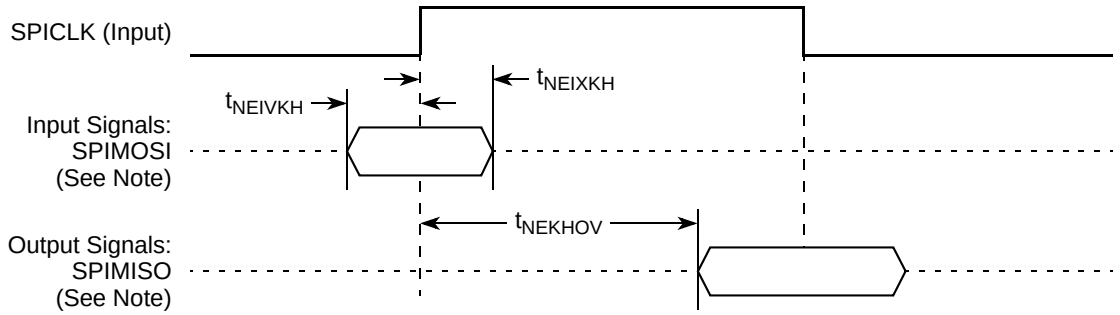
This section describes the general AC timing parameters of the PCI bus. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8313E is configured as a host or agent device.

This table shows the PCI AC timing specifications at 66 MHz.

**Table 51. PCI AC Timing Specifications at 66 MHz**

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Clock to output valid | $t_{PCKHOV}$ | — | 6.0 | ns | 2 |
| Output hold from clock | $t_{PCKHOX}$ | 1 | — | ns | 2 |

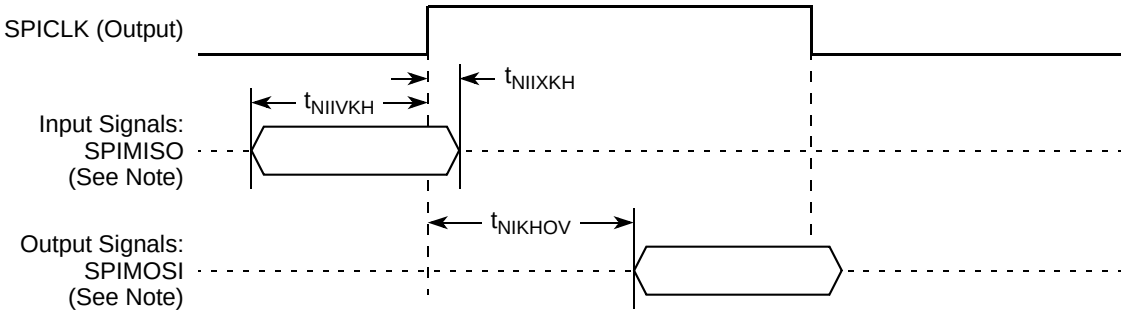
This figure shows the SPI timing in slave mode (external clock).




**Note:** The clock edge is selectable on SPI.

**Figure 54. SPI AC Timing in Slave Mode (External Clock) Diagram**

This figure shows the SPI timing in master mode (internal clock).




**Note:** The clock edge is selectable on SPI.

**Figure 55. SPI AC Timing in Master Mode (Internal Clock) Diagram**

# 19 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8313E is available in a thermally enhanced plastic ball grid array (TEPBGAII), see Section 19.1, "Package Parameters for the MPC8313E TEPBGAII," and Section 19.2, "Mechanical Dimensions of the MPC8313E TEPBGAII," for information on the TEPBGAII.

## 19.1 Package Parameters for the MPC8313E TEPBGAII

The package parameters are as provided in the following list. The package type is 27 mm × 27 mm, 516 TEPBGAII.

| | |
|---|---|
| Package outline | 27 mm × 27 mm |
| Interconnects | 516 |
| Pitch | 1.00 mm |
| Module height (typical) | 2.25 mm |
| Solder Balls | 96.5 Sn/3.5 Ag(VR package) ,<br>62 Sn/36 Pb/2 Ag (ZQ package) Ball diameter (typical) |
| 0.6 mm | |

**Table 62. MPC8313E TEPBGAII Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| TMS | E4 | I | $NV_{DD}$ | 4 |
| $\overline{\text{TRST}}$ | E5 | I | $NV_{DD}$ | 4 |
| **TEST** | | | | |
| TEST_MODE | F4 | I | $NV_{DD}$ | 6 |
| **DEBUG** | | | | |
| $\overline{\text{QUIESCE}}$ | F5 | O | $NV_{DD}$ | — |
| **System Control** | | | | |
| $\overline{\text{HRESET}}$ | F2 | I/O | $NV_{DD}$ | 1 |
| $\overline{\text{PORESET}}$ | F3 | I | $NV_{DD}$ | — |
| $\overline{\text{SRESET}}$ | F1 | I | $NV_{DD}$ | — |
| **Clocks** | | | | |
| SYS_CR_CLK_IN | U26 | I | $NV_{DD}$ | — |
| SYS_CR_CLK_OUT | U25 | O | $NV_{DD}$ | — |
| SYS_CLK_IN | U23 | I | $NV_{DD}$ | — |
| USB_CR_CLK_IN | T26 | I | $NV_{DD}$ | — |
| USB_CR_CLK_OUT | R26 | O | $NV_{DD}$ | — |
| USB_CLK_IN | T22 | I | $NV_{DD}$ | — |
| PCI_SYNC_OUT | U24 | O | $NV_{DD}$ | 3 |
| RTC_PIT_CLOCK | R22 | I | $NV_{DD}$ | — |
| PCI_SYNC_IN | T24 | I | $NV_{DD}$ | — |
| **MISC** | | | | |
| THERM0 | N1 | I | $NV_{DD}$ | 7 |
| THERM1 | N3 | I | $NV_{DD}$ | 7 |
| **PCI** | | | | |
| $\overline{\text{PCI\_INTA}}$ | AF7 | O | $NV_{DD}$ | — |
| $\overline{\text{PCI\_RESET\_OUT}}$ | AB11 | O | $NV_{DD}$ | — |
| PCI_AD0 | AB20 | I/O | $NV_{DD}$ | — |
| PCI_AD1 | AF23 | I/O | $NV_{DD}$ | — |
| PCI_AD2 | AF22 | I/O | $NV_{DD}$ | — |
| PCI_AD3 | AB19 | I/O | $NV_{DD}$ | — |
| PCI_AD4 | AE22 | I/O | $NV_{DD}$ | — |
| PCI_AD5 | AF21 | I/O | $NV_{DD}$ | — |

**Table 62. MPC8313E TEPBGAII Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| PCI_AD6 | AD19 | I/O | $NV_{DD}$ | — |
| PCI_AD7 | AD20 | I/O | $NV_{DD}$ | — |
| PCI_AD8 | AC18 | I/O | $NV_{DD}$ | — |
| PCI_AD9 | AD18 | I/O | $NV_{DD}$ | — |
| PCI_AD10 | AB18 | I/O | $NV_{DD}$ | — |
| PCI_AD11 | AE19 | I/O | $NV_{DD}$ | — |
| PCI_AD12 | AB17 | I/O | $NV_{DD}$ | — |
| PCI_AD13 | AE18 | I/O | $NV_{DD}$ | — |
| PCI_AD14 | AD17 | I/O | $NV_{DD}$ | — |
| PCI_AD15 | AF19 | I/O | $NV_{DD}$ | — |
| PCI_AD16 | AB14 | I/O | $NV_{DD}$ | — |
| PCI_AD17 | AF15 | I/O | $NV_{DD}$ | — |
| PCI_AD18 | AD14 | I/O | $NV_{DD}$ | — |
| PCI_AD19 | AE14 | I/O | $NV_{DD}$ | — |
| PCI_AD20 | AF12 | I/O | $NV_{DD}$ | — |
| PCI_AD21 | AE11 | I/O | $NV_{DD}$ | — |
| PCI_AD22 | AD12 | I/O | $NV_{DD}$ | — |
| PCI_AD23 | AB13 | I/O | $NV_{DD}$ | — |
| PCI_AD24 | AF9 | I/O | $NV_{DD}$ | — |
| PCI_AD25 | AD11 | I/O | $NV_{DD}$ | — |
| PCI_AD26 | AE10 | I/O | $NV_{DD}$ | — |
| PCI_AD27 | AB12 | I/O | $NV_{DD}$ | — |
| PCI_AD28 | AD10 | I/O | $NV_{DD}$ | — |
| PCI_AD29 | AC10 | I/O | $NV_{DD}$ | — |
| PCI_AD30 | AF10 | I/O | $NV_{DD}$ | — |
| PCI_AD31 | AF8 | I/O | $NV_{DD}$ | — |
| PCI_C/$\overline{BE0}$ | AC19 | I/O | $NV_{DD}$ | — |
| PCI_C/$\overline{BE1}$ | AB15 | I/O | $NV_{DD}$ | — |
| PCI_C/$\overline{BE2}$ | AF14 | I/O | $NV_{DD}$ | — |
| PCI_C/$\overline{BE3}$ | AF11 | I/O | $NV_{DD}$ | — |
| PCI_PAR | AD16 | I/O | $NV_{DD}$ | — |
| $\overline{PCI\_FRAME}$ | AF16 | I/O | $NV_{DD}$ | 5 |

## 20.3 Example Clock Frequency Combinations

This table shows several possible frequency combinations that can be selected based on the indicated input reference frequencies, with RCWLR[LBCM] = 0 and RCWLR[DDRCM] =1, such that the LBC operates with a frequency equal to the frequency of *csb_clk* and the DDR controller operates at twice the frequency of *csb_clk*.

**Table 68. System Clock Frequencies**

| | | | | | | LBC(lbc_clk) | | | | e300 Core(core_clk) | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SYS_ CLK_IN/ PCI_CLK | SPMF[1] | VCOD[2] | VCO[3] | CSB (*csb_clk*)[4] | DDR (ddr_clk) | /2 | /4 | /8 | USB ref[5] | × 1 | × 1.5 | × 2 | × 2.5 | × 3 |
| 25.0 | 6 | 2 | 600.0 | 150.0 | 300.0 | — | 37.5 | 18.8 | Note[6] | 150.0 | 225 | 300 | 375 | — |
| 25.0 | 5 | 2 | 500.0 | 125.0 | 250.0 | 62.5 | 31.25 | 15.6 | Note 6 | 125.0 | 188 | 250 | 313 | 375 |
| 33.3 | 5 | 2 | 666.0 | 166.5 | 333.0 | — | 41.63 | 20.8 | Note 6 | 166.5 | 250 | 333 | — | — |
| 33.3 | 4 | 2 | 532.8 | 133.2 | 266.4 | 66.6 | 33.3 | 16.7 | Note 6 | 133.2 | 200 | 266 | 333 | 400 |
| 48.0 | 3 | 2 | 576.0 | 144.0 | 288.0 | — | 36 | 18.0 | 48.0 | 144.0 | 216 | 288 | 360 | — |
| 66.7 | 2 | 2 | 533.4 | 133.3 | 266.7 | 66.7 | 33.34 | 16.7 | Note 6 | 133.3 | 200 | 267 | 333 | 400 |

**Note:**

1. System PLL multiplication factor.
2. System PLL VCO divider.
3. When considering operating frequencies, the valid core VCO operating range of 400–800 MHz must not be violated.
4. Due to erratum eTSEC40, *csb_clk* frequencies of less than 133 MHz do not support gigabit Ethernet data rates. The core frequency must be 333 MHz for gigabit Ethernet operation. This erratum will be fixed in revision 2 silicon.
5. Frequency of USB PLL input reference.
6. USB reference clock must be supplied from a separate source as it must be 24 or 48 MHz, the USB reference must be supplied from a separate external source using USB_CLK_IN.

# 21 Thermal

This section describes the thermal specifications of the MPC8313E.

## 21.1 Thermal Characteristics

This table provides the package thermal characteristics for the 516, 27 × 27 mm TEPBGAII.

**Table 69. Package Thermal Characteristics for TEPBGAII**

| Characteristic | Board Type | Symbol | TEPBGA II | Unit | Note |
|---|---|---|---|---|---|
| Junction-to-ambient natural convection | Single layer board (1s) | $R_{\theta JA}$ | 25 | °C/W | 1, 2 |
| Junction-to-ambient natural convection | Four layer board (2s2p) | $R_{\theta JA}$ | 18 | °C/W | 1, 2, 3 |
| Junction-to-ambient (@200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ | 20 | °C/W | 1, 3 |
| Junction-to-ambient (@200 ft/min) | Four layer board (2s2p) | $R_{\theta JMA}$ | 15 | °C/W | 1, 3 |
| Junction-to-board | — | $R_{\theta JB}$ | 10 | °C/W | 4 |

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$T_J$ = junction temperature (°C)
$T_B$ = board temperature at the package perimeter (°C)
$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51–8
$P_D$ = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

### 21.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$T_J$ = junction temperature (°C)
$T_T$ = thermocouple temperature on top of package (°C)
$\Psi_{JT}$ = thermal characterization parameter (°C/W)
$P_D$ = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

### 21.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to- ambient thermal resistance (°C/W)

# 24 Revision History

This table summarizes a revision history for this document.

**Table 73. Document Revision History**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 4 | 11/2011 | • In Table 2, added following notes:<br>– Note 3: Min temperature is specified with $T_A$; Max temperature is specified with $T_J$<br>– Note 4: All Power rails must be connected and power applied to the MPC8313 even if the IP interfaces are not used.<br>– Note 5: All I/O pins should be interfaced with peripherals operating at same voltage level.<br>– Note 6: This voltage is the input to the filter discussed in Section 22.2, “PLL Power Supply Filtering.” and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter<br>• Decoupled PCI_CLK and SYS_CLK_IN rise and fall times in Table 8. Relaxed maximum rise/fall time of SYS_CLK_IN to 4ns.<br>• Added a note in Table 27 stating “The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm."<br>• In Table 30:<br>– Changed max value of $t_{skrgt}$ in “Data to clock input skew (at receiver)” row from 2.8 to 2.6.<br>– Added Note 7, stating that, “The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm.”<br>• Added a note stating “eTSEC should be interfaced with peripheral operating at same voltage level” in Section 8.1.1, “TSEC DC Electrical Characteristics.”<br>• TSEC1_MDC and TSEC_MDIO are powered at 3.3V by NVDD. Replaced LVDDA/LVDDB with NVDD and removed instances of 2.5V at several places in Section 8.5, “Ethernet Management Interface Electrical Characteristics.”<br>• In Table 43, changed min/max values of $t_{CLK\_TOL}$ from 0.05 to 0.005.<br>• In Table 62:<br>– Added Note 2 for LGPL4 in showing LGPL4 as open-drain.<br>– Removed Note 2 from TSEC1_MDIO.<br>– Added Note 10: This pin has an internal pull-up.<br>– Added Note 11: This pin has an internal pull-down.<br>– Added Note 12: “In MII mode, GTX_CLK should be pulled down by 300 Ω to $V_{SS}$” to TSEC1_GTX_CLK and TSEC2_GTX_CLK.<br>• In Section 19.1, “Package Parameters for the MPC8313E TEPBGAII,” replaced "5.5 Sn/0.5 Cu/4 Ag" with "Sn/3.5 Ag."<br>• Added foot note 3 in Table 65 stating “The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.”<br>• In Table 72:<br>– Added AD = 266 and D = 266.<br>– Added “C = 2.2” in “Revision level” column.<br>– Added Note 4.<br>• Changed resitor from 1.0 Ω to 10 Ω in Figure 58.<br>• Replaced LCCR with LCRR throughout.<br>• Added high-speed to USB Phy description. |
| 3 | 01/2009 | • Table 72, in column aa, changed to AG = 400 MHz. |
| 2.2 | 12/2008 | • Made cross-references active for sections, figures, and tables. |
| 2.1 | 12/2008 | • Added Figure 2, after Table 2 and renumbered the following figures. |