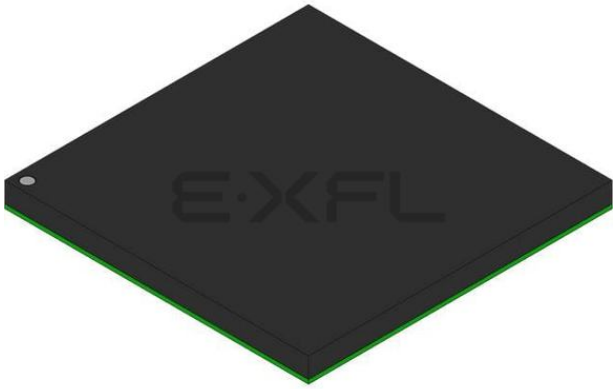

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

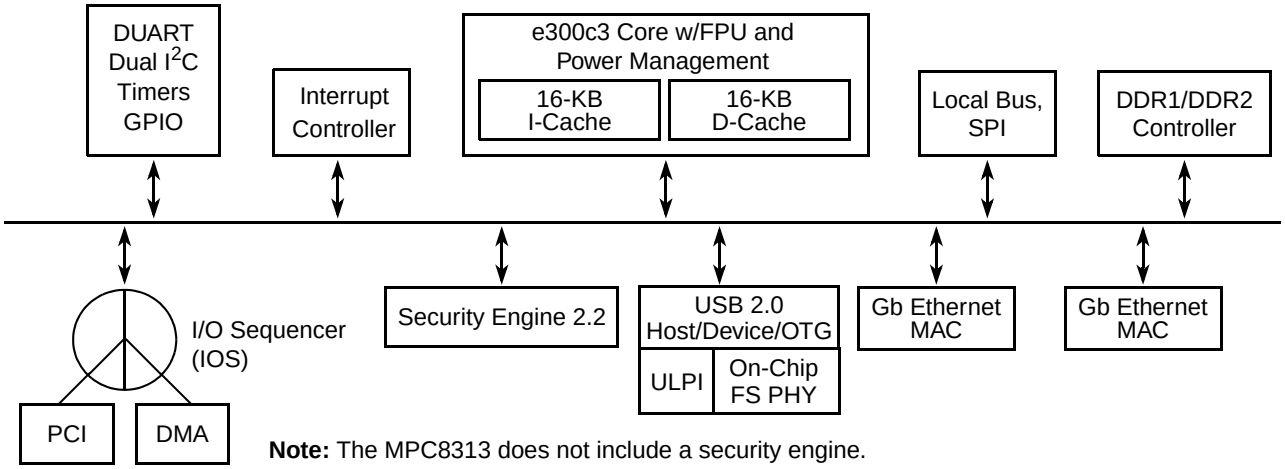
## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300c3 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 333MHz |
| Co-Processors/DSP | Security; SEC 2.2 |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | USB 2.0 + PHY (1) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography |
| Package / Case | 516-BBGA Exposed Pad |
| Supplier Device Package | 516-TEPBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8313evraffb |

# 1 Overview

The MPC8313E incorporates the e300c3 core, which includes 16 Kbytes of L1 instruction and data caches and on-chip memory management units (MMUs). The MPC8313E has interfaces to dual enhanced three-speed 10/100/1000 Mbps Ethernet controllers, a DDR1/DDR2 SDRAM memory controller, an enhanced local bus controller, a 32-bit PCI controller, a dedicated security engine, a USB 2.0 dual-role controller and an on-chip high-speed PHY, a programmable interrupt controller, dual $I^2C$ controllers, a 4-channel DMA controller, and a general-purpose I/O port. This figure shows a block diagram of the MPC8313E.




**Note:** The MPC8313 does not include a security engine.

**Figure 1. MPC8313E Block Diagram**

The MPC8313E security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

## 1.1 MPC8313E Features

The following features are supported in the MPC8313E:

- Embedded PowerPC™ e300 processor core built on Power Architecture™ technology; operates at up to 333 MHz.
- High-performance, low-power, and cost-effective host processor
- DDR1/DDR2 memory controller—one 16-/32-bit interface at up to 333 MHz supporting both DDR1 and DDR2
- 16-Kbyte instruction cache and 16-Kbyte data cache, a floating point unit, and two integer units
- Peripheral interfaces such as 32-bit PCI interface with up to 66-MHz operation, 16-bit enhanced local bus interface with up to 66-MHz operation, and USB 2.0 (high speed) with an on-chip PHY.
- Security engine provides acceleration for control and data plane security protocols
- Power management controller for low-power consumption
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration

**Table 5. MPC8313E Typical I/O Power Dissipation (continued)**

| Interface | Parameter | $GV_{DD}$ (1.8 V) | $GV_{DD}$ (2.5 V) | $NV_{DD}$ (3.3 V) | $LV_{DDA}$/ $LV_{DDB}$ (3.3 V) | $LV_{DDA}$/ $LV_{DDB}$ (2.5 V) | $LV_{DD}$ (3.3 V) | Unit | Comments |
|---|---|---|---|---|---|---|---|---|---|
| USBDR controller load = 20 pF | 60 MHz | — | — | — | 0.078 | — | — | W | — |
| Other I/O | — | — | — | 0.015 | — | — | — | W | — |

This table shows the estimated core power dissipation of the MPC8313E while transitioning into the D3 warm low-power state.

**Table 6. MPC8313E Low-Power Modes Power Dissipation[1]**

| 333-MHz Core, 167-MHz CSB[2] | Rev. 1.0[3] | Rev. 2.x or Later[3] | Unit |
|---|---|---|---|
| D3 warm | 400 | 425 | mW |

**Note:**

1. All interfaces are enabled. For further power savings, disable the clocks to unused blocks.
2. The interfaces are run at the following frequencies: DDR: 333 MHz, eLBC 83 MHz, PCI 33 MHz, eTSEC1 and TSEC2: 167 MHz, SEC: 167 MHz, USB: 167 MHz. See the SCCR register for more information.
3. This is maximum power in D3 Warm based on a voltage of 1.05 V and a junction temperature of 105°C.

# 4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8313E.

## 4.1 DC Electrical Characteristics

This table provides the system clock input (SYS_CLK_IN/PCI_SYNC_IN) DC timing specifications for the MPC8313E.

**Table 7. SYS_CLK_IN DC Electrical Characteristics**

| Parameter | Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | — | $V_{IH}$ | 2.4 | $NV_{DD}$ + 0.3 | V |
| Input low voltage | — | $V_{IL}$ | –0.3 | 0.4 | V |
| SYS_CLK_IN input current | $0 V \le V_{IN} \le NV_{DD}$ | $I_{IN}$ | — | ±10 | μA |
| PCI_SYNC_IN input current | $0 V \le V_{IN} \le 0.5 V$ or $NV_{DD} – 0.5 V \le V_{IN} \le NV_{DD}$ | $I_{IN}$ | — | ±10 | μA |
| PCI_SYNC_IN input current | $0.5 V \le V_{IN} \le NV_{DD} – 0.5 V$ | $I_{IN}$ | — | ±50 | μA |

This table provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}$(typ) = 2.5 V.

**Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface**

At recommended operating conditions with $GV_{DD}$ of 2.5 ± 5%.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| AC input low voltage | $V_{IL}$ | — | $MV_{REF}$ – 0.31 | V | — |
| AC input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.31 | — | V | — |

This table provides the input AC timing specifications for the DDR2 SDRAM interface.

**Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications**

At recommended operating conditions. with $GV_{DD}$ of 2.5 ± 5%.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Controller skew for MDQS—MDQ | $t_{CISKEW}$ | — | — | ps | 1, 2 |
| 333 MHz | — | –750 | 750 | — | — |
| 266 MHz | — | –750 | 750 | — | — |

**Notes:**

1. $t_{CISKEW}$ represents the total amount of skew consumed by the controller between MDQS[*n*] and any corresponding bit that is captured with MDQS[*n*]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called $t_{DISKEW}$. This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of $t_{CISKEW}$.

This figure illustrates the DDR input timing diagram showing the $t_{DISKEW}$ timing parameter.

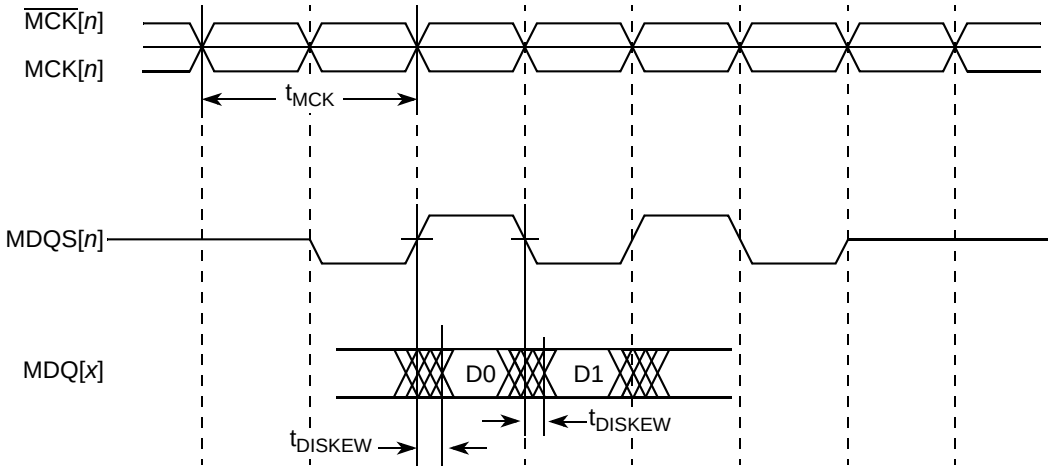



**Figure 4. DDR Input Timing Diagram**

## 8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all the media independent interface (MII), reduced gigabit media independent interface (RGMII), serial gigabit media independent interface (SGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the MII interface can be operated at 3.3 V. The RMII and SGMII interfaces can be operated at either 3.3 or 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for *Gigabit Ethernet Physical Layer Device Specification Version 1.2*a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.5, "Ethernet Management Interface Electrical Characteristics."

### 8.1.1 TSEC DC Electrical Characteristics

All RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

**NOTE**

eTSEC should be interfaced with peripheral operating at same voltage level.

**Table 24. MII DC Electrical Characteristics**

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage 3.3 V | $LV_{DDA}/LV_{DDB}$ | — | | 2.97 | 3.63 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –4.0 mA | $LV_{DDA}$ or $LV_{DDB}$ = Min | 2.40 | $LV_{DDA}$ + 0.3 or $LV_{DDB}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 4.0 mA | $LV_{DDA}$ or $LV_{DDB}$ = Min | $V_{SS}$ | 0.50 | V |
| Input high voltage | $V_{IH}$ | — | — | 2.0 | $LV_{DDA}$ + 0.3 or $LV_{DDB}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | — | –0.3 | 0.90 | V |
| Input high current | $I_{IH}$ | $V_{IN}$[1] = $LV_{DDA}$ or $LV_{DDB}$ | | — | 40 | μA |
| Input low current | $I_{IL}$ | $V_{IN}$[1] = VSS | | –600 | — | μA |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ symbol referenced in Table 1 and Table 2.

**Table 25. RGMII/RTBI DC Electrical Characteristics**

| Parameters | Symbol | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage 2.5 V | $LV_{DDA}/LV_{DDB}$ | — | 2.37 | 2.63 | V |

— The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 23. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to $\text{XCOREV}_{SS}$ followed by on-chip AC coupling.

— The external reference clock driver must be able to drive this termination.

— The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range:
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above $\text{XCOREV}_{SS}$. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  — If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 Ω to $\text{XCOREV}_{SS}$ DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement. This requirement is described in detail in the following sections.

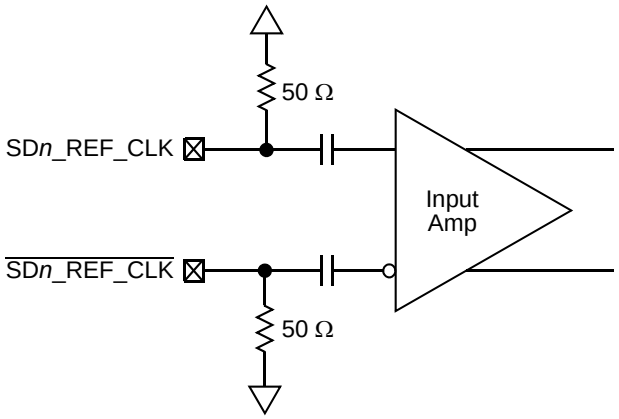



**Figure 23. Receiver of SerDes Reference Clocks**

## 9.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8313E SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- Differential mode
  — The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-to-peak (or between 200 and 800 mV differential peak). In other words, each signal wire

This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8313E SerDes reference clock input's DC requirement.

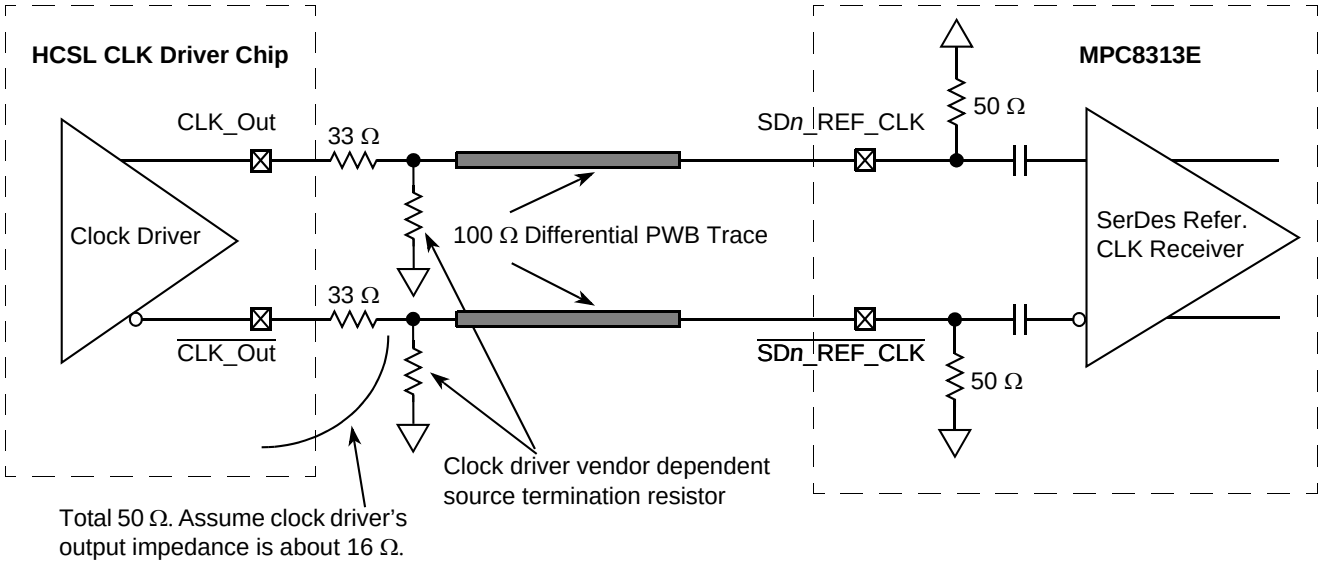



**Figure 27. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)**

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8313E SerDes reference clock input's allowed range (100 to 400 mV), the AC-coupled connection scheme must be used. It assumes the LVDS output driver features a 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

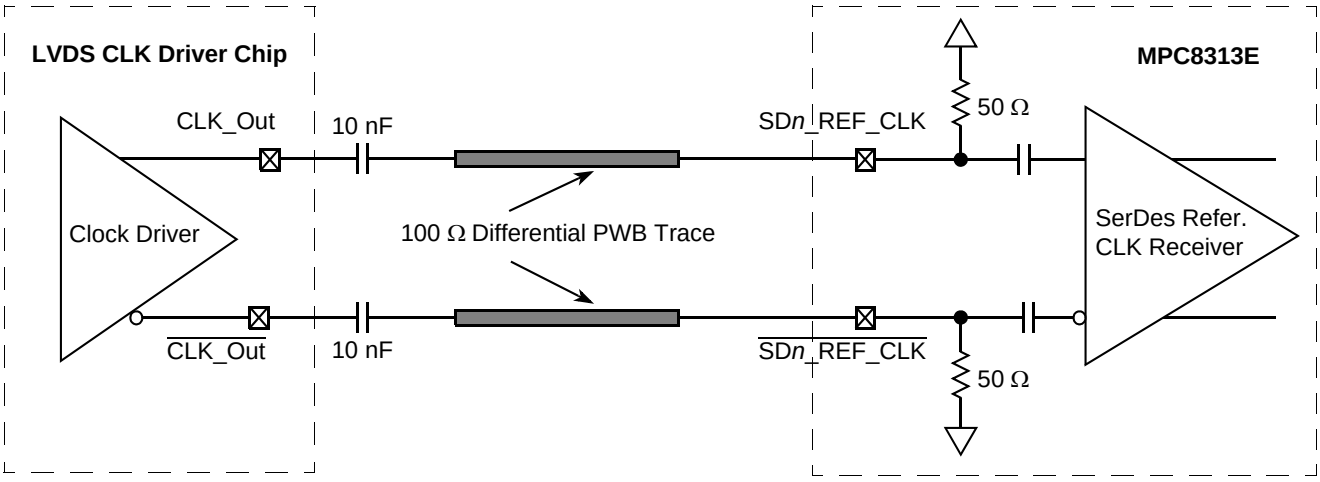



**Figure 28. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)**

This figure shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the MPC8313E SerDes reference clock input's DC requirement, AC coupling has to be used. Figure 29

**Table 49. I²C AC Electrical Specifications (continued)**

All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 48).

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| Data hold time:<br>CBUS compatible masters<br>I²C bus devices | $t_{I2DXKL}$ | <br>—<br>0[2] | <br>—<br>0.9[3] | µs |
| Fall time of both SDA and SCL signals[5] | $t_{I2CF}$ | — | 300 | ns |
| Setup time for STOP condition | $t_{I2PVKH}$ | 0.6 | — | µs |
| Bus free time between a STOP and START condition | $t_{I2KHDX}$ | 1.3 | — | µs |
| Noise margin at the LOW level for each connected device (including hysteresis) | $V_{NL}$ | $0.1 \times NV_{DD}$ | — | V |
| Noise margin at the HIGH level for each connected device (including hysteresis) | $V_{NH}$ | $0.2 \times NV_{DD}$ | — | V |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{I2DVKH}$ symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{I2SXKL}$ symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the $t_{I2C}$ clock reference (K) going to the low (L) state or hold time. Also, $t_{I2PVKH}$ symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the $t_{I2C}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The MPC8313E provides a hold time of at least 300 ns for the SDA signal (referred to the $V_{IHmin}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{I2DVKH}$ has only to be met if the device does not stretch the LOW period ($t_{I2CL}$) of the SCL signal.
4. $C_B$ = capacitance of one bus line in pF.
5. The MPC8313E does not follow the *I²C-BUS Specifications, Version 2.1,* regarding the $t_{I2CF}$ AC parameter.

This figure provides the AC test load for the I²C.

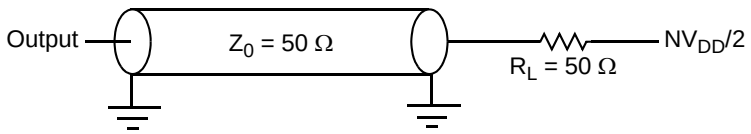



**Figure 46. I²C AC Test Load**

**Table 51. PCI AC Timing Specifications at 66 MHz (continued)**

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Clock to output high impedance | $t_{PCKHOZ}$ | — | 14 | ns | 2, 3 |
| Input setup to clock | $t_{PCIVKH}$ | 3.0 | — | ns | 2, 4 |
| Input hold from clock | $t_{PCIXKH}$ | 0 | — | ns | 2, 4 |

**Notes:**
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{PCIVKH}$ symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, $t_{SYS}$, reference (K) going to the high (H) state or setup time. Also, $t_{PCRHFV}$ symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

This table shows the PCI AC timing specifications at 33 MHz.

**Table 52. PCI AC Timing Specifications at 33 MHz**

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Clock to output valid | $t_{PCKHOV}$ | — | 11 | ns | 2 |
| Output hold from clock | $t_{PCKHOX}$ | 2 | — | ns | 2 |
| Clock to output high impedance | $t_{PCKHOZ}$ | — | 14 | ns | 2, 3 |
| Input setup to clock | $t_{PCIVKH}$ | 3.0 | — | ns | 2, 4 |
| Input hold from clock | $t_{PCIXKH}$ | 0 | — | ns | 2, 4 |

**Notes**:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{PCIVKH}$ symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, $t_{SYS}$, reference (K) going to the high (H) state or setup time. Also, $t_{PCRHFV}$ symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

This figure provides the AC test load for PCI.

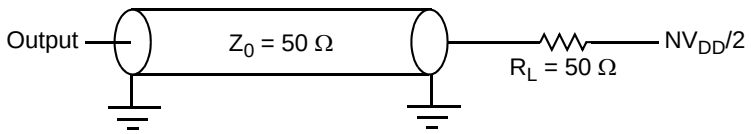



**Figure 48. PCI AC Test Load**

**Table 62. MPC8313E TEPBGAII Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| LA24 | E23 | O | $LV_{DD}$ | 11 |
| LA25 | D22 | O | $LV_{DD}$ | 11 |
| $\overline{\text{LCS0}}$ | D23 | O | $LV_{DD}$ | 10 |
| $\overline{\text{LCS1}}$ | J26 | O | $LV_{DD}$ | 10 |
| $\overline{\text{LCS2}}$ | F22 | O | $LV_{DD}$ | 10 |
| $\overline{\text{LCS3}}$ | D26 | O | $LV_{DD}$ | 10 |
| $\overline{\text{LWE0}}$/$\overline{\text{LFWE}}$ | E24 | O | $LV_{DD}$ | 10 |
| $\overline{\text{LWE1}}$ | H26 | O | $LV_{DD}$ | 10 |
| LBCTL | L22 | O | $LV_{DD}$ | 10 |
| LALE/M1LALE/M2LALE | E26 | O | $LV_{DD}$ | 11 |
| LGPL0/LFCLE | AA23 | O | $LV_{DD}$ | — |
| LGPL1/LFALE | AA24 | O | $LV_{DD}$ | — |
| LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$ | AA25 | O | $LV_{DD}$ | 10 |
| LGPL3/$\overline{\text{LFWP}}$ | AA26 | O | $LV_{DD}$ | — |
| LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/$\overline{\text{LFRB}}$ | Y22 | I/O | $LV_{DD}$ | 2 |
| LGPL5 | E21 | O | $LV_{DD}$ | 10 |
| LCLK0 | H22 | O | $LV_{DD}$ | 11 |
| LCLK1 | G26 | O | $LV_{DD}$ | 11 |
| LA0/GPIO0/MSRCID0 | AC24 | I/O | $LV_{DD}$ | — |
| LA1/GPIO1//MSRCID1 | Y24 | I/O | $LV_{DD}$ | — |
| LA2/GPIO2//MSRCID2 | Y26 | I/O | $LV_{DD}$ | — |
| LA3/GPIO3//MSRCID3 | W22 | I/O | $LV_{DD}$ | — |
| LA4/GPIO4//MSRCID4 | W24 | I/O | $LV_{DD}$ | — |
| LA5/GPIO5/MDVAL | W26 | I/O | $LV_{DD}$ | — |
| LA6/GPIO6 | V22 | I/O | $LV_{DD}$ | — |
| LA7/GPIO7/TSEC_1588_TRIG2 | V23 | I/O | $LV_{DD}$ | 8 |
| LA8/GPIO13/TSEC_1588_ALARM1 | V24 | I/O | $LV_{DD}$ | 8 |
| LA9/GPIO14/TSEC_1588_PP3 | V25 | I/O | $LV_{DD}$ | 8 |
| LA10/TSEC_1588_CLK | V26 | O | $LV_{DD}$ | 8 |
| LA11/TSEC_1588_GCLK | U22 | O | $LV_{DD}$ | 8 |
| LA12/TSEC_1588_PP1 | AD24 | O | $LV_{DD}$ | 8 |
| LA13/TSEC_1588_PP2 | L25 | O | $LV_{DD}$ | 8 |

**Table 62. MPC8313E TEPBGAII Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| TMS | E4 | I | $NV_{DD}$ | 4 |
| $\overline{\text{TRST}}$ | E5 | I | $NV_{DD}$ | 4 |
| **TEST** | | | | |
| TEST_MODE | F4 | I | $NV_{DD}$ | 6 |
| **DEBUG** | | | | |
| $\overline{\text{QUIESCE}}$ | F5 | O | $NV_{DD}$ | — |
| **System Control** | | | | |
| $\overline{\text{HRESET}}$ | F2 | I/O | $NV_{DD}$ | 1 |
| $\overline{\text{PORESET}}$ | F3 | I | $NV_{DD}$ | — |
| $\overline{\text{SRESET}}$ | F1 | I | $NV_{DD}$ | — |
| **Clocks** | | | | |
| SYS_CR_CLK_IN | U26 | I | $NV_{DD}$ | — |
| SYS_CR_CLK_OUT | U25 | O | $NV_{DD}$ | — |
| SYS_CLK_IN | U23 | I | $NV_{DD}$ | — |
| USB_CR_CLK_IN | T26 | I | $NV_{DD}$ | — |
| USB_CR_CLK_OUT | R26 | O | $NV_{DD}$ | — |
| USB_CLK_IN | T22 | I | $NV_{DD}$ | — |
| PCI_SYNC_OUT | U24 | O | $NV_{DD}$ | 3 |
| RTC_PIT_CLOCK | R22 | I | $NV_{DD}$ | — |
| PCI_SYNC_IN | T24 | I | $NV_{DD}$ | — |
| **MISC** | | | | |
| THERM0 | N1 | I | $NV_{DD}$ | 7 |
| THERM1 | N3 | I | $NV_{DD}$ | 7 |
| **PCI** | | | | |
| $\overline{\text{PCI\_INTA}}$ | AF7 | O | $NV_{DD}$ | — |
| $\overline{\text{PCI\_RESET\_OUT}}$ | AB11 | O | $NV_{DD}$ | — |
| PCI_AD0 | AB20 | I/O | $NV_{DD}$ | — |
| PCI_AD1 | AF23 | I/O | $NV_{DD}$ | — |
| PCI_AD2 | AF22 | I/O | $NV_{DD}$ | — |
| PCI_AD3 | AB19 | I/O | $NV_{DD}$ | — |
| PCI_AD4 | AE22 | I/O | $NV_{DD}$ | — |
| PCI_AD5 | AF21 | I/O | $NV_{DD}$ | — |

**Table 62. MPC8313E TEPBGAII Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| PCI_AD6 | AD19 | I/O | $NV_{DD}$ | — |
| PCI_AD7 | AD20 | I/O | $NV_{DD}$ | — |
| PCI_AD8 | AC18 | I/O | $NV_{DD}$ | — |
| PCI_AD9 | AD18 | I/O | $NV_{DD}$ | — |
| PCI_AD10 | AB18 | I/O | $NV_{DD}$ | — |
| PCI_AD11 | AE19 | I/O | $NV_{DD}$ | — |
| PCI_AD12 | AB17 | I/O | $NV_{DD}$ | — |
| PCI_AD13 | AE18 | I/O | $NV_{DD}$ | — |
| PCI_AD14 | AD17 | I/O | $NV_{DD}$ | — |
| PCI_AD15 | AF19 | I/O | $NV_{DD}$ | — |
| PCI_AD16 | AB14 | I/O | $NV_{DD}$ | — |
| PCI_AD17 | AF15 | I/O | $NV_{DD}$ | — |
| PCI_AD18 | AD14 | I/O | $NV_{DD}$ | — |
| PCI_AD19 | AE14 | I/O | $NV_{DD}$ | — |
| PCI_AD20 | AF12 | I/O | $NV_{DD}$ | — |
| PCI_AD21 | AE11 | I/O | $NV_{DD}$ | — |
| PCI_AD22 | AD12 | I/O | $NV_{DD}$ | — |
| PCI_AD23 | AB13 | I/O | $NV_{DD}$ | — |
| PCI_AD24 | AF9 | I/O | $NV_{DD}$ | — |
| PCI_AD25 | AD11 | I/O | $NV_{DD}$ | — |
| PCI_AD26 | AE10 | I/O | $NV_{DD}$ | — |
| PCI_AD27 | AB12 | I/O | $NV_{DD}$ | — |
| PCI_AD28 | AD10 | I/O | $NV_{DD}$ | — |
| PCI_AD29 | AC10 | I/O | $NV_{DD}$ | — |
| PCI_AD30 | AF10 | I/O | $NV_{DD}$ | — |
| PCI_AD31 | AF8 | I/O | $NV_{DD}$ | — |
| PCI_C/$\overline{BE0}$ | AC19 | I/O | $NV_{DD}$ | — |
| PCI_C/$\overline{BE1}$ | AB15 | I/O | $NV_{DD}$ | — |
| PCI_C/$\overline{BE2}$ | AF14 | I/O | $NV_{DD}$ | — |
| PCI_C/$\overline{BE3}$ | AF11 | I/O | $NV_{DD}$ | — |
| PCI_PAR | AD16 | I/O | $NV_{DD}$ | — |
| $\overline{PCI\_FRAME}$ | AF16 | I/O | $NV_{DD}$ | 5 |

**Table 62. MPC8313E TEPBGAII Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| RXB | R1 | I | | — |
| $\overline{\text{RXB}}$ | P1 | I | | — |
| SD_IMP_CAL_RX | V5 | I | | 200 Ω ± 10% to GND |
| $\overline{\text{SD\_REF\_CLK}}$ | T5 | I | | — |
| SD_REF_CLK | T4 | I | | — |
| SD_PLL_TPD | T2 | O | | — |
| SD_IMP_CAL_TX | N5 | I | | 100 Ω ± 10% to GND |
| SDAVDD | R5 | I/O | | — |
| SD_PLL_TPA_ANA | R4 | O | | — |
| SDAVSS | R3 | I/O | | — |
| **USB PHY** | | | | |
| USB_DP | P26 | I/O | | — |
| USB_DM | N26 | I/O | | — |
| USB_VBUS | P24 | I/O | | — |
| USB_TPA | L26 | I/O | | — |
| USB_RBIAS | M24 | I/O | | — |
| USB_PLL_PWR3 | M26 | I/O | | — |
| USB_PLL_GND | N24 | I/O | | — |
| USB_PLL_PWR1 | N25 | I/O | | — |
| USB_VSSA_BIAS | M25 | I/O | | — |
| USB_VDDA_BIAS | M22 | I/O | | — |
| USB_VSSA | N22 | I/O | | — |
| USB_VDDA | P22 | I/O | | — |
| **GTM/USB** | | | | |
| USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2/LSRCID0 | AD23 | I/O | $NV_{DD}$ | — |
| USBDR_PWRFAULT/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$/ LSRCID1 | AE23 | I/O | $NV_{DD}$ | — |
| USBDR_PCTL0/$\overline{\text{GTM1\_TOUT1}}$/LSRCID2 | AC22 | O | $NV_{DD}$ | — |
| USBDR_PCTL1/LBC_PM_REF_10/LSRCID3 | AB21 | O | $NV_{DD}$ | — |

**Table 63. Configurable Clock Units**

| Unit | Default Frequency | Options |
|---|---|---|
| TSEC1 | *csb_clk* | Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3 |
| TSEC2 | *csb_clk* | Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3 |
| Security Core, $I^2C$, SAP, TPR | *csb_clk* | Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3 |
| USB DR | *csb_clk* | Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3 |
| PCI and DMA complex | *csb_clk* | Off, *csb_clk* |

This table provides the operating frequencies for the MPC8313E TEPBGAII under recommended operating conditions (see Table 2).

**Table 64. Operating Frequencies for TEPBGAII**

| Characteristic[1] | Maximum Operating Frequency | Unit |
|---|---|---|
| e300 core frequency (*core_clk*) | 333 | MHz |
| Coherent system bus frequency (*csb_clk*) | 167 | MHz |
| DDR1/2 memory bus frequency (MCK)[2] | 167 | MHz |
| Local bus frequency (LCLK*n*)[3] | 66 | MHz |
| PCI input frequency (SYS_CLK_IN or PCI_CLK) | 66 | MHz |

**Note:**

1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK[0:1], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM] and SCCR[USBDRCM] must be programmed such that the maximum internal operating frequency of the security core and USB modules do not exceed their respective value listed in this table.
2. The DDR data rate is 2x the DDR memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbc_clk* frequency (depending on LCRR[CLKDIV]), which is in turn, 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

## 20.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. This table shows the multiplication factor encodings for the system PLL.

**Table 65. System PLL Multiplication Factors**

| RCWL[SPMF] | System PLL Multiplication Factor |
|---|---|
| 0000 | Reserved |
| 0001 | Reserved |
| 0010 | × 2 |
| 0011 | × 3 |

## 20.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in this table should be considered as reserved.

**NOTE**

Core VCO frequency = core frequency × VCO divider. The VCO divider, which is determined by RCWLR[COREPLL], must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

**Table 67. e300 Core PLL Configuration**

| RCWL[COREPLL] | | | ***core_clk* : *csb_clk* Ratio**[1] | **VCO Divider (VCOD)**[3] |
|---|---|---|---|---|
| **0–1** | **2–5** | **6** | | |
| ***nn*** | **0000** | 0 | PLL bypassed (PLL off, *csb_clk* clocks core directly) | PLL bypassed (PLL off, *csb_clk* clocks core directly) |
| **11** | ***nnnn*** | n | n/a | n/a |
| **00** | **0001** | 0 | 1:1 | 2 |
| **01** | **0001** | 0 | 1:1 | 4 |
| **10** | **0001** | 0 | 1:1 | 8 |
| **00** | **0001** | 1 | 1.5:1 | 2 |
| **01** | **0001** | 1 | 1.5:1 | 4 |
| **10** | **0001** | 1 | 1.5:1 | 8 |
| **00** | **0010** | 0 | 2:1 | 2 |
| **01** | **0010** | 0 | 2:1 | 4 |
| **10** | **0010** | 0 | 2:1 | 8 |
| **00** | **0010** | 1 | 2.5:1 | 2 |
| **01** | **0010** | 1 | 2.5:1 | 4 |
| **10** | **0010** | 1 | 2.5:1 | 8 |
| **00** | **0011** | 0 | 3:1 | 2 |
| **01** | **0011** | 0 | 3:1 | 4 |
| **10** | **0011** | 0 | 3:1 | 8 |

**Note:**

1. For *core_clk:csb_clk* ratios of 2.5:1 and 3:1, the *core_clk* must not exceed its maximum operating frequency of 333 MHz.
2. Core VCO frequency = core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 400–800 MHz.

Heat sink Vendors include the following list:

| | |
|---|---|
| Aavid Thermalloy<br>80 Commercial St.<br>Concord, NH 03301<br>Internet: www.aavidthermalloy.com | 603-224-9988 |
| Alpha Novatech<br>473 Sapena Ct. #12<br>Santa Clara, CA 95054<br>Internet: www.alphanovatech.com | 408-749-7601 |
| International Electronic Research Corporation (IERC)<br>413 North Moss St.<br>Burbank, CA 91502<br>Internet: www.ctscorp.com | 818-842-7277 |
| Millennium Electronics (MEI)<br>Loroco Sites<br>671 East Brokaw Road<br>San Jose, CA 95112<br>Internet: www.mei-thermal.com | 408-436-8770 |
| Tyco Electronics<br>Chip Coolers™<br>P.O. Box 3668<br>Harrisburg, PA 17105<br>Internet: www.chipcoolers.com | 800-522-6752 |
| Wakefield Engineering<br>33 Bridge St.<br>Pelham, NH 03076<br>Internet: www.wakefield.com | 603-635-2800 |

Interface material vendors include the following:

| | |
|---|---|
| Chomerics, Inc.<br>77 Dragon Ct.<br>Woburn, MA 01801<br>Internet: www.chomerics.com | 781-935-4850 |
| Dow-Corning Corporation<br>Corporate Center<br>PO BOX 994<br>Midland, MI 48686-0994<br>Internet: www.dowcorning.com | 800-248-2481 |
| Shin-Etsu MicroSi, Inc.<br>10028 S. 51st St.<br>Phoenix, AZ 85044<br>Internet: www.microsi.com | 888-642-7674 |
| The Bergquist Company<br>18930 West 78th St.<br>Chanhassen, MN 55317<br>Internet: www.bergquistcompany.com | 800-347-4572 |

- Output signals on the SerDes interface are fed from the $XPADV_{DD}$ power plane. Input signals and sensitive transceiver analog circuits are on the $XCOREV_{DD}$ supply.
- Power: $XPADV_{DD}$ consumes less than 300 mW; $XCOREV_{DD}$ + $SDAV_{DD}$ consumes less than 750 mW.

## 22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8313E system, and the MPC8313E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each $V_{DD}$, $NV_{DD}$, $GV_{DD}$, $LV_{DD}$, $LV_{DDA}$, and $LV_{DDB}$ pin of the device. These decoupling capacitors should receive their power from separate $V_{DD}$, $NV_{DD}$, $GV_{DD}$, $LV_{DD}$, $LV_{DDA}$, $LV_{DDB}$, and VSS power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the $V_{DD}$, $NV_{DD}$, $GV_{DD}$, $LV_{DD}$, $LV_{DDA}$, and $LV_{DDB}$ planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100 to 330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

## 22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power ($XCOREV_{DD}$ and $XPADV_{DD}$) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor from each SerDes supply ($XCOREV_{DD}$ and $XPADV_{DD}$) to the board ground plane on each side of the device. This should be done for all SerDes supplies.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum $V_{DD}$, nominal $NV_{DD}$, 105°C.

**Table 71. Impedance Characteristics**

| Impedance | Local Bus, Ethernet, DUART, Control, Configuration, Power Management | PCI Signals (Not Including PCI Output Clocks) | PCI Output Clocks (Including PCI_SYNC_OUT) | DDR DRAM | Symbol | Unit |
|---|---|---|---|---|---|---|
| $R_N$ | 42 Target | 25 Target | 42 Target | 20 Target | $Z_0$ | Ω |
| $R_P$ | 42 Target | 25 Target | 42 Target | 20 Target | $Z_0$ | Ω |
| Differential | NA | NA | NA | NA | $Z_{DIFF}$ | Ω |

**Note:** Nominal supply voltages. See Table 1, $T_J$ = 105 °C.

## 22.7 Configuration Pin Muxing

The MPC8313E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{PORESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

## 22.8 Pull-Up Resistor Requirements

The MPC8313E requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including $I^2C$, and IPIC (integrated programmable interrupt controller).

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 61. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions because most have asynchronous behavior and spurious assertion, which give unpredictable results.

Refer to the *PCI 2.2 Specification*, for all pull-ups required for PCI.

## 22.9 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in IEEE 1149.1, but is provided on any Freescale devices that are built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, systems generally assert $\overline{\text{TRST}}$ during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ is not practical.

**Table 73. Document Revision History (continued)**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 2 | 10/2008 | • Added Note “The information in this document is accurate for revision 1.0, and 2.x and later. See Section 24.1, “Part Numbers Fully Addressed by this Document,” before Section 1, “Overview.”<br>• Added part numbering details for all the silicon revisions in Table 74.<br>• Changed $V_{IH}$ from 2.7 V to 2.4 V in Table 7.<br>• Added a row for $V_{IH}$ level for Rev 2.x or later in Table 45.<br>• Added a column for maximum power dissipation in low power mode for Rev 2.x or later silicon in Table 6.<br>• Added a column for Power Nos for Rev 2.x or later silicon and added a row for 400 MHz in Table 4.<br>• Removed footnote, “These are preliminary estimates.” from Table 4.<br>• Added Table 21 for DDR AC Specs on Rev 2.x or later silicon.<br>• Added Section 9, “High-Speed Serial Interfaces (HSSI).”<br>• Added $\overline{\text{LFWE}}$, LFCLE, LFALE, $\overline{\text{LOE}}$, $\overline{\text{LFRE}}$, $\overline{\text{LFWP}}$, $\overline{\text{LGTA}}$, LUPWAIT, and $\overline{\text{LFRB}}$ in Table 63.<br>• In Table 39, added note 2: “This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)”<br>• Removed mentions of SGMII (SGMII has separate specs) from Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics.”<br>• Corrected Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics,” to state that RGMII/RTBI interfaces only operate at 2.5 V, not 3.3 V.<br>• Added ZQ package to ordering information In Table 74 and Section 19.1, “Package Parameters for the MPC8313E TEPBGAII” (applicable to both silicon rev. 1.0 and 2.1)<br>• Removed footnotes 5 and 6 from Table 1 (left over when the PCI undershoot/overshoot voltages and maximum AC waveforms were removed from Section 2.1.2, “Power Supply Voltage Specification”).<br>• Removed SD_PLL_TPD (T2) and SD_PLL_TPA_ANA (R4) from Table 63.<br>• Added Section 8.3, “SGMII Interface Electrical Characteristics.” Removed Section 8.5.3 SGMII DC Electrical Characteristics.<br>• Removed “HRESET negation to SRESET negation (output)” spec and changed “HRESET/SRESET assertion (output)” spec to “HRESET assertion (output)” in Table 10.<br>• Clarified POR configuration signal specs to “Time for the device to turn off POR configuration signal drivers with respect to the assertion of HRESET” and “Time for the device to turn on POR configuration signal drivers with respect to the negation of HRESET” in Table 10.<br>• Added Section 24.2, “Part Marking,” and Figure 62. |

**Table 73. Document Revision History (continued)**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 1 | 3/2008 | • In Table 63, added LBC_PM_REF_10 & LSRCID3 as muxed with USBDR_PCTL1<br>• In Table 63, added LSRCID2 as muxed with USBDR_PCTL0<br>• In Table 63, added LSRCID1 as muxed with USBDR_PWRFAULT<br>• In Table 63, added LSRCID0 as muxed with USBDR_DRIVE_VBUS<br>• In Table 63, moved T1, U2,& V2 from $V_{DD}$ to XCOREVDD.<br>• In Table 63, moved P2, R2, & T3 from $V_{SS}$ to XCOREVSS.<br>• In Table 63, moved P5, & U4 from $V_{DD}$ to XPADVDD.<br>• In Table 63, moved P3, & V4 from $V_{SS}$ to XPADVSS.<br>• In Table 63, removed “Double with pad” for $AV_{DD1}$ and $AV_{DD2}$ and moved $AV_{DD1}$ and $AV_{DD2}$ to Power and Ground Supplies section<br>• In Table 63, added impedance control requirements for SD_IMP_CAL_TX (100 ohms to GND) and SD_IMP_CAL_RX (200 ohms to GND).<br>• In Table 63, updated muxing in pinout to show new options for selecting IEEE 1588 functionality. Added footnote 8<br>• In Table 63, updated muxing in pinout to show new LBC ECC boot enable control muxed with eTSEC1_MDC<br>• Added pin type information for power supplies.<br>• Removed N1 and N3 from Vss section of Table 63. Added Therm0 and Therm1 (N1 and N3, respectively). Added note 7 to state: “Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.”<br>• In Table 65 corrected maximum frequency of Local Bus Frequency from “33–66” to 66 MHz<br>• In Table 65 corrected maximum frequency of PCI from “24–66” to 66 MHz<br>• Added “which is determined by RCWLR[COREPLL],” to the note in Section 20.2, “Core PLL Configuration” about the VCO divider.<br>• Added “(VCOD)” next to VCO divider column in Table 68. Added footnote stating that core_clk frequency must not exceed its maximum, so 2.5:1 and 3:1 *core_clk:csb_clk* ratios are invalid for certain *csb_clk* values.<br>• In Table 69, notes were confusing. Added note 3 for VCO column, note 4 for CSB (*csb_clk*) column, note 5 for USB ref column, and note 6 to replace “Note 1”. Clarified note 4 to explain erratum eTSEC40.<br>• In Table 69, updated note 6 to specify USB reference clock frequencies limited to 24 and 48 for rev. 2 silicon.<br>• Replaced Table 71 “Thermal Resistance for TEPBGAII with Heat Sink in Open Flow”.<br>• Removed last row of Table 19.<br>• Removed 200 MHz rows from Table 21 and Table 5.<br>• Changed VIH minimum spec from 2.0 to 2.1 for clock, PIC, JTAG, SPI, and reset pins in Table 9, Table 47, Table 54, Table 59, and Table 61.<br>• Added Figure 4 showing the DDR input timing diagram.<br>• In Table 19, removed “MDM” from the “MDQS-MDQ/MECC/MDM” text under the Parameter column for the tCISKEW parameter. MDM is an output signal and should be removed from the input AC timing spec table (tCISKEW).<br>• Added “and power” to rows 2 and 3 in Table 10<br>• Added the sentence “Once both the power supplies...” and PORESET to Section 2.2, “Power Sequencing,” and Figure 3.<br>• In Figure 35, corrected “USB0_CLK/USB1_CLK/DR_CLK” with “USBDR_CLK”<br>• In Table 42, clarified that AC specs are for ULPI only. |
| 0 | 6/2007 | Initial release. |

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