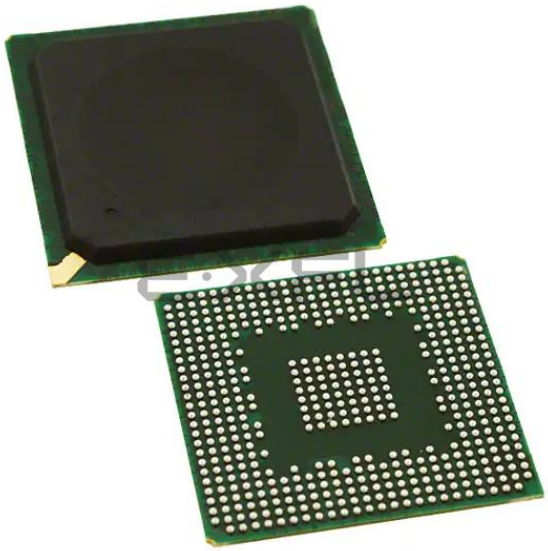

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	267MHz
Co-Processors/DSP	Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8313ezqaddb

1.10 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the MPC8313E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

1.11 DMA Controller, Dual I^2C, DUART, Local Bus Controller, and Timers

The MPC8313E provides an integrated four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Supports misaligned transfers

There are two I^2C controllers. These synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. The 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8313E local bus controller (LBC) port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The three user programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM or UPM controller. The FCM provides a glueless interface to parallel-bus NAND Flash E2PROM devices. The FCM contains three basic configuration register groups—BR*n*, OR*n*, and FMR. Both may exist in the same system. The local bus can operate at up to 66 MHz.

The MPC8313E system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8313E. The MPC8313E is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

4.2 AC Electrical Characteristics

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the system clock input (SYS_CLK_IN/PCI_CLK) AC timing specifications for the MPC8313E.

Table 8. SYS_CLK_IN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYS_CLK_IN/PCI_CLK frequency	$f_{SYS\_CLK\_IN}$	24	—	66.67	MHz	1
SYS_CLK_IN/PCI_CLK cycle time	$t_{SYS\_CLK\_IN}$	15	—	—	ns	—
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	0.6	0.8	4	ns	2
PCI_CLK rise and fall time	t_{PCH}, t_{PCL}	0.6	0.8	1.2	ns	2
SYS_CLK_IN/PCI_CLK duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3
SYS_CLK_IN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system, core, security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN/PCI_CLK are measured at 0.4 and 2.4 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8313E.

5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins.

Table 9. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) when GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	2.3	2.7	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.15	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.15	V	—

This figure provides the AC test load for the DDR bus.

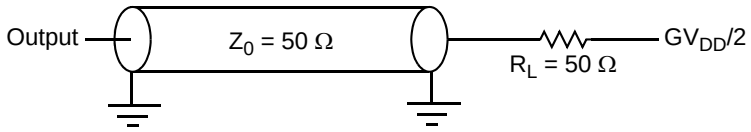


Figure 7. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 22. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.0	NV_{DD} + 0.3	V
Low-level input voltage NV_{DD}	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	NV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current (0 V ≤V_{IN} ≤ NV_{DD})	I_{IN}	—	±5	μA

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all the media independent interface (MII), reduced gigabit media independent interface (RGMII), serial gigabit media independent interface (SGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the MII interface can be operated at 3.3 V. The RMII and SGMII interfaces can be operated at either 3.3 or 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for *Gigabit Ethernet Physical Layer Device Specification Version 1.2*a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.5, "Ethernet Management Interface Electrical Characteristics."

8.1.1 TSEC DC Electrical Characteristics

All RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

NOTE

eTSEC should be interfaced with peripheral operating at same voltage level.

Table 24. MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DDA}/LV_{DDB}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LV_{DDA} or LV_{DDB} = Min	2.40	LV_{DDA} + 0.3 or LV_{DDB} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LV_{DDA} or LV_{DDB} = Min	V_{SS}	0.50	V
Input high voltage	V_{IH}	—	—	2.0	LV_{DDA} + 0.3 or LV_{DDB} + 0.3	V
Input low voltage	V_{IL}	—	—	–0.3	0.90	V
Input high current	I_{IH}	V_{IN}[1] = LV_{DDA} or LV_{DDB}		—	40	μA
Input low current	I_{IL}	V_{IN}[1] = VSS		–600	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 25. RGMII/RTBI DC Electrical Characteristics

Parameters	Symbol	Conditions	Min	Max	Unit
Supply voltage 2.5 V	LV_{DDA}/LV_{DDB}	—	2.37	2.63	V

8.3.2 AC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

This table lists the SGMII SerDes reference clock AC requirements. Note that SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Table 31. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit
t_{REF}	REFCLK cycle time	—	8	—	ns
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps

8.3.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 32 and Table 33 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX[*n*] and $\overline{\text{SD\_TX}}$[*n*]) as depicted in Figure 16.

Table 32. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$XCOREV_{DD}$	0.95	1.0	1.05	V	
Output high voltage	V_{OH}	—	—	$XCOREV_{DD\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-max}}/2$	mV	1
Output low voltage	V_{OL}	$XCOREV_{DD\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-max}}/2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	
Output differential voltage[2, 3]	$\lvert V_{OD}\rvert$	323	500	725	mV	Equalization setting: 1.0x
Output offset voltage	V_{OS}	425	500	575	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	
Mismatch in a pair	ΔR_O	—	—	10	%	
Change in V_{OD} between 0 and 1	$\Delta\lvert V_{OD}\rvert$	—	—	25	mV	
Change in V_{OS} between 0 and 1	ΔV_{OS}	—	—	25	mV	
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	

Notes:

1. This will not align to DC-coupled SGMII. $XCOREV_{DD\text{-}Typ}$ = 1.0 V.
2. $\lvert V_{OD}\rvert = \lvert V_{TXn} - V_{\overline{TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $XCOREV_{DD\text{-}Typ}$ = 1.0 V, no common mode offset variation (V_{OS} = 500 mV), SerDes transmitter is terminated with 100-Ω differential load between TX[*n*] and $\overline{\text{TX}}$[*n*].
4. V_{OS} is also referred to as output common mode voltage.

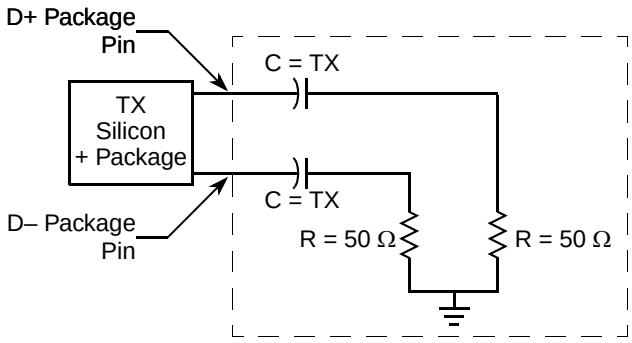
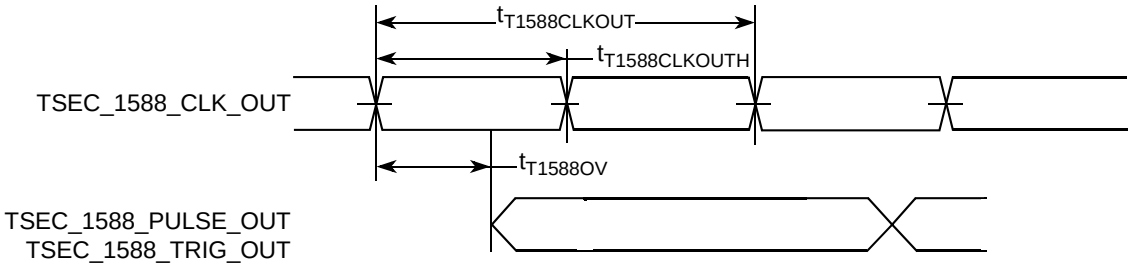


Figure 18. SGMII AC Test/Measurement Load

8.4 eTSEC IEEE 1588 AC Specifications

This figure provides the data and command output timing diagram.



Note: The output delay is count starting rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is count starting falling edge.

Figure 19. eTSEC IEEE 1588 Output AC Timing

This figure provides the data and command input timing diagram.

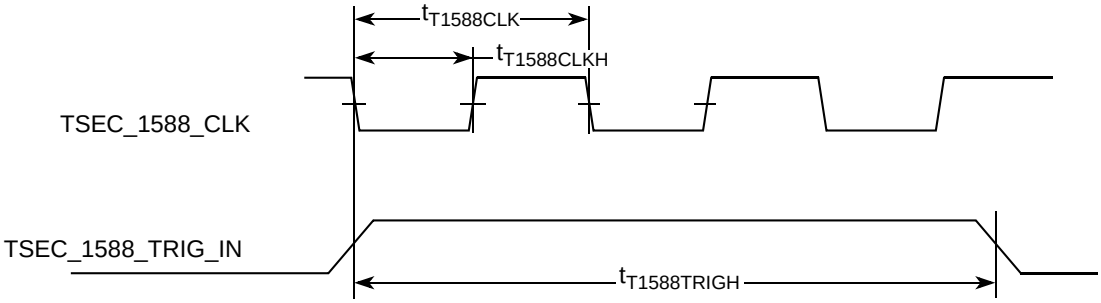


Figure 20. eTSEC IEEE 1588 Input AC Timing

This table lists the IEEE 1588 AC timing specifications.

Table 36. eTSEC IEEE 1588 AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.8	—	$T_{RX\_CLK} \times 9$	ns	1, 3
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	

Table 37. MII Management DC Electrical Characteristics When Powered at 3.3 V (continued)

Note:
1. Note that the symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

8.5.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 38. MII Management AC Timing Specifications

At recommended operating conditions with NV_{DD} is 3.3 V ± 0.3V

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO delay	t_{MDKHDX}	10	—	170	ns	
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	
MDC fall time	t_{MDHF}	—	—	10	ns	

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)

This figure shows the MII management AC timing diagram.

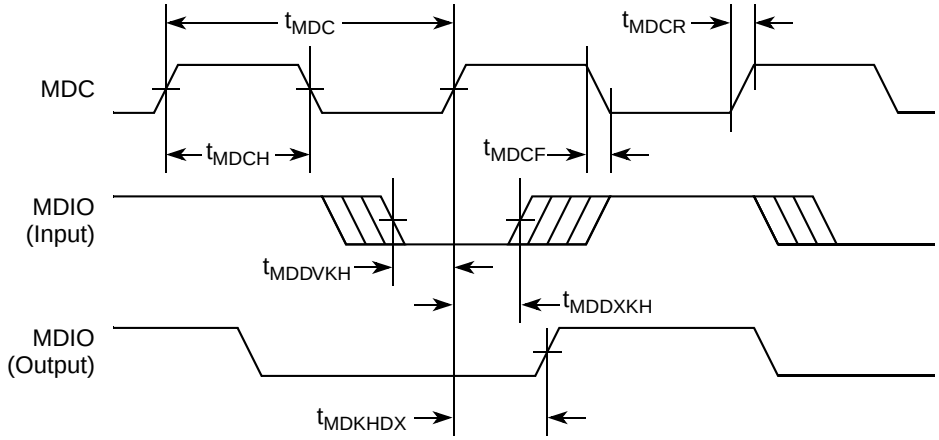


Figure 21. MII Management Interface Timing Diagram

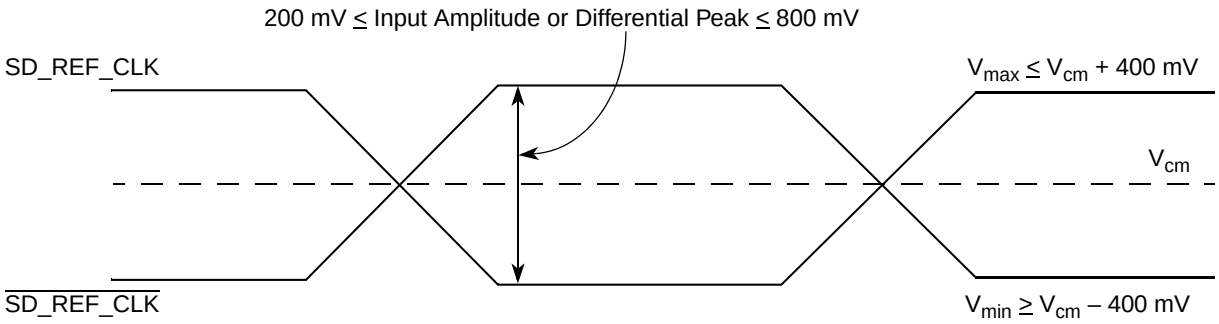


Figure 25. Differential Reference Clock Input DC Requirements (External AC-Coupled)

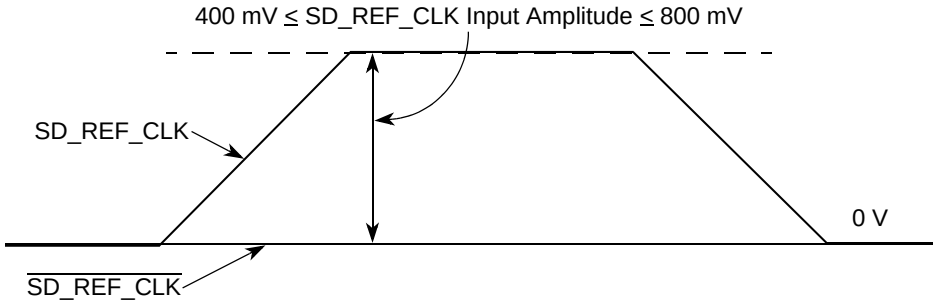


Figure 26. Single-Ended Reference Clock Input DC Requirements

9.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to $XCOREV_{SS}$, the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce a signal with too large of an amplitude and may need to be DC-biased at the clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC coupling.

NOTE

Figure 27 through Figure 30 are for conceptual reference only. Due to the fact that the clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is possible that the clock circuit reference designs provided by clock driver chip vendors are different from what is shown in the figures. They might also vary from one vendor to the other. Therefore, Freescale can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. It is recommended that the system designer contact the selected clock driver chip vendor for the optimal reference circuits for the MPC8313E SerDes reference clock receiver requirement provided in this document.

Figure 37 through Figure 40 show the local bus signals.

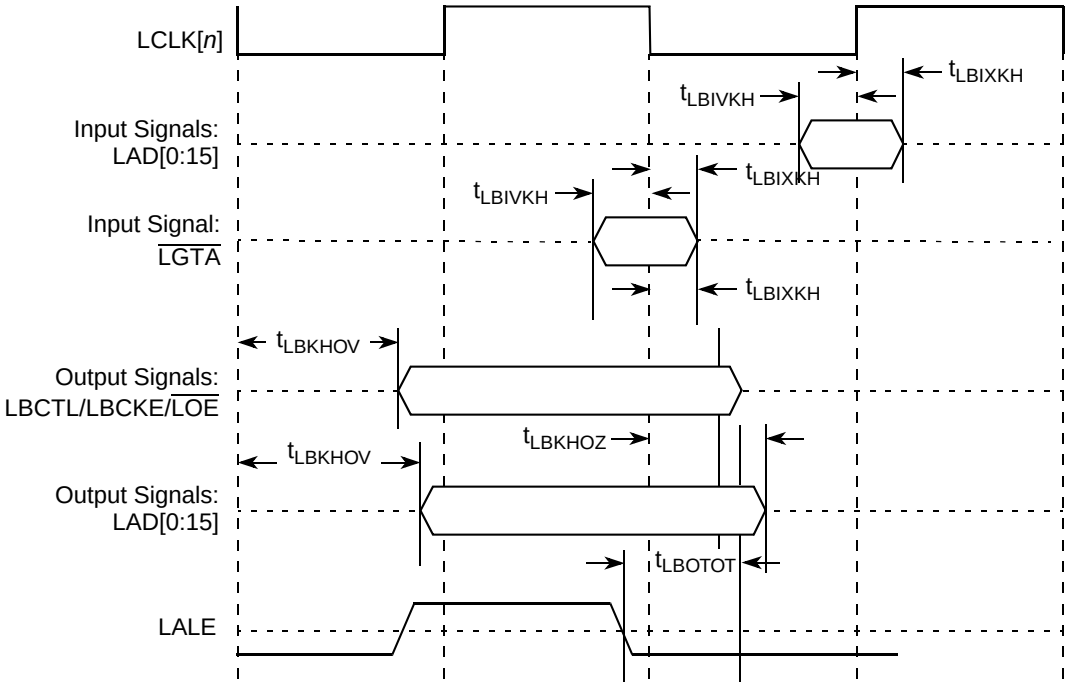


Figure 37. Local Bus Signals, Non-Special Signals Only

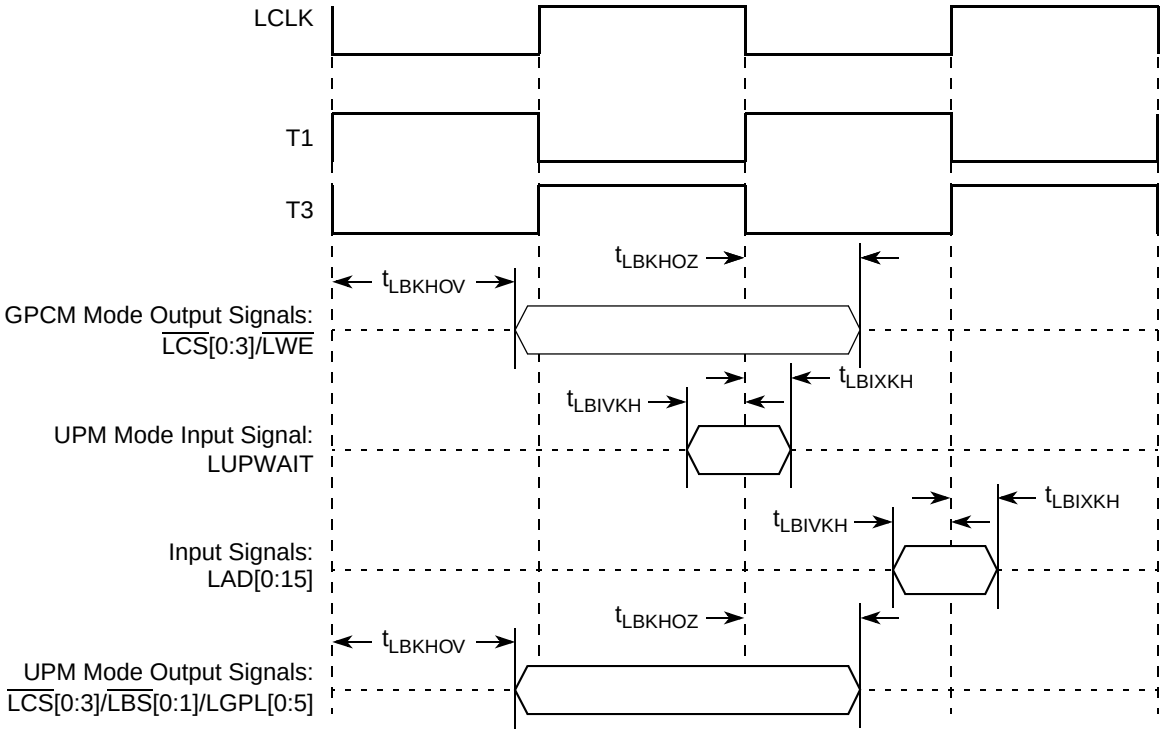


Figure 38. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2

13 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interface.

13.1 I^2C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interface.

Table 48. I^2C DC Electrical Characteristics

At recommended operating conditions with NV_{DD} of 3.3 V ± 0.3 V.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage level	V_{IH}	$0.7 \times NV_{DD}$	$NV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times NV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times NV_{DD}$	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	
Input current, ($0 V \le V_{IN} \le NV_{DD}$)	I_{IN}	—	± 5	μA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if NV_{DD} is switched off.

13.2 I^2C AC Electrical Specifications

This table provides the AC timing parameters for the I^2C interface.

Table 49. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 48).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns

This figure shows the AC timing diagram for the I^2C bus.

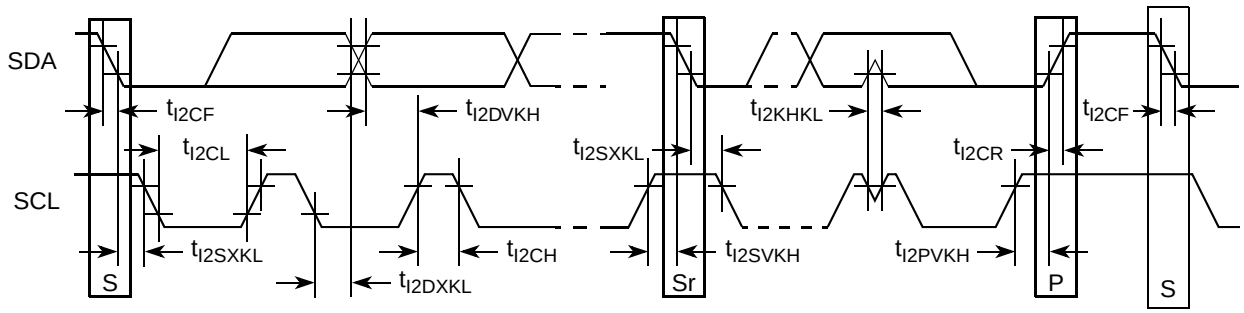


Figure 47. I^2C Bus AC Timing Diagram

14 PCI

This section describes the DC and AC electrical specifications for the PCI bus.

14.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface.

Table 50. PCI DC Electrical Characteristics[1]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	0.5 × NV_{DD}	NV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.5	0.3 × NV_{DD}	V
High-level output voltage	V_{OH}	NV_{DD} = min, I_{OH} = –100 µA	0.9 × NV_{DD}	—	V
Low-level output voltage	V_{OL}	NV_{DD} = min, I_{OL} = 100 µA	—	0.1 × NV_{DD}	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NV_{DD}	—	±5	µA

Note:
1. Note that the symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

14.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8313E is configured as a host or agent device.

This table shows the PCI AC timing specifications at 66 MHz.

Table 51. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TMS	E4	I	NV_{DD}	4
$\overline{\text{TRST}}$	E5	I	NV_{DD}	4
TEST				
TEST_MODE	F4	I	NV_{DD}	6
DEBUG				
$\overline{\text{QUIESCE}}$	F5	O	NV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	F2	I/O	NV_{DD}	1
$\overline{\text{PORESET}}$	F3	I	NV_{DD}	—
$\overline{\text{SRESET}}$	F1	I	NV_{DD}	—
Clocks				
SYS_CR_CLK_IN	U26	I	NV_{DD}	—
SYS_CR_CLK_OUT	U25	O	NV_{DD}	—
SYS_CLK_IN	U23	I	NV_{DD}	—
USB_CR_CLK_IN	T26	I	NV_{DD}	—
USB_CR_CLK_OUT	R26	O	NV_{DD}	—
USB_CLK_IN	T22	I	NV_{DD}	—
PCI_SYNC_OUT	U24	O	NV_{DD}	3
RTC_PIT_CLOCK	R22	I	NV_{DD}	—
PCI_SYNC_IN	T24	I	NV_{DD}	—
MISC				
THERM0	N1	I	NV_{DD}	7
THERM1	N3	I	NV_{DD}	7
PCI				
$\overline{\text{PCI\_INTA}}$	AF7	O	NV_{DD}	—
$\overline{\text{PCI\_RESET\_OUT}}$	AB11	O	NV_{DD}	—
PCI_AD0	AB20	I/O	NV_{DD}	—
PCI_AD1	AF23	I/O	NV_{DD}	—
PCI_AD2	AF22	I/O	NV_{DD}	—
PCI_AD3	AB19	I/O	NV_{DD}	—
PCI_AD4	AE22	I/O	NV_{DD}	—
PCI_AD5	AF21	I/O	NV_{DD}	—

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICOE*n*] parameters select whether the PCI_SYNC_OUT is driven out on the PCI_CLK_OUT*n* signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the SYS_CLK_IN signal should be tied to VSS.

As shown in Figure 57, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbc_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{\text{PCI\_SYNC\_IN} \times (1 + \sim\overline{\text{CFG\_CLKIN\_DIV}})\} \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~$\overline{\text{CFG\_CLKIN\_DIV}}$) is the SYS_CLK_IN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*, for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + \text{RCWL[DDRCM]})$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbc_clk* frequency is determined by the following equation:

$$lbc\_clk = csb\_clk \times (1 + \text{RCWL[LBCM]})$$

Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the a LBC clock divider to create the external local bus clock outputs (LCLK[0:1]). The LBC clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 63 specifies which units have a configurable clock frequency.

Table 63. Configurable Clock Units

Unit	Default Frequency	Options
TSEC1	*csb_clk*	Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3
TSEC2	*csb_clk*	Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3
Security Core, I^2C, SAP, TPR	*csb_clk*	Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3
USB DR	*csb_clk*	Off, *csb_clk*, *csb_clk*/2, *csb_clk*/3
PCI and DMA complex	*csb_clk*	Off, *csb_clk*

This table provides the operating frequencies for the MPC8313E TEPBGAII under recommended operating conditions (see Table 2).

Table 64. Operating Frequencies for TEPBGAII

Characteristic[1]	Maximum Operating Frequency	Unit
e300 core frequency (*core_clk*)	333	MHz
Coherent system bus frequency (*csb_clk*)	167	MHz
DDR1/2 memory bus frequency (MCK)[2]	167	MHz
Local bus frequency (LCLK*n*)[3]	66	MHz
PCI input frequency (SYS_CLK_IN or PCI_CLK)	66	MHz

Note:

1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK[0:1], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM] and SCCR[USBDRCM] must be programmed such that the maximum internal operating frequency of the security core and USB modules do not exceed their respective value listed in this table.
2. The DDR data rate is 2x the DDR memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbc_clk* frequency (depending on LCRR[CLKDIV]), which is in turn, 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

20.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. This table shows the multiplication factor encodings for the system PLL.

Table 65. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 70. Thermal Resistance for TEPBGAII with Heat Sink in Open Flow

Heat Sink Assuming Thermal Grease	Airflow	Thermal Resistance (°C/W)
Wakefield 53 × 53 × 2.5 mm pin fin	Natural convection	13.0
	0.5 m/s	10.6
	1 m/s	9.7
	2 m/s	9.2
	4 m/s	8.9
Aavid 35 × 31 × 23 mm pin fin	Natural convection	14.4
	0.5 m/s	11.3
	1 m/s	10.5
	2 m/s	9.9
	4 m/s	9.4
Aavid 30 × 30 × 9.4 mm pin fin	Natural convection	16.5
	0.5 m/s	13.5
	1 m/s	12.1
	2 m/s	10.9
	4 m/s	10.0
Aavid 43 × 41 × 16.5 mm pin fin	Natural convection	14.5
	0.5 m/s	11.7
	1 m/s	10.5
	2 m/s	9.7
	4 m/s	9.2

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in Table 70. More detailed thermal models can be made available on request.

21.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb (4.5 kg) force. If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

21.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction to case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)
T_C = case temperature of the package
$R_{\theta JC}$ = junction-to-case thermal resistance
P_D = power dissipation

22 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8313E SYS_CLK_IN

22.1 System Clocking

The MPC8313E includes three PLLs.

1. The platform PLL (AV_{DD2}) generates the platform clock from the externally supplied SYS_CLK_IN input in PCI host mode or SYS_CLK_IN/PCI_SYNC_IN in PCI agent mode. The frequency ratio between the platform and SYS_CLK_IN is selected using the platform PLL ratio configuration bits as described in Section 20.1, “System PLL Configuration.”
2. The e300 core PLL (AV_{DD1}) generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 20.2, “Core PLL Configuration.”
3. There is a PLL for the SerDes block.

22.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD1}, AV_{DD2}, and $SDAV_{DD}$, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 58, one to each of the five AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

This figure shows the PLL power supply filter circuits.

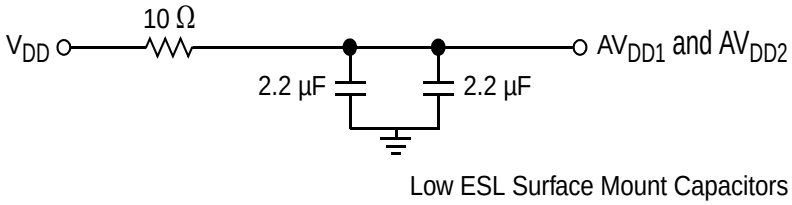
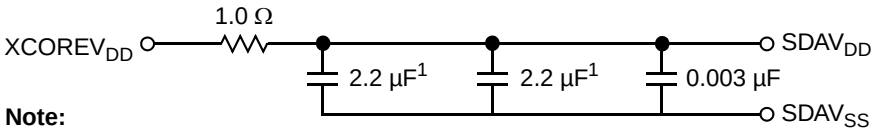


Figure 58. PLL Power Supply Filter Circuit

The $SDAV_{DD}$ signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit like the one shown in Figure 59. For maximum effectiveness, the filter circuit should be placed as closely as possible to the $SDAV_{DD}$ ball to ensure it filters out as much noise as possible. The ground connection should be near the $SDAV_{DD}$ ball. The 0.003-µF capacitor is closest to the ball, followed by the two 2.2-µF capacitors, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from traces from $SDAV_{DD}$ to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.



Note:
1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 59. SerDes PLL Power Supply Filter Circuit

Note the following:

- $SDAV_{DD}$ should be a filtered version of $XCOREV_{DD}$.

24 Revision History

This table summarizes a revision history for this document.

Table 73. Document Revision History

Rev. Number	Date	Substantive Change(s)
4	11/2011	• In Table 2, added following notes: – Note 3: Min temperature is specified with T_A; Max temperature is specified with T_J – Note 4: All Power rails must be connected and power applied to the MPC8313 even if the IP interfaces are not used. – Note 5: All I/O pins should be interfaced with peripherals operating at same voltage level. – Note 6: This voltage is the input to the filter discussed in Section 22.2, “PLL Power Supply Filtering.” and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter • Decoupled PCI_CLK and SYS_CLK_IN rise and fall times in Table 8. Relaxed maximum rise/fall time of SYS_CLK_IN to 4ns. • Added a note in Table 27 stating “The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm." • In Table 30: – Changed max value of t_{skrgt} in “Data to clock input skew (at receiver)” row from 2.8 to 2.6. – Added Note 7, stating that, “The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm.” • Added a note stating “eTSEC should be interfaced with peripheral operating at same voltage level” in Section 8.1.1, “TSEC DC Electrical Characteristics.” • TSEC1_MDC and TSEC_MDIO are powered at 3.3V by NVDD. Replaced LVDDA/LVDDB with NVDD and removed instances of 2.5V at several places in Section 8.5, “Ethernet Management Interface Electrical Characteristics.” • In Table 43, changed min/max values of t_{CLK_TOL} from 0.05 to 0.005. • In Table 62: – Added Note 2 for LGPL4 in showing LGPL4 as open-drain. – Removed Note 2 from TSEC1_MDIO. – Added Note 10: This pin has an internal pull-up. – Added Note 11: This pin has an internal pull-down. – Added Note 12: “In MII mode, GTX_CLK should be pulled down by 300 Ω to V_{SS}” to TSEC1_GTX_CLK and TSEC2_GTX_CLK. • In Section 19.1, “Package Parameters for the MPC8313E TEPBGAII,” replaced "5.5 Sn/0.5 Cu/4 Ag" with "Sn/3.5 Ag." • Added foot note 3 in Table 65 stating “The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.” • In Table 72: – Added AD = 266 and D = 266. – Added “C = 2.2” in “Revision level” column. – Added Note 4. • Changed resitor from 1.0 Ω to 10 Ω in Figure 58. • Replaced LCCR with LCRR throughout. • Added high-speed to USB Phy description.
3	01/2009	• Table 72, in column aa, changed to AG = 400 MHz.
2.2	12/2008	• Made cross-references active for sections, figures, and tables.
2.1	12/2008	• Added Figure 2, after Table 2 and renumbered the following figures.

Table 73. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
2	10/2008	• Added Note “The information in this document is accurate for revision 1.0, and 2.x and later. See Section 24.1, “Part Numbers Fully Addressed by this Document,” before Section 1, “Overview.” • Added part numbering details for all the silicon revisions in Table 74. • Changed V_{IH} from 2.7 V to 2.4 V in Table 7. • Added a row for V_{IH} level for Rev 2.x or later in Table 45. • Added a column for maximum power dissipation in low power mode for Rev 2.x or later silicon in Table 6. • Added a column for Power Nos for Rev 2.x or later silicon and added a row for 400 MHz in Table 4. • Removed footnote, “These are preliminary estimates.” from Table 4. • Added Table 21 for DDR AC Specs on Rev 2.x or later silicon. • Added Section 9, “High-Speed Serial Interfaces (HSSI).” • Added $\overline{\text{LFWE}}$, LFCLE, LFALE, $\overline{\text{LOE}}$, $\overline{\text{LFRE}}$, $\overline{\text{LFWP}}$, $\overline{\text{LGTA}}$, LUPWAIT, and $\overline{\text{LFRB}}$ in Table 63. • In Table 39, added note 2: “This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)” • Removed mentions of SGMII (SGMII has separate specs) from Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics.” • Corrected Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics,” to state that RGMII/RTBI interfaces only operate at 2.5 V, not 3.3 V. • Added ZQ package to ordering information In Table 74 and Section 19.1, “Package Parameters for the MPC8313E TEPBGAII” (applicable to both silicon rev. 1.0 and 2.1) • Removed footnotes 5 and 6 from Table 1 (left over when the PCI undershoot/overshoot voltages and maximum AC waveforms were removed from Section 2.1.2, “Power Supply Voltage Specification”). • Removed SD_PLL_TPD (T2) and SD_PLL_TPA_ANA (R4) from Table 63. • Added Section 8.3, “SGMII Interface Electrical Characteristics.” Removed Section 8.5.3 SGMII DC Electrical Characteristics. • Removed “HRESET negation to SRESET negation (output)” spec and changed “HRESET/SRESET assertion (output)” spec to “HRESET assertion (output)” in Table 10. • Clarified POR configuration signal specs to “Time for the device to turn off POR configuration signal drivers with respect to the assertion of HRESET” and “Time for the device to turn on POR configuration signal drivers with respect to the negation of HRESET” in Table 10. • Added Section 24.2, “Part Marking,” and Figure 62.