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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	267MHz
Co-Processors/DSP	Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8313ezqaddc

1.6 USB Dual-Role Controller

The MPC8313E USB controller includes the following features:

- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Compatible with *Universal Serial Bus Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI + low pin interface (ULPI) or on-chip USB 2.0 full-speed/high-speed PHY

1.7 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8313E eTSECs include the following features:

- Two RGMII/SGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3®, 802.3u®, 802.3x®, 802.3z®, 802.3au®, and 802.3ab®
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status
- Three-speed support (10/100/1000 Mbps)
- On-chip high-speed serial interface to external SGMII PHY interface
- Support for IEEE Std 1588™
- Support for two full-duplex FIFO interface modes
- Multiple PHY interface configuration
- TCP/IP acceleration and QoS features available
- IP v4 and IP v6 header recognition on receive
- IP v4 header checksum verification and generation
- TCP and UDP checksum verification and generation
- Per-packet configurable acceleration
- Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2®, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
- Transmission from up to eight physical queues.
- Reception to up to eight physical queues

- Full and half-duplex Ethernet support (1000 Mbps supports only full-duplex):
  - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE 802.1 virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision
  - CRC generation and verification of inbound/outbound packets
  - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
  - Exact match on primary and virtual 48-bit unicast addresses
    - VRRP and HSRP support for seamless router fail-over
  - Up to 16 exact-match MAC addresses supported
  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status

1.8 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model supports 5 external and 34 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

1.9 Power Management Controller (PMC)

The MPC8313E power management controller includes the following features:

- Provides power management when the device is used in both host and agent modes
- Supports PCI power management 1.2 D0, D1, D2, D3hot, and D3cold states
- On-chip split power supply controlled through external power switch for minimum standby power
- Support for PME generation in PCI agent mode, PME detection in PCI host mode
- Supports wake-up from Ethernet (Magic Packet), USB, GPIO, and PCI (PME input as host)

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value[1]	Unit	Current Requirement
Core supply voltage	V_{DD}	1.0 V ± 50 mV	V	469 mA
Internal core logic constant power	V_{DDC}	1.0 V ± 50 mV	V	377 mA
SerDes internal digital power	$XCOREV_{DD}$	1.0	V	170 mA
SerDes internal digital ground	$XCOREV_{SS}$	0.0	V	—
SerDes I/O digital power	$XPADV_{DD}$	1.0	V	10 mA
SerDes I/O digital ground	$XPADV_{SS}$	0.0	V	—
SerDes analog power for PLL	$SDAV_{DD}$	1.0 V ± 50 mV	V	10 mA
SerDes analog ground for PLL	$SDAV_{SS}$	0.0	V	—
Dedicated 3.3 V analog power for USB PLL	USB_PLL_PWR3	3.3 V ± 300 mV	V	2–3 mA
Dedicated 1.0 V analog power for USB PLL	USB_PLL_PWR1	1.0 V ± 50 mV	V	2–3 mA
Dedicated analog ground for USB PLL	USB_PLL_GND	0.0	V	—
Dedicated USB power for USB bias circuit	USB_VDDA_BIAS	3.3 V ± 300 mV	V	4–5 mA
Dedicated USB ground for USB bias circuit	USB_VSSA_BIAS	0.0	V	—
Dedicated power for USB transceiver	USB_VDDA	3.3 V ± 300 mV	V	75 mA
Dedicated ground for USB transceiver	USB_VSSA	0.0	V	—
Analog power for e300 core APLL	AV_{DD1} [6]	1.0 V ± 50 mV	V	2–3 mA
Analog power for system APLL	AV_{DD2} [6]	1.0 V ± 50 mV	V	2–3 mA
DDR1 DRAM I/O voltage (333 MHz, 32-bit operation)	GV_{DD}	2.5 V ± 125 mV	V	131 mA
DDR2 DRAM I/O voltage (333 MHz, 32-bit operation)	GV_{DD}	1.8 V ± 80 mV	V	140 mA
Differential reference voltage for DDR controller	MV_{REF}	1/2 DDR supply ($0.49 \times GV_{DD}$ to $0.51 \times GV_{DD}$)	V	—
Standard I/O voltage	NV_{DD}	3.3 V ± 300 mV[2]	V	74 mA
eTSEC2 I/O supply	LV_{DDA}	2.5 V ± 125 mV/ 3.3 V ± 300 mV	V	22 mA
eTSEC1/USB DR I/O supply	LV_{DDB}	2.5 V ± 125 mV/ 3.3 V ± 300 mV	V	44 mA
Supply for eLBC IOs	LV_{DD}	3.3 V ± 300 mV	V	16 mA
Analog and digital ground	V_{SS}	0.0	V	—
Junction temperature range	T_A/T_J [3]	0 to 105	°C	

4.2 AC Electrical Characteristics

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the system clock input (SYS_CLK_IN/PCI_CLK) AC timing specifications for the MPC8313E.

Table 8. SYS_CLK_IN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYS_CLK_IN/PCI_CLK frequency	$f_{SYS\_CLK\_IN}$	24	—	66.67	MHz	1
SYS_CLK_IN/PCI_CLK cycle time	$t_{SYS\_CLK\_IN}$	15	—	—	ns	—
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	0.6	0.8	4	ns	2
PCI_CLK rise and fall time	t_{PCH}, t_{PCL}	0.6	0.8	1.2	ns	2
SYS_CLK_IN/PCI_CLK duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3
SYS_CLK_IN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system, core, security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN/PCI_CLK are measured at 0.4 and 2.4 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8313E.

5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins.

Table 9. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) when GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	2.3	2.7	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.15	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.15	V	—

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Silicon Rev 2.x or Later

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK[*n*] cycle time, MCK[*n*]/$\overline{\text{MCK}}$[*n*] crossing	t_{MCK}	6	10	ns	2
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz	t_{DDKHAS}	 2.1 2.5	 — —	ns	3
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz	t_{DDKHAX}	 2.0 2.7	 — —	ns	3
$\overline{\text{MCS}}$[*n*] output setup with respect to MCK 333 MHz 266 MHz	t_{DDKHCS}	 2.1 3.15	 — —	ns	3
$\overline{\text{MCS}}$[*n*] output hold with respect to MCK 333 MHz 266 MHz	t_{DDKHCX}	 2.0 2.7	 — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS 333 MHz 266 MHz	t_{DDKHDS}, t_{DDKLDS}	 800 900	 — —	ps	5
MDQ//MDM output hold with respect to MDQS 333 MHz 266 MHz	t_{DDKHDX}, t_{DDKLDX}	 750 1000	 — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

NOTE

For the ADDR/CMD setup and hold specifications in Table 21, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

This figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

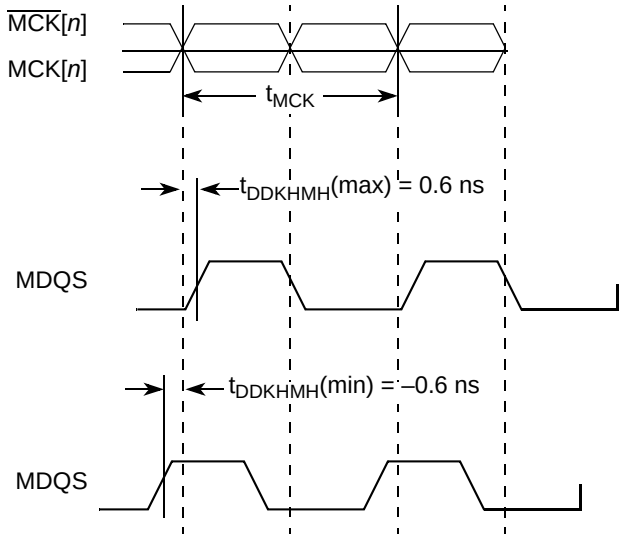


Figure 5. Timing Diagram for t_{DDKHMH}

This figure shows the DDR and DDR2 SDRAM output timing diagram.

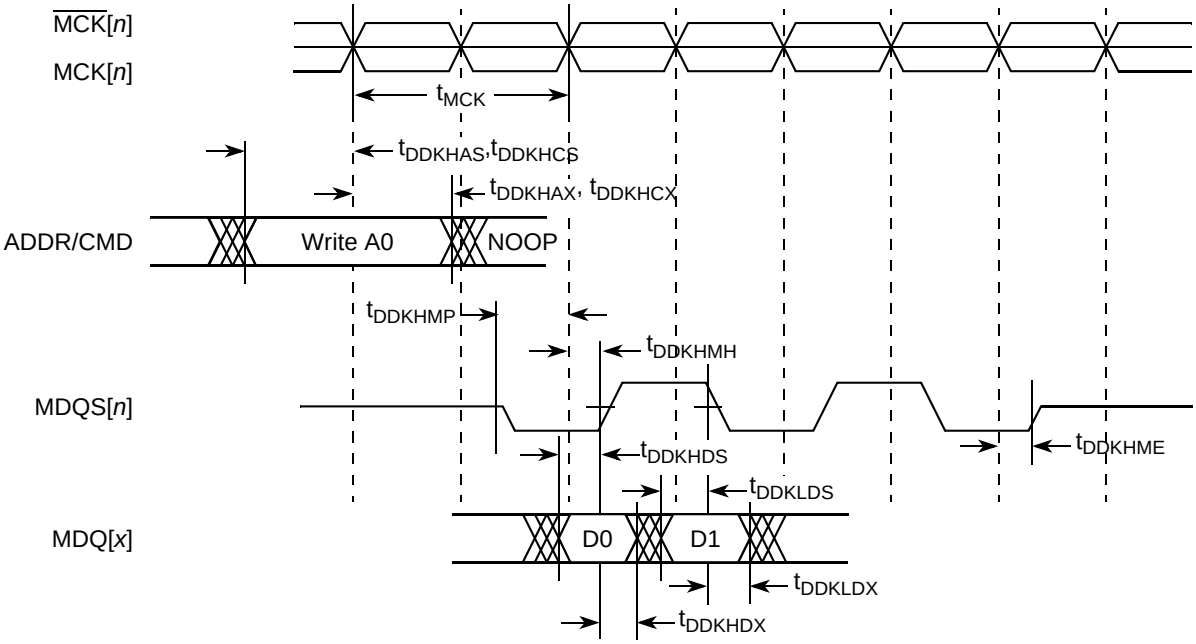


Figure 6. DDR and DDR2 SDRAM Output Timing Diagram

This figure shows the MII receive AC timing diagram.

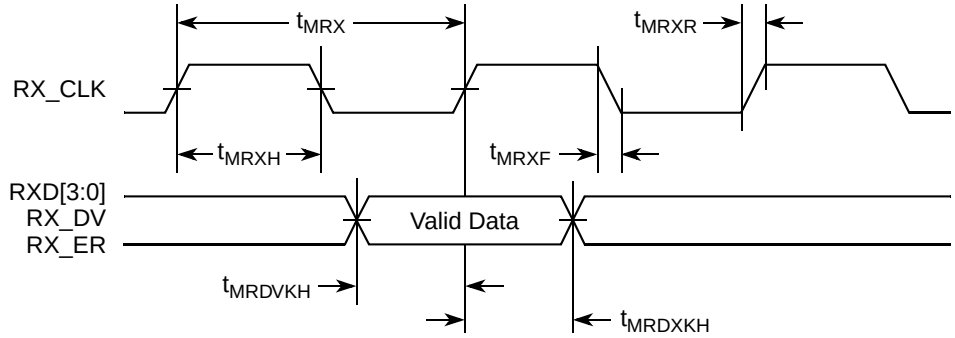


Figure 10. MII Receive AC Timing Diagram RMII AC Timing Specifications

8.2.1.3 RMII Transmit AC Timing Specifications

This table provides the RMII transmit AC timing specifications.

Table 28. RMII Transmit AC Timing Specifications

At recommended operating conditions with NV_{DD} of 3.3 V ± 0.3 V.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	10	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

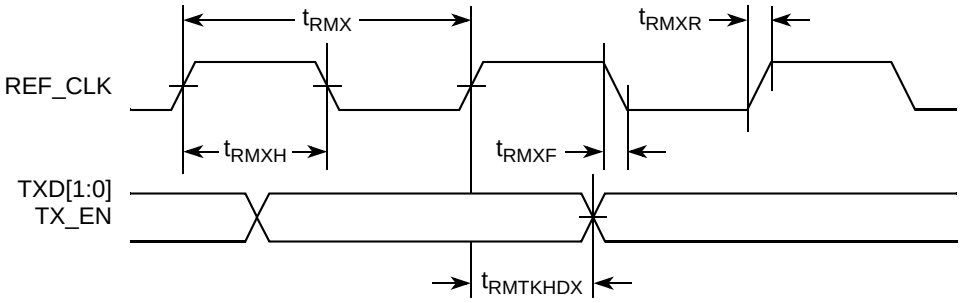


Figure 11. RMII Transmit AC Timing Diagram

Table 37. MII Management DC Electrical Characteristics When Powered at 3.3 V (continued)

Note:
1. Note that the symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

8.5.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 38. MII Management AC Timing Specifications

At recommended operating conditions with NV_{DD} is 3.3 V ± 0.3V

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	
MDC to MDIO delay	t_{MDKHDX}	10	—	170	ns	
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	
MDC rise time	t_{MDCR}	—	—	10	ns	
MDC fall time	t_{MDHF}	—	—	10	ns	

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)

This figure shows the MII management AC timing diagram.

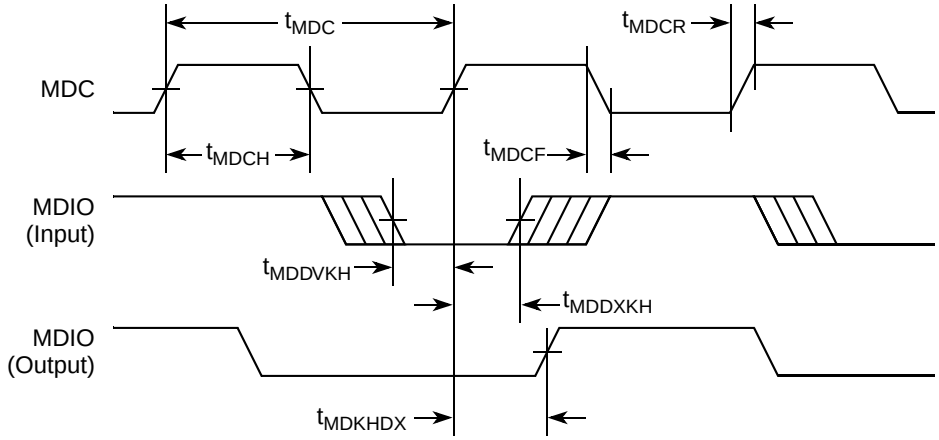


Figure 21. MII Management Interface Timing Diagram

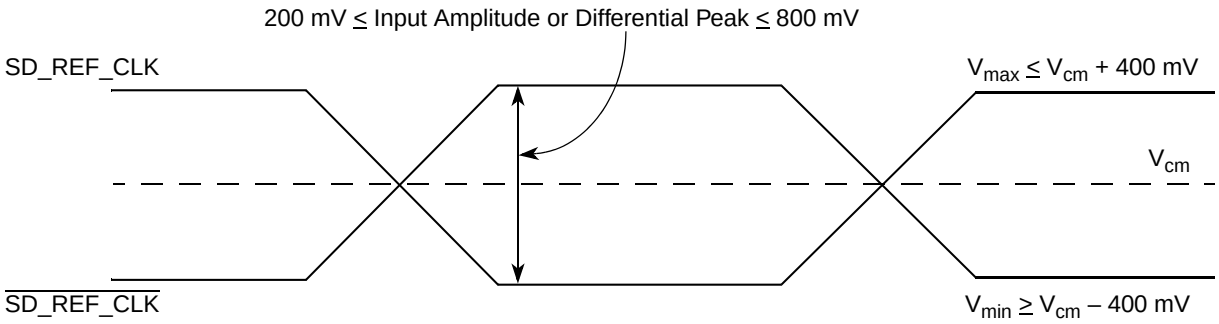


Figure 25. Differential Reference Clock Input DC Requirements (External AC-Coupled)

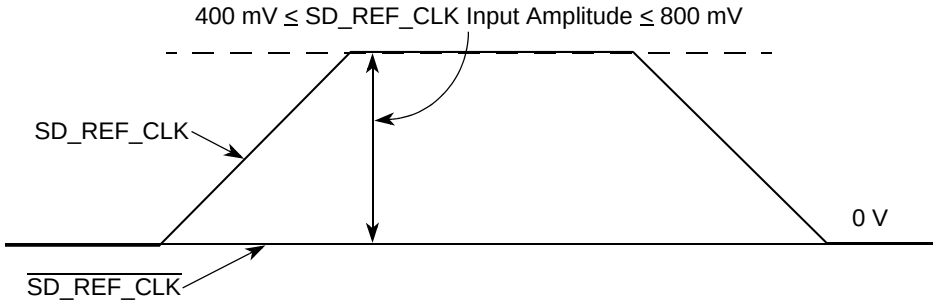


Figure 26. Single-Ended Reference Clock Input DC Requirements

9.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to $XCOREV_{SS}$, the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce a signal with too large of an amplitude and may need to be DC-biased at the clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC coupling.

NOTE

Figure 27 through Figure 30 are for conceptual reference only. Due to the fact that the clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is possible that the clock circuit reference designs provided by clock driver chip vendors are different from what is shown in the figures. They might also vary from one vendor to the other. Therefore, Freescale can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. It is recommended that the system designer contact the selected clock driver chip vendor for the optimal reference circuits for the MPC8313E SerDes reference clock receiver requirement provided in this document.

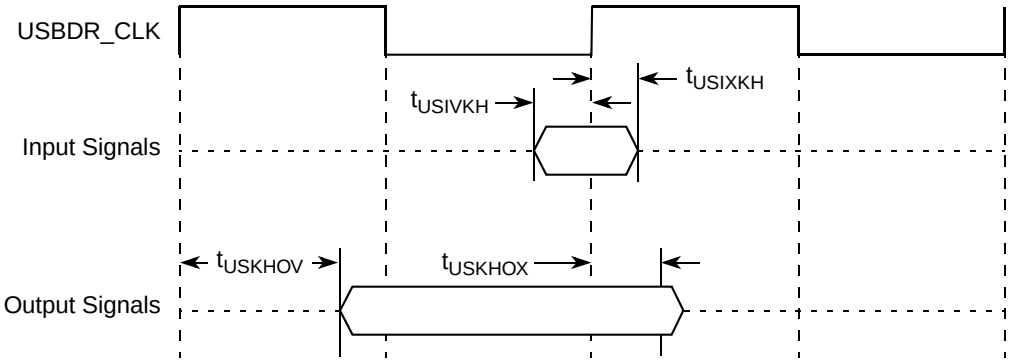


Figure 35. USB Signals

10.2 On-Chip USB PHY

This section describes the DC and AC electrical specifications for the on-chip USB PHY of the MPC8313E. See Chapter 7 in the *USB Specifications Rev. 2*, for more information.

This table provides the USB clock input (USB_CLK_IN) DC timing specifications.

Table 42. USB_CLK_IN DC Electrical Characteristics

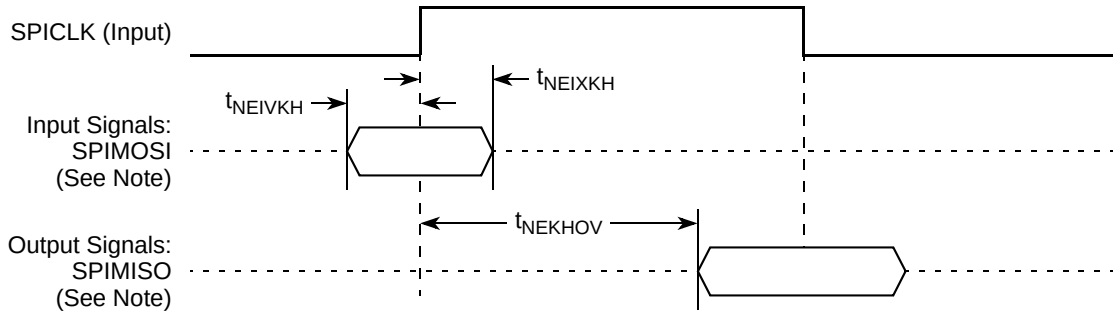
Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2.7	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	–0.3	0.4	V

This table provides the USB clock input (USB_CLK_IN) AC timing specifications.

Table 43. USB_CLK_IN AC Timing Specifications

Parameter/Condition	Conditions	Symbol	Min	Typ	Max	Unit
Frequency range	—	$f_{USB\_CLK\_IN}$	—	24	48	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	–0.005	0	0.005	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/time interval error	Peak-to-peak value measured with a second order high-pass filter of 500 kHz bandwidth	t_{CLK_PJ}	—	—	200	ps

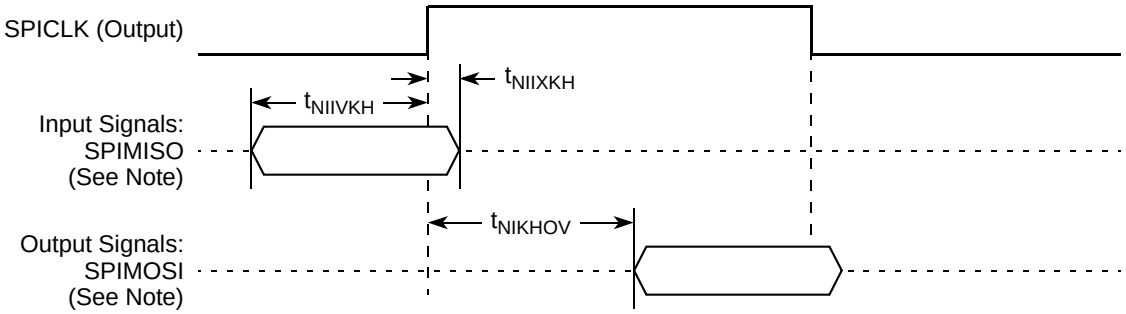
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 54. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 55. SPI AC Timing in Master Mode (Internal Clock) Diagram

19 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8313E is available in a thermally enhanced plastic ball grid array (TEPBGAII), see Section 19.1, "Package Parameters for the MPC8313E TEPBGAII," and Section 19.2, "Mechanical Dimensions of the MPC8313E TEPBGAII," for information on the TEPBGAII.

19.1 Package Parameters for the MPC8313E TEPBGAII

The package parameters are as provided in the following list. The package type is 27 mm × 27 mm, 516 TEPBGAII.

Package outline	27 mm × 27 mm
Interconnects	516
Pitch	1.00 mm
Module height (typical)	2.25 mm
Solder Balls	96.5 Sn/3.5 Ag(VR package) , 62 Sn/36 Pb/2 Ag (ZQ package) Ball diameter (typical)
0.6 mm	

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{MEMC\_MCS0}}$	D10	O	GV_{DD}	—
$\overline{\text{MEMC\_MCS1}}$	A10	O	GV_{DD}	—
MEMC_MCKE	B14	O	GV_{DD}	3
MEMC_MCK	A13	O	GV_{DD}	—
$\overline{\text{MEMC\_MCK}}$	A14	O	GV_{DD}	—
MEMC_MODT0	B23	O	GV_{DD}	—
MEMC_MODT1	C23	O	GV_{DD}	—
Local Bus Controller Interface				
LAD0	K25	I/O	LV_{DD}	11
LAD1	K24	I/O	LV_{DD}	11
LAD2	K23	I/O	LV_{DD}	11
LAD3	K22	I/O	LV_{DD}	11
LAD4	J25	I/O	LV_{DD}	11
LAD5	J24	I/O	LV_{DD}	11
LAD6	J23	I/O	LV_{DD}	11
LAD7	J22	I/O	LV_{DD}	11
LAD8	H24	I/O	LV_{DD}	11
LAD9	F26	I/O	LV_{DD}	11
LAD10	G24	I/O	LV_{DD}	11
LAD11	F25	I/O	LV_{DD}	11
LAD12	E25	I/O	LV_{DD}	11
LAD13	F24	I/O	LV_{DD}	11
LAD14	G22	I/O	LV_{DD}	11
LAD15	F23	I/O	LV_{DD}	11
LA16	AC25	O	LV_{DD}	11
LA17	AC26	O	LV_{DD}	11
LA18	AB22	O	LV_{DD}	11
LA19	AB23	O	LV_{DD}	11
LA20	AB24	O	LV_{DD}	11
LA21	AB25	O	LV_{DD}	11
LA22	AB26	O	LV_{DD}	11
LA23	E22	O	LV_{DD}	11

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
RXB	R1	I		—
$\overline{\text{RXB}}$	P1	I		—
SD_IMP_CAL_RX	V5	I		200 Ω ± 10% to GND
$\overline{\text{SD\_REF\_CLK}}$	T5	I		—
SD_REF_CLK	T4	I		—
SD_PLL_TPD	T2	O		—
SD_IMP_CAL_TX	N5	I		100 Ω ± 10% to GND
SDAVDD	R5	I/O		—
SD_PLL_TPA_ANA	R4	O		—
SDAVSS	R3	I/O		—
USB PHY				
USB_DP	P26	I/O		—
USB_DM	N26	I/O		—
USB_VBUS	P24	I/O		—
USB_TPA	L26	I/O		—
USB_RBIAS	M24	I/O		—
USB_PLL_PWR3	M26	I/O		—
USB_PLL_GND	N24	I/O		—
USB_PLL_PWR1	N25	I/O		—
USB_VSSA_BIAS	M25	I/O		—
USB_VDDA_BIAS	M22	I/O		—
USB_VSSA	N22	I/O		—
USB_VDDA	P22	I/O		—
GTM/USB				
USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2/LSRCID0	AD23	I/O	NV_{DD}	—
USBDR_PWRFAULT/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$/ LSRCID1	AE23	I/O	NV_{DD}	—
USBDR_PCTL0/$\overline{\text{GTM1\_TOUT1}}$/LSRCID2	AC22	O	NV_{DD}	—
USBDR_PCTL1/LBC_PM_REF_10/LSRCID3	AB21	O	NV_{DD}	—

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICOE*n*] parameters select whether the PCI_SYNC_OUT is driven out on the PCI_CLK_OUT*n* signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the SYS_CLK_IN signal should be tied to VSS.

As shown in Figure 57, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbc_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{\text{PCI\_SYNC\_IN} \times (1 + \sim\overline{\text{CFG\_CLKIN\_DIV}})\} \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~$\overline{\text{CFG\_CLKIN\_DIV}}$) is the SYS_CLK_IN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*, for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + \text{RCWL[DDRCM]})$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbc_clk* frequency is determined by the following equation:

$$lbc\_clk = csb\_clk \times (1 + \text{RCWL[LBCM]})$$

Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the a LBC clock divider to create the external local bus clock outputs (LCLK[0:1]). The LBC clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 63 specifies which units have a configurable clock frequency.

- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

22.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA}, or LV_{DDB} as required. Unused active high inputs should be connected to V_{SS}. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA}, LV_{DDB}, and V_{SS} pins of the device.

22.6 Output Buffer DC Impedance

The MPC8313E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to NV_{DD} or V_{SS}. Then, the value of each resistor is varied until the pad voltage is $NV_{DD}/2$ (see Figure 60). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $NV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

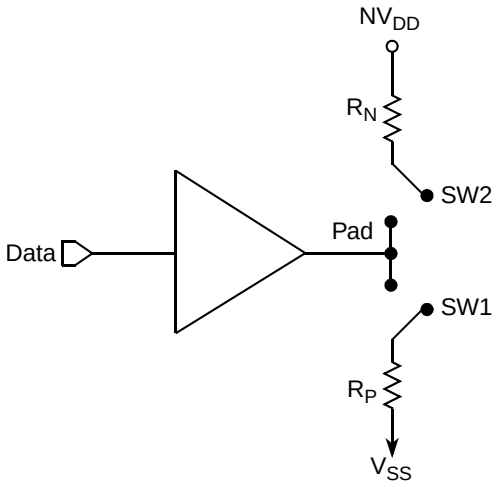
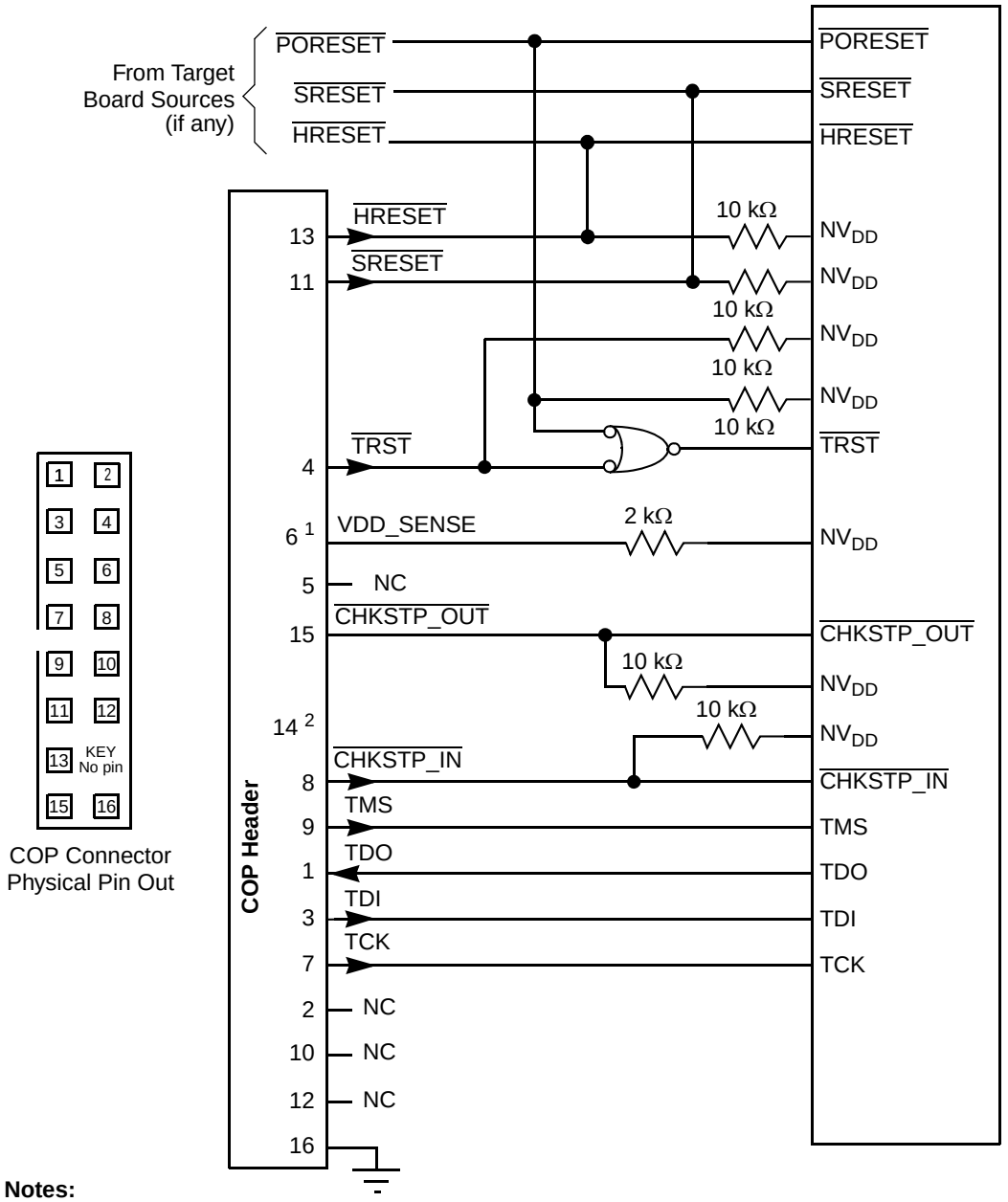


Figure 60. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.



Notes:
1. Some systems require power to be fed from the application board into the debugger repeater card via the COP header. In this case the resistor value for VDD_SENSE should be around 20 Ω.
2. Key location; pin 14 is not physically present on the COP header.

Figure 61. JTAG Interface Connection

23 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 23.1, “Part Numbers Fully Addressed by this Document.”

23.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the MPC8313E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 72. Part Numbering Nomenclature

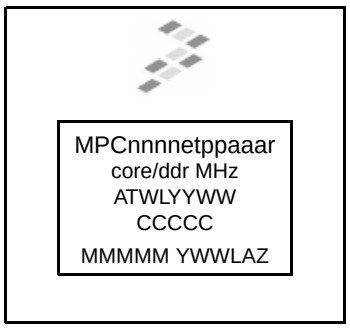
MPC	*nnnn*	*e*	*t*	*pp*	*aa*	*a*	*x*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range [3]**	**Package [1, 4]**	**e300 core Frequency [2]**	**DDR Frequency**	**Revision Level**
MPC	8313	Blank = Not included E = included	Blank = 0° to 105°C C= –40° to 105°C	ZQ = PB TEPBGAII VR = PB free TEPBGAII	AD = 266 MHz AF = 333 MHz AG = 400 MHz	D = 266 MHz F = 333 MHz	Blank = 1.0 A = 2.0 B = 2.1 C = 2.2

Note:

1. See Section 19, “Package and Pin Listings,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
3. Contact local Freescale office on availability of parts with °C temperature range.
4. ZQ package was available for Rev 1.0. For Rev 2.x, only VR package is available.

23.2 Part Marking

Parts are marked as shown in this figure.



TePBGA

Notes:
MPCnnnnetppaar is the orderable part number.
ATWLYYWW is the standard assembly, test, year, and work week codes.
CCCCC is the country code.
MMMMM is the mask number.

Figure 62. Part Marking for TEPBGAII Device

Table 73. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
1	3/2008	• In Table 63, added LBC_PM_REF_10 & LSRCID3 as muxed with USBDR_PCTL1 • In Table 63, added LSRCID2 as muxed with USBDR_PCTL0 • In Table 63, added LSRCID1 as muxed with USBDR_PWRFAULT • In Table 63, added LSRCID0 as muxed with USBDR_DRIVE_VBUS • In Table 63, moved T1, U2,& V2 from V_{DD} to XCOREVDD. • In Table 63, moved P2, R2, & T3 from V_{SS} to XCOREVSS. • In Table 63, moved P5, & U4 from V_{DD} to XPADVDD. • In Table 63, moved P3, & V4 from V_{SS} to XPADVSS. • In Table 63, removed “Double with pad” for AV_{DD1} and AV_{DD2} and moved AV_{DD1} and AV_{DD2} to Power and Ground Supplies section • In Table 63, added impedance control requirements for SD_IMP_CAL_TX (100 ohms to GND) and SD_IMP_CAL_RX (200 ohms to GND). • In Table 63, updated muxing in pinout to show new options for selecting IEEE 1588 functionality. Added footnote 8 • In Table 63, updated muxing in pinout to show new LBC ECC boot enable control muxed with eTSEC1_MDC • Added pin type information for power supplies. • Removed N1 and N3 from Vss section of Table 63. Added Therm0 and Therm1 (N1 and N3, respectively). Added note 7 to state: “Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.” • In Table 65 corrected maximum frequency of Local Bus Frequency from “33–66” to 66 MHz • In Table 65 corrected maximum frequency of PCI from “24–66” to 66 MHz • Added “which is determined by RCWLR[COREPLL],” to the note in Section 20.2, “Core PLL Configuration” about the VCO divider. • Added “(VCOD)” next to VCO divider column in Table 68. Added footnote stating that core_clk frequency must not exceed its maximum, so 2.5:1 and 3:1 *core_clk:csb_clk* ratios are invalid for certain *csb_clk* values. • In Table 69, notes were confusing. Added note 3 for VCO column, note 4 for CSB (*csb_clk*) column, note 5 for USB ref column, and note 6 to replace “Note 1”. Clarified note 4 to explain erratum eTSEC40. • In Table 69, updated note 6 to specify USB reference clock frequencies limited to 24 and 48 for rev. 2 silicon. • Replaced Table 71 “Thermal Resistance for TEPBGAII with Heat Sink in Open Flow”. • Removed last row of Table 19. • Removed 200 MHz rows from Table 21 and Table 5. • Changed VIH minimum spec from 2.0 to 2.1 for clock, PIC, JTAG, SPI, and reset pins in Table 9, Table 47, Table 54, Table 59, and Table 61. • Added Figure 4 showing the DDR input timing diagram. • In Table 19, removed “MDM” from the “MDQS-MDQ/MECC/MDM” text under the Parameter column for the tCISKEW parameter. MDM is an output signal and should be removed from the input AC timing spec table (tCISKEW). • Added “and power” to rows 2 and 3 in Table 10 • Added the sentence “Once both the power supplies...” and PORESET to Section 2.2, “Power Sequencing,” and Figure 3. • In Figure 35, corrected “USB0_CLK/USB1_CLK/DR_CLK” with “USBDR_CLK” • In Table 42, clarified that AC specs are for ULPI only.
0	6/2007	Initial release.

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