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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Security; SEC 2.2
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8313ezqaff

1 Overview

The MPC8313E incorporates the e300c3 core, which includes 16 Kbytes of L1 instruction and data caches and on-chip memory management units (MMUs). The MPC8313E has interfaces to dual enhanced three-speed 10/100/1000 Mbps Ethernet controllers, a DDR1/DDR2 SDRAM memory controller, an enhanced local bus controller, a 32-bit PCI controller, a dedicated security engine, a USB 2.0 dual-role controller and an on-chip high-speed PHY, a programmable interrupt controller, dual I²C controllers, a 4-channel DMA controller, and a general-purpose I/O port. This figure shows a block diagram of the MPC8313E.

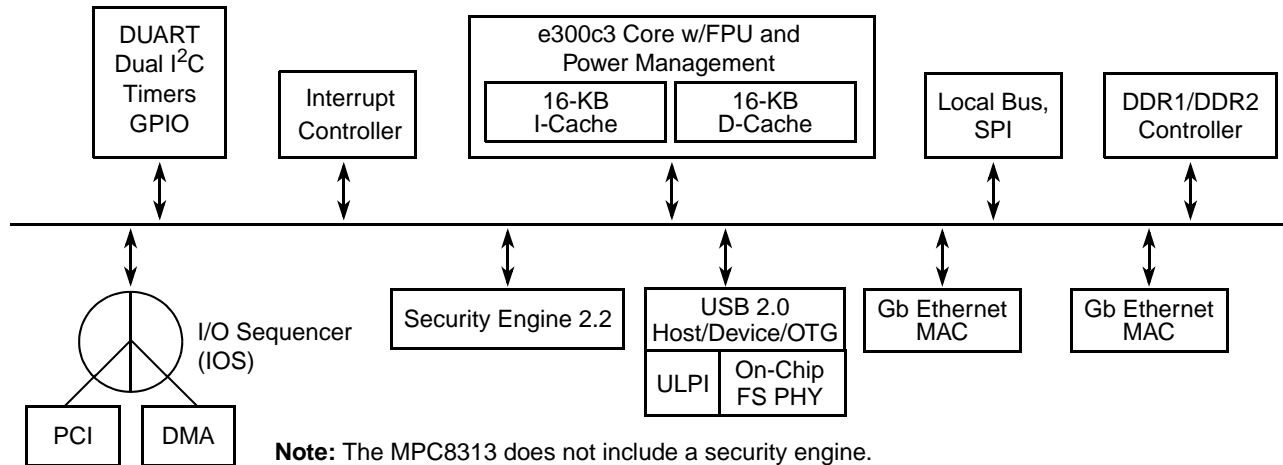


Figure 1. MPC8313E Block Diagram

The MPC8313E security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

1.1 MPC8313E Features

The following features are supported in the MPC8313E:

- Embedded PowerPC™ e300 processor core built on Power Architecture™ technology; operates at up to 333 MHz.
- High-performance, low-power, and cost-effective host processor
- DDR1/DDR2 memory controller—one 16-/32-bit interface at up to 333 MHz supporting both DDR1 and DDR2
- 16-Kbyte instruction cache and 16-Kbyte data cache, a floating point unit, and two integer units
- Peripheral interfaces such as 32-bit PCI interface with up to 66-MHz operation, 16-bit enhanced local bus interface with up to 66-MHz operation, and USB 2.0 (high speed) with an on-chip PHY.
- Security engine provides acceleration for control and data plane security protocols
- Power management controller for low-power consumption
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration

1.2 Serial Interfaces

The following interfaces are supported in the MPC8313E: dual UART, dual I²C, and an SPI interface.

1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE Std 802.11i®, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are as follows:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-224, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

1.4 DDR Memory Controller

The MPC8313E DDR1/DDR2 memory controller includes the following features:

- Single 16- or 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 333 MHz
- Support for two physical banks (chip selects), each bank independently addressable
- 64-Mbit to 2-Gbit (for DDR1) and to 4-Gbit (for DDR2) devices with x8/x16/x32 data ports (no direct x4 support)
- Support for one 16-bit device or two 8-bit devices on a 16-bit bus, or one 32-bit device or two 16-bit devices on a 32-bit bus
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

1.5 PCI Controller

The MPC8313E PCI controller includes the following features:

- PCI specification revision 2.3 compatible
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

1.6 USB Dual-Role Controller

The MPC8313E USB controller includes the following features:

- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Compatible with *Universal Serial Bus Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
 - Supports one upstream facing port
 - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
 - Supports USB root hub with one downstream-facing port
 - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI + low pin interface (ULPI) or on-chip USB 2.0 full-speed/high-speed PHY

1.7 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8313E eTSECs include the following features:

- Two RGMII/SGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3®, 802.3u®, 802.3x®, 802.3z®, 802.3au®, and 802.3ab®
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status
- Three-speed support (10/100/1000 Mbps)
- On-chip high-speed serial interface to external SGMII PHY interface
- Support for IEEE Std 1588™
- Support for two full-duplex FIFO interface modes
- Multiple PHY interface configuration
- TCP/IP acceleration and QoS features available
- IP v4 and IP v6 header recognition on receive
- IP v4 header checksum verification and generation
- TCP and UDP checksum verification and generation
- Per-packet configurable acceleration
- Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2®, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
- Transmission from up to eight physical queues.
- Reception to up to eight physical queues



- Full and half-duplex Ethernet support (1000 Mbps supports only full-duplex):
 - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
 - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE 802.1 virtual local area network (VLAN) tags and priority
 - VLAN insertion and deletion
 - Per-frame VLAN control word or default VLAN for each eTSEC
 - Extracted VLAN control word passed to software separately
 - Retransmission following a collision
 - CRC generation and verification of inbound/outbound packets
 - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition:
 - Exact match on primary and virtual 48-bit unicast addresses
 - VRRP and HSRP support for seamless router fail-over
 - Up to 16 exact-match MAC addresses supported
 - Broadcast address (accept/reject)
 - Hash table match on up to 512 multicast addresses
 - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status

1.8 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model supports 5 external and 34 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

1.9 Power Management Controller (PMC)

The MPC8313E power management controller includes the following features:

- Provides power management when the device is used in both host and agent modes
- Supports PCI power management 1.2 D0, D1, D2, D3hot, and D3cold states
- On-chip split power supply controlled through external power switch for minimum standby power
- Support for PME generation in PCI agent mode, PME detection in PCI host mode
- Supports wake-up from Ethernet (Magic Packet), USB, GPIO, and PCI (PME input as host)

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings¹

Characteristic		Symbol	Max Value	Unit	Note
Core supply voltage		V_{DD}	-0.3 to 1.26	V	—
PLL supply voltage		AV_{DD}	-0.3 to 1.26	V	—
Core power supply for SerDes transceivers		$XCOREV_{DD}$	-0.3 to 1.26	V	—
Pad power supply for SerDes transceivers		$XPADV_{DD}$	-0.3 to 1.26	V	—
DDR and DDR2 DRAM I/O voltage		GV_{DD}	-0.3 to 2.75 -0.3 to 1.98	V	—
PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage		NV_{DD}/LV_{DD}	-0.3 to 3.6	V	—
eTSEC, USB		LV_{DDA}/LV_{DDB}	-0.3 to 3.6	V	—
Input voltage	DDR DRAM signals	MV_{IN}	-0.3 to ($GV_{DD} + 0.3$)	V	2, 5
	DDR DRAM reference	MV_{REF}	-0.3 to ($GV_{DD} + 0.3$)	V	2, 5
	Enhanced three-speed Ethernet signals	LV_{IN}	-0.3 to ($LV_{DDA} + 0.3$) or -0.3 to ($LV_{DDB} + 0.3$)	V	4, 5
	Local bus, DUART, SYS_CLK_IN, system control, and power management, I ² C, and JTAG signals	NV_{IN}	-0.3 to ($NV_{DD} + 0.3$)	V	3, 5
	PCI	NV_{IN}	-0.3 to ($NV_{DD} + 0.3$)	V	6
Storage temperature range		T_{STG}	-55 to 150	°C	—

Notes:

- Functional and tested operating conditions are given in [Table 2](#). Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** NV_{IN} must not exceed NV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution:** LV_{IN} must not exceed LV_{DDA}/LV_{DDB} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the MPC8313E. Note that the values in this table are the recommended and tested operating conditions. If a particular block is given a voltage falling within the range in the Recommended Value column, the MPC8313E is capable of delivering the amount of current listed in the Current Requirement column; this is the maximum current possible. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value ¹	Unit	Current Requirement
Core supply voltage	V_{DD}	1.0 V \pm 50 mV	V	469 mA
Internal core logic constant power	V_{DDC}	1.0 V \pm 50 mV	V	377 mA
SerDes internal digital power	$XCOREV_{DD}$	1.0	V	170 mA
SerDes internal digital ground	$XCOREV_{SS}$	0.0	V	—
SerDes I/O digital power	$XPADV_{DD}$	1.0	V	10 mA
SerDes I/O digital ground	$XPADV_{SS}$	0.0	V	—
SerDes analog power for PLL	$SDAV_{DD}$	1.0 V \pm 50 mV	V	10 mA
SerDes analog ground for PLL	$SDAV_{SS}$	0.0	V	—
Dedicated 3.3 V analog power for USB PLL	USB_PLL_PWR3	3.3 V \pm 300 mV	V	2–3 mA
Dedicated 1.0 V analog power for USB PLL	USB_PLL_PWR1	1.0 V \pm 50 mV	V	2–3 mA
Dedicated analog ground for USB PLL	USB_PLL_GND	0.0	V	—
Dedicated USB power for USB bias circuit	USB_VDDA_BIAS	3.3 V \pm 300 mV	V	4–5 mA
Dedicated USB ground for USB bias circuit	USB_VSSA_BIAS	0.0	V	—
Dedicated power for USB transceiver	USB_VDDA	3.3 V \pm 300 mV	V	75 mA
Dedicated ground for USB transceiver	USB_VSSA	0.0	V	—
Analog power for e300 core APLL	AV_{DD1} ⁶	1.0 V \pm 50 mV	V	2–3 mA
Analog power for system APLL	AV_{DD2} ⁶	1.0 V \pm 50 mV	V	2–3 mA
DDR1 DRAM I/O voltage (333 MHz, 32-bit operation)	GV_{DD}	2.5 V \pm 125 mV	V	131 mA
DDR2 DRAM I/O voltage (333 MHz, 32-bit operation)	GV_{DD}	1.8 V \pm 80 mV	V	140 mA
Differential reference voltage for DDR controller	MV_{REF}	1/2 DDR supply ($0.49 \times GV_{DD}$ to $0.51 \times GV_{DD}$)	V	—
Standard I/O voltage	NV_{DD}	3.3 V \pm 300 mV ²	V	74 mA
eTSEC2 I/O supply	LV_{DDA}	2.5 V \pm 125 mV/ 3.3 V \pm 300 mV	V	22 mA
eTSEC1/USB DR I/O supply	LV_{DDB}	2.5 V \pm 125 mV/ 3.3 V \pm 300 mV	V	44 mA
Supply for eLBC IOs	LV_{DD}	3.3 V \pm 300 mV	V	16 mA
Analog and digital ground	V_{SS}	0.0	V	—
Junction temperature range	T_A/T_J ³	0 to 105	°C	

Table 3. Output Drive Capability (continued)

Driver Type	Output Impedance (Ω)	Supply Voltage
DDR2 signal	18	$GV_{DD} = 1.8\text{ V}$
DUART, system control, I ² C, JTAG, SPI	42	$NV_{DD} = 3.3\text{ V}$
GPIO signals	42	$NV_{DD} = 3.3\text{ V}$
eTSEC signals	42	$LV_{DDA}, LV_{DDB} = 2.5/3.3\text{ V}$
USB signals	42	$LV_{DDB} = 2.5/3.3\text{ V}$

2.2 Power Sequencing

The MPC8313E does not require the core supply voltage (V_{DD} and V_{DDC}) and I/O supply voltages (GV_{DD} , LV_{DD} , and NV_{DD}) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD} and V_{DDC}) before the I/O voltage (GV_{DD} , LV_{DD} , and NV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating $\overline{\text{PORESET}}$.

Note that there is no specific power down sequence requirement for the MPC8313E. I/O voltage supplies (GV_{DD} , LV_{DD} , and NV_{DD}) do not have any ordering requirements with respect to one another.

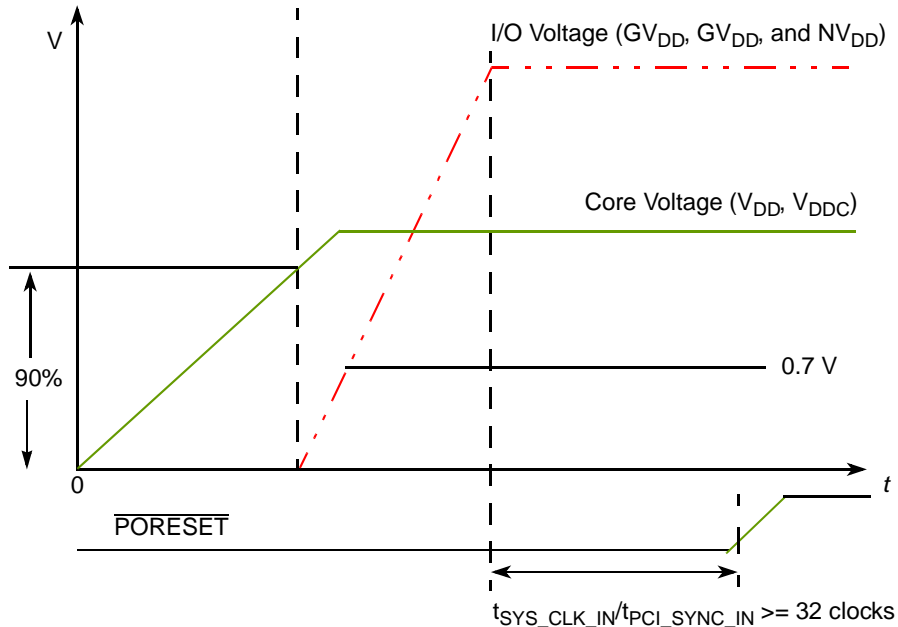


Figure 3. Power-Up Sequencing Example

This table provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(\text{typ}) = 2.5 \text{ V}$.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of $2.5 \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	—	V	—

This table provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions, with GV_{DD} of $2.5 \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ	t_{CISKEW}	—	—	ps	1, 2
333 MHz	—	-750	750	—	—
266 MHz	—	-750	750	—	—

Notes:

- t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

This figure illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

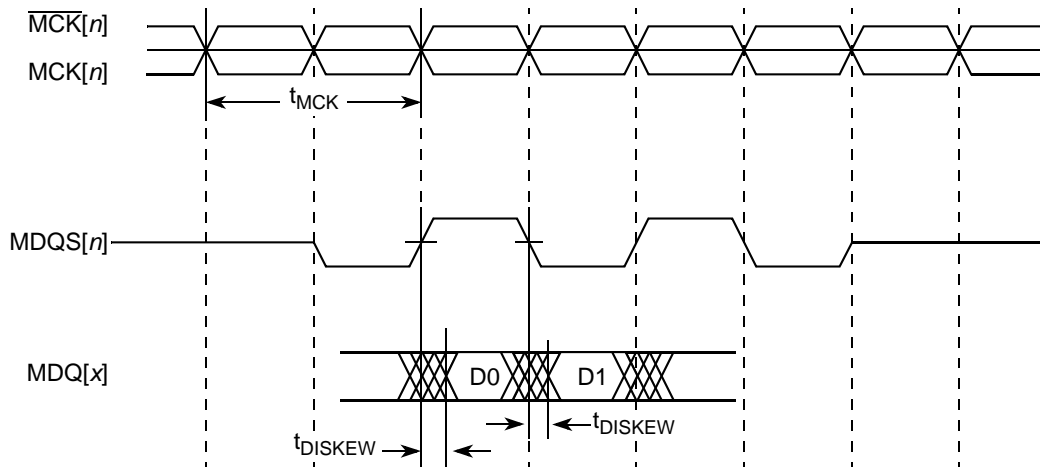


Figure 4. DDR Input Timing Diagram

This figure provides the AC test load for the DDR bus.

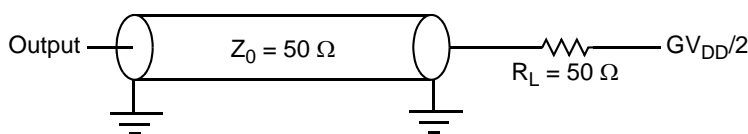


Figure 7. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 22. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.0	$NV_{DD} + 0.3$	V
Low-level input voltage NV_{DD}	V_{IL}	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$NV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V
Input current ($0 V \leq V_{IN} \leq NV_{DD}$)	I_{IN}	—	± 5	μA

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:

1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all the media independent interface (MII), reduced gigabit media independent interface (RGMII), serial gigabit media independent interface (SGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the MII interface can be operated at 3.3 V. The RMII and SGMII interfaces can be operated at either 3.3 or 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for *Gigabit Ethernet Physical Layer Device Specification Version 1.2a* (9/22/2000). The electrical characteristics for MDIO and MDC are specified in [Section 8.5, “Ethernet Management Interface Electrical Characteristics.”](#)

8.1.1 TSEC DC Electrical Characteristics

All RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in [Table 24](#) and [Table 25](#). The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

NOTE

eTSEC should be interfaced with peripheral operating at same voltage level.

Table 24. MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV _{DDA} /LV _{DDB}	—		2.97	3.63	V
Output high voltage	V _{OH}	I _{OH} = -4.0 mA	LV _{DDA} or LV _{DDB} = Min	2.40	LV _{DDA} + 0.3 or LV _{DDB} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 4.0 mA	LV _{DDA} or LV _{DDB} = Min	V _{SS}	0.50	V
Input high voltage	V _{IH}	—	—	2.0	LV _{DDA} + 0.3 or LV _{DDB} + 0.3	V
Input low voltage	V _{IL}	—	—	-0.3	0.90	V
Input high current	I _{IH}	V _{IN} ¹ = LV _{DDA} or LV _{DDB}		—	40	μA
Input low current	I _{IL}	V _{IN} ¹ = V _{SS}		-600	—	μA

Note:

1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

Table 25. RGMII/RTBI DC Electrical Characteristics

Parameters	Symbol	Conditions	Min	Max	Unit
Supply voltage 2.5 V	LV _{DDA} /LV _{DDB}	—	2.37	2.63	V

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

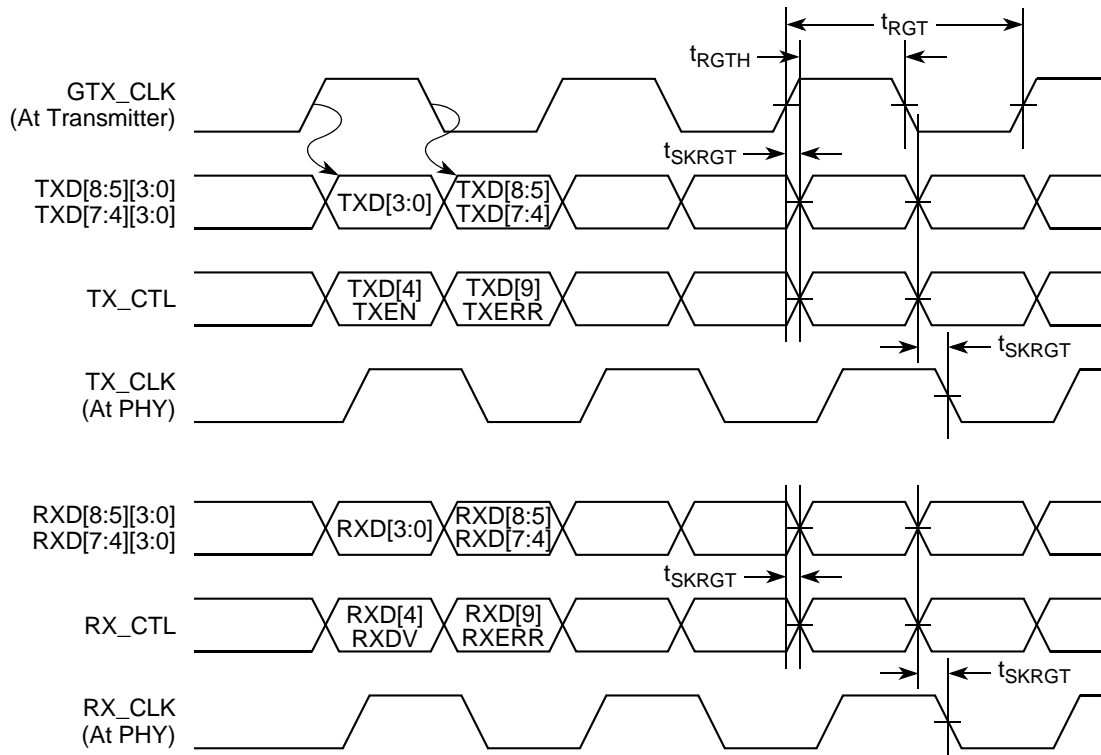


Figure 14. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-coupled serial link from the dedicated SerDes interface of MPC8313E as shown in [Figure 15](#), where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features a 50- Ω output impedance. Each input of the SerDes receiver differential pair features 50- Ω on-die termination to XCOREVSS. The reference circuit of the SerDes transmitter and receiver is shown in [Figure 33](#).

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in [Section 22.5, "Connection Recommendations,"](#) as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the TSEC_GTX_CLK125 clock is not required for this port. Instead, the SerDes reference clock is required on SD_REF_CLK and $\overline{SD_REF_CLK}$ pins.

8.3.1 DC Requirements for SGMII $\overline{SD_REF_CLK}$ and $\overline{SD_REF_CLK}$

The characteristics and DC requirements of the separate SerDes reference clock are described in [Section 9, "High-Speed Serial Interfaces \(HSSI\)."](#)

Table 35. SGMII Receive AC Timing Specifications (continued)

At recommended operating conditions with $XCOREV_{DD} = 1.0\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Total jitter tolerance	JT	0.65	—	—	UI p-p	1
Bit error ratio	BER	—	—	10^{-12}		
Unit interval	UI	799.92	800	800.08	ps	2
AC coupling capacitor	C_{TX}	5	—	200	nF	3

Notes:

1. Measured at receiver.
2. Each UI is $800\text{ ps} \pm 100\text{ ppm}$.
3. The external AC coupling capacitor is required. It is recommended to be placed near the device transmitter outputs.

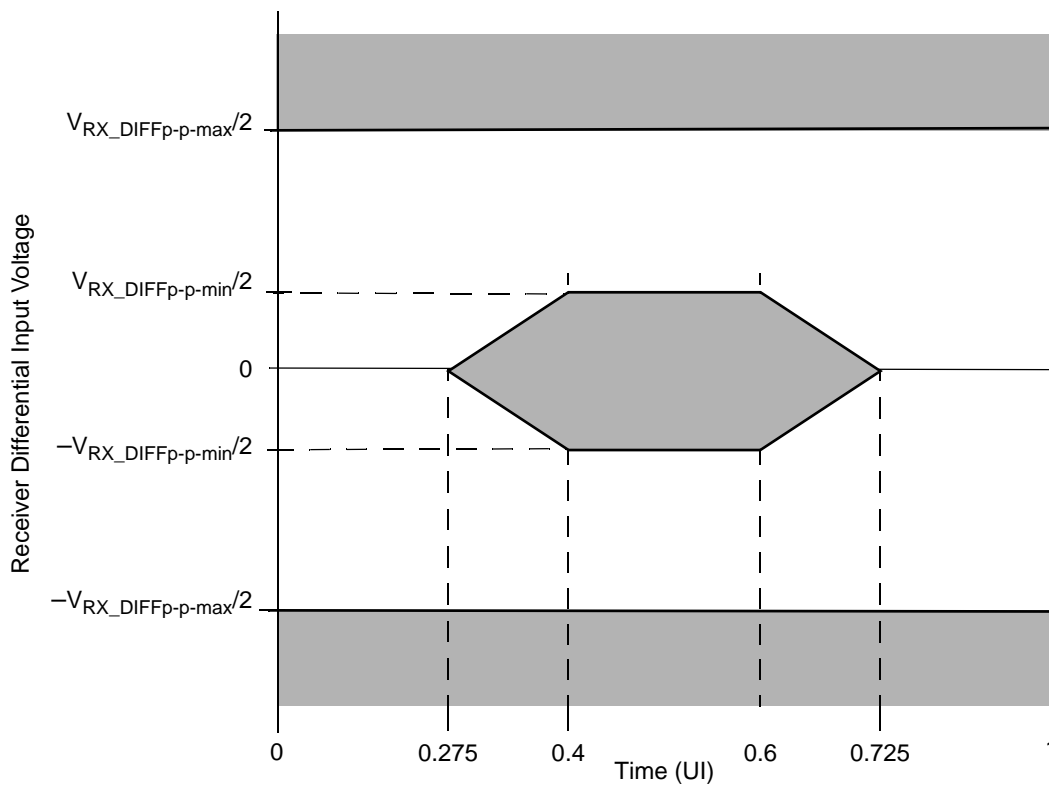


Figure 17. SGMII Receiver Input Compliance Mask

9 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

9.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 22 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TX_n and $\overline{TX_n}$) or a receiver input (RX_n and $\overline{RX_n}$). Each signal swings between A volts and B volts where $A > B$.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-ended swing
The transmitter output signals and the receiver input signals TX_n , $\overline{TX_n}$, RX_n , and $\overline{RX_n}$ each have a peak-to-peak swing of $A - B$ volts. This is also referred as each signal wire's single-ended swing.
2. Differential output voltage, V_{OD} (or differential output swing):
The differential output voltage (or swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{TX_n} - V_{\overline{TX_n}}$. The V_{OD} value can be either positive or negative.
3. Differential input voltage, V_{ID} (or differential input swing):
The differential input voltage (or swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{RX_n} - V_{\overline{RX_n}}$. The V_{ID} value can be either positive or negative.
4. Differential peak voltage, V_{DIFFp}
The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.
5. Differential peak-to-peak, $V_{DIFFp-p}$
Since the differential output signal of the transmitter and the differential input signal of the receiver each range from $A - B$ to $-(A - B)$ volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |A - B|$ volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.
6. Differential waveform
The differential waveform is constructed by subtracting the inverting signal (TX_n , for example) from the non-inverting signal ($\overline{TX_n}$, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 22 as an example for differential waveform.
7. Common mode voltage, V_{cm}

of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

- For external DC-coupled connection, as described in [Section 9.2.1, “SerDes Reference Clock Receiver Characteristics,”](#) the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. [Figure 24](#) shows the SerDes reference clock input requirement for the DC-coupled connection scheme.
- For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to $XCOREV_{SS}$. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage ($XCOREV_{SS}$). [Figure 25](#) shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- Single-ended mode
 - The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-to-peak (from V_{min} to V_{max}) with SD_REF_CLK either left unconnected or tied to ground.
 - The SD_REF_CLK input average voltage must be between 200 and 400 mV. [Figure 26](#) shows the SerDes reference clock input requirement for the single-ended signaling mode.
 - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC coupled externally. For the best noise performance, the reference of the clock could be DC or AC coupled into the unused phase (SD_REF_CLK) through the same source impedance as the clock input (SD_REF_CLK) in use.

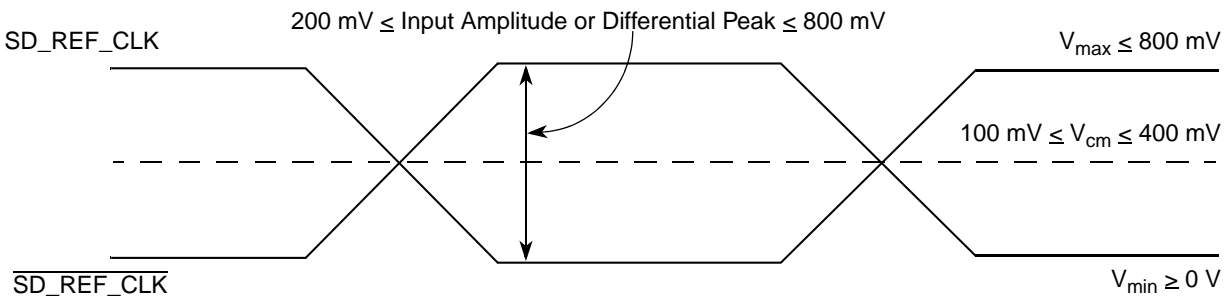


Figure 24. Differential Reference Clock Input DC Requirements (External DC-Coupled)

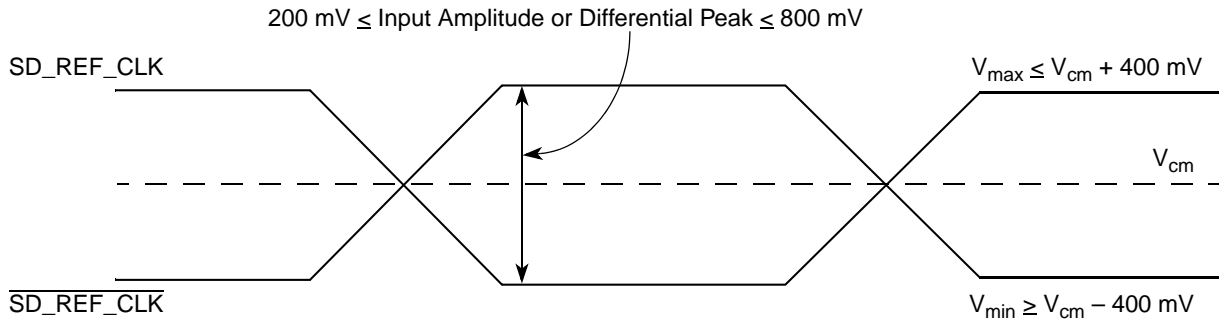


Figure 25. Differential Reference Clock Input DC Requirements (External AC-Coupled)

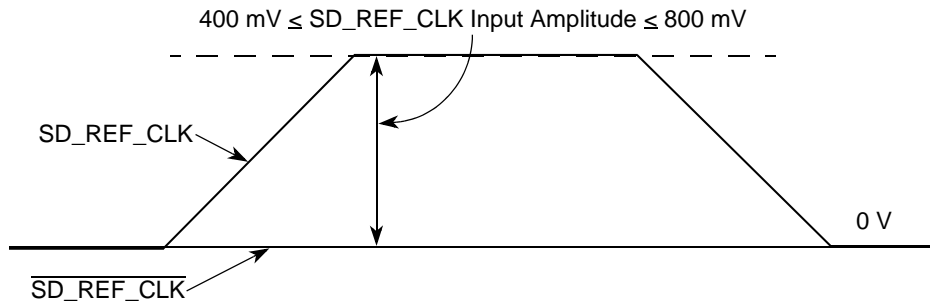


Figure 26. Single-Ended Reference Clock Input DC Requirements

9.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to $XCOREV_{SS}$, the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce a signal with too large of an amplitude and may need to be DC-biased at the clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC coupling.

NOTE

Figure 27 through Figure 30 are for conceptual reference only. Due to the fact that the clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is possible that the clock circuit reference designs provided by clock driver chip vendors are different from what is shown in the figures. They might also vary from one vendor to the other. Therefore, Freescale can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. It is recommended that the system designer contact the selected clock driver chip vendor for the optimal reference circuits for the MPC8313E SerDes reference clock receiver requirement provided in this document.

This figure shows the AC timing diagram for the I²C bus.

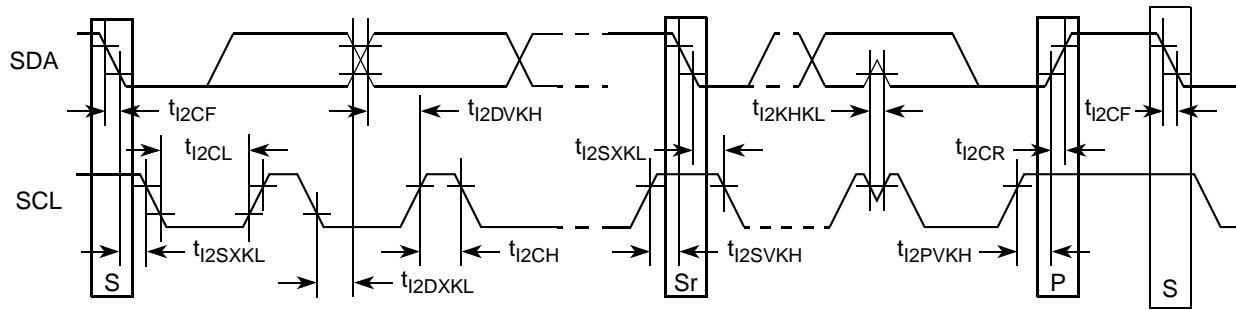


Figure 47. I²C Bus AC Timing Diagram

14 PCI

This section describes the DC and AC electrical specifications for the PCI bus.

14.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface.

Table 50. PCI DC Electrical Characteristics¹

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH} (\text{min})$ or	$0.5 \times NV_{DD}$	$NV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL} (\text{max})$	-0.5	$0.3 \times NV_{DD}$	V
High-level output voltage	V_{OH}	$NV_{DD} = \text{min}, I_{OH} = -100 \mu\text{A}$	$0.9 \times NV_{DD}$	—	V
Low-level output voltage	V_{OL}	$NV_{DD} = \text{min}, I_{OL} = 100 \mu\text{A}$	—	$0.1 \times NV_{DD}$	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq NV_{DD}$	—	± 5	μA

Note:

- Note that the symbol V_{IN} , in this case, represents the NV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

14.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8313E is configured as a host or agent device.

This table shows the PCI AC timing specifications at 66 MHz.

Table 51. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol ¹	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2

Table 62. MPC8313E TEPBGAI Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TMS	E4	I	NV _{DD}	4
$\overline{\text{TRST}}$	E5	I	NV _{DD}	4
TEST				
TEST_MODE	F4	I	NV _{DD}	6
DEBUG				
$\overline{\text{QUIESCE}}$	F5	O	NV _{DD}	—
System Control				
$\overline{\text{HRESET}}$	F2	I/O	NV _{DD}	1
$\overline{\text{PORESET}}$	F3	I	NV _{DD}	—
$\overline{\text{SRESET}}$	F1	I	NV _{DD}	—
Clocks				
SYS_CR_CLK_IN	U26	I	NV _{DD}	—
SYS_CR_CLK_OUT	U25	O	NV _{DD}	—
SYS_CLK_IN	U23	I	NV _{DD}	—
USB_CR_CLK_IN	T26	I	NV _{DD}	—
USB_CR_CLK_OUT	R26	O	NV _{DD}	—
USB_CLK_IN	T22	I	NV _{DD}	—
PCI_SYNC_OUT	U24	O	NV _{DD}	3
RTC_PIT_CLOCK	R22	I	NV _{DD}	—
PCI_SYNC_IN	T24	I	NV _{DD}	—
MISC				
THERM0	N1	I	NV _{DD}	7
THERM1	N3	I	NV _{DD}	7
PCI				
$\overline{\text{PCI_INTA}}$	AF7	O	NV _{DD}	—
$\overline{\text{PCI_RESET_OUT}}$	AB11	O	NV _{DD}	—
PCI_AD0	AB20	I/O	NV _{DD}	—
PCI_AD1	AF23	I/O	NV _{DD}	—
PCI_AD2	AF22	I/O	NV _{DD}	—
PCI_AD3	AB19	I/O	NV _{DD}	—
PCI_AD4	AE22	I/O	NV _{DD}	—
PCI_AD5	AF21	I/O	NV _{DD}	—

Table 62. MPC8313E TEPBGAI Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
RXB	R1	I		—
$\overline{\text{RXB}}$	P1	I		—
SD_IMP_CAL_RX	V5	I		200 Ω \pm 10% to GND
SD_REF_CLK	T5	I		—
SD_REF_CLK	T4	I		—
SD_PLL_TPD	T2	O		—
SD_IMP_CAL_TX	N5	I		100 Ω \pm 10% to GND
SDAVDD	R5	I/O		—
SD_PLL_TPA_ANA	R4	O		—
SDAVSS	R3	I/O		—
USB PHY				
USB_DP	P26	I/O		—
USB_DM	N26	I/O		—
USB_VBUS	P24	I/O		—
USB_TPA	L26	I/O		—
USB_RBIAS	M24	I/O		—
USB_PLL_PWR3	M26	I/O		—
USB_PLL_GND	N24	I/O		—
USB_PLL_PWR1	N25	I/O		—
USB_VSSA_BIAS	M25	I/O		—
USB_VDDA_BIAS	M22	I/O		—
USB_VSSA	N22	I/O		—
USB_VDDA	P22	I/O		—
GTM/USB				
USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2/LSRCID0	AD23	I/O	NV _{DD}	—
USBDR_PWRFAULT/GTM1_TGATE1/GTM2_TGATE2/LSRCID1	AE23	I/O	NV _{DD}	—
USBDR_PCTL0/GTM1_TOUT1/LSRCID2	AC22	O	NV _{DD}	—
USBDR_PCTL1/LBC_PM_REF_10/LSRCID3	AB21	O	NV _{DD}	—

24 Revision History

This table summarizes a revision history for this document.

Table 73. Document Revision History

Rev. Number	Date	Substantive Change(s)
4	11/2011	<ul style="list-style-type: none"> • In Table 2, added following notes: <ul style="list-style-type: none"> – Note 3: Min temperature is specified with T_A; Max temperature is specified with T_J – Note 4: All Power rails must be connected and power applied to the MPC8313 even if the IP interfaces are not used. – Note 5: All I/O pins should be interfaced with peripherals operating at same voltage level. – Note 6: This voltage is the input to the filter discussed in Section 22.2, “PLL Power Supply Filtering.” and not necessarily the voltage at the AVDD pin, which may be reduced from VDD by the filter • Decoupled PCI_CLK and SYS_CLK_IN rise and fall times in Table 8. Relaxed maximum rise/fall time of SYS_CLK_IN to 4ns. • Added a note in Table 27 stating “The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm.” • In Table 30: <ul style="list-style-type: none"> – Changed max value of t_{skrgt} in “Data to clock input skew (at receiver)” row from 2.8 to 2.6. – Added Note 7, stating that, “The frequency of RX_CLK should not exceed the GTX_CLK125 by more than 300 ppm.” • Added a note stating “eTSEC should be interfaced with peripheral operating at same voltage level” in Section 8.1.1, “TSEC DC Electrical Characteristics.” • TSEC1_MDC and TSEC_MDIO are powered at 3.3V by NVDD. Replaced LVDDA/LVDDDB with NVDD and removed instances of 2.5V at several places in Section 8.5, “Ethernet Management Interface Electrical Characteristics.” • In Table 43, changed min/max values of t_{CLK_TOL} from 0.05 to 0.005. • In Table 62: <ul style="list-style-type: none"> – Added Note 2 for LGPL4 in showing LGPL4 as open-drain. – Removed Note 2 from TSEC1_MDIO. – Added Note 10: This pin has an internal pull-up. – Added Note 11: This pin has an internal pull-down. – Added Note 12: “In MII mode, GTX_CLK should be pulled down by $300\ \Omega$ to V_{SS}” to TSEC1_GTX_CLK and TSEC2_GTX_CLK. • In Section 19.1, “Package Parameters for the MPC8313E TEPBGAII,” replaced “5.5 Sn/0.5 Cu/4 Ag” with “Sn/3.5 Ag.” • Added foot note 3 in Table 65 stating “The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.” • In Table 72: <ul style="list-style-type: none"> – Added AD = 266 and D = 266. – Added “C = 2.2” in “Revision level” column. – Added Note 4. • Changed resistor from $1.0\ \Omega$ to $10\ \Omega$ in Figure 58. • Replaced LCCR with LCRR throughout. • Added high-speed to USB Phy description.
3	01/2009	<ul style="list-style-type: none"> • Table 72, in column aa, changed to AG = 400 MHz.
2.2	12/2008	<ul style="list-style-type: none"> • Made cross-references active for sections, figures, and tables.
2.1	12/2008	<ul style="list-style-type: none"> • Added Figure 2, after Table 2 and renumbered the following figures.

Table 73. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
2	10/2008	<ul style="list-style-type: none"> • Added Note “The information in this document is accurate for revision 1.0, and 2.x and later. See Section 24.1, “Part Numbers Fully Addressed by this Document,” before Section 1, “Overview.” • Added part numbering details for all the silicon revisions in Table 74. • Changed V_{IH} from 2.7 V to 2.4 V in Table 7. • Added a row for V_{IH} level for Rev 2.x or later in Table 45. • Added a column for maximum power dissipation in low power mode for Rev 2.x or later silicon in Table 6. • Added a column for Power Nos for Rev 2.x or later silicon and added a row for 400 MHz in Table 4. • Removed footnote, “These are preliminary estimates.” from Table 4. • Added Table 21 for DDR AC Specs on Rev 2.x or later silicon. • Added Section 9, “High-Speed Serial Interfaces (HSSI).” • Added \overline{LFW}, \overline{LFCLE}, \overline{LFALE}, \overline{LOE}, \overline{LFRE}, \overline{LFWP}, \overline{LGTA}, $\overline{LUPWAIT}$, and \overline{LFRB} in Table 63. • In Table 39, added note 2: “This parameter is dependent on the <code>csb_clk</code> speed. (The <code>MIIMCFG[Mgmt Clock Select]</code> field determines the clock frequency of the Mgmt Clock <code>EC_MDC</code>.)” • Removed mentions of SGMII (SGMII has separate specs) from Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics.” • Corrected Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics,” to state that RGMII/RTBI interfaces only operate at 2.5 V, not 3.3 V. • Added ZQ package to ordering information In Table 74 and Section 19.1, “Package Parameters for the MPC8313E TEPBGAI1” (applicable to both silicon rev. 1.0 and 2.1) • Removed footnotes 5 and 6 from Table 1 (left over when the PCI undershoot/overshoot voltages and maximum AC waveforms were removed from Section 2.1.2, “Power Supply Voltage Specification”). • Removed <code>SD_PLL_TPD</code> (T2) and <code>SD_PLL_TPA_ANA</code> (R4) from Table 63. • Added Section 8.3, “SGMII Interface Electrical Characteristics.” Removed Section 8.5.3 SGMII DC Electrical Characteristics. • Removed “HRESET negation to SRESET negation (output)” spec and changed “HRESET/SRESET assertion (output)” spec to “HRESET assertion (output)” in Table 10. • Clarified POR configuration signal specs to “Time for the device to turn off POR configuration signal drivers with respect to the assertion of HRESET” and “Time for the device to turn on POR configuration signal drivers with respect to the negation of HRESET” in Table 10. • Added Section 24.2, “Part Marking,” and Figure 62.