### Freescale Semiconductor - MPC8313VRAFFB Datasheet



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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

EXF

Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8313vraffb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



# 1.2 Serial Interfaces

The following interfaces are supported in the MPC8313E: dual UART, dual I<sup>2</sup>C, and an SPI interface.

# 1.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, IEEE Std 802.11i®, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are as follows:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-224, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

# 1.4 DDR Memory Controller

The MPC8313E DDR1/DDR2 memory controller includes the following features:

- Single 16- or 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 333 MHz
- Support for two physical banks (chip selects), each bank independently addressable
- 64-Mbit to 2-Gbit (for DDR1) and to 4-Gbit (for DDR2) devices with x8/x16/x32 data ports (no direct x4 support)
- Support for one 16-bit device or two 8-bit devices on a 16-bit bus, or one 32-bit device or two 16-bit devices on a 32-bit bus
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

# 1.5 PCI Controller

The MPC8313E PCI controller includes the following features:

- PCI specification revision 2.3 compatible
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency



# 1.6 USB Dual-Role Controller

The MPC8313E USB controller includes the following features:

- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Compatible with Universal Serial Bus Specification, Rev. 2.0
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI + low pin interface (ULPI) or on-chip USB 2.0 full-speed/high-speed PHY

# 1.7 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8313E eTSECs include the following features:

- Two RGMII/SGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3®, 802.3u®, 802.3x®, 802.3z®, 802.3au®, and 802.3ab®
- Support for Wake-on-Magic Packet<sup>™</sup>, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status
- Three-speed support (10/100/1000 Mbps)
- On-chip high-speed serial interface to external SGMII PHY interface
- Support for IEEE Std 1588<sup>TM</sup>
- Support for two full-duplex FIFO interface modes
- Multiple PHY interface configuration
- TCP/IP acceleration and QoS features available
- IP v4 and IP v6 header recognition on receive
- IP v4 header checksum verification and generation
- TCP and UDP checksum verification and generation
- Per-packet configurable acceleration
- Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2<sup>®</sup>, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
- Transmission from up to eight physical queues.
- Reception to up to eight physical queues



Driver Type	Output Impedance ( $\Omega$ )	Supply Voltage
DDR2 signal	18	GV <sub>DD</sub> = 1.8 V
DUART, system control, I <sup>2</sup> C, JTAG, SPI	42	NV <sub>DD</sub> = 3.3 V
GPIO signals	42	NV <sub>DD</sub> = 3.3 V
eTSEC signals	42	$LV_{DDA}$ , $LV_{DDB}$ = 2.5/3.3 V
USB signals	42	LV <sub>DDB</sub> = 2.5/3.3 V

Table 3. Output Drive Capability (continued)

# 2.2 Power Sequencing

The MPC8313E does not require the core supply voltage ( $V_{DD}$  and  $V_{DDC}$ ) and I/O supply voltages ( $GV_{DD}$ ,  $LV_{DD}$ , and  $NV_{DD}$ ) to be applied in any particular order. Note that during power ramp-up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there might be a period of time that all input and output pins are actively driven and cause contention and excessive current. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage ( $V_{DD}$  and  $V_{DDC}$ ) before the I/O voltage ( $GV_{DD}$ ,  $LV_{DD}$ , and  $NV_{DD}$ ) and assert PORESET before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V; see Figure 3. Once both the power supplies (I/O voltage and core voltage) are stable, wait for a minimum of 32 clock cycles before negating PORESET.

Note that there is no specific power down sequence requirement for the MPC8313E. I/O voltage supplies  $(GV_{DD}, LV_{DD}, and NV_{DD})$  do not have any ordering requirements with respect to one another.



Figure 3. Power-Up Sequencing Example



# 4.2 AC Electrical Characteristics

The primary clock source for the MPC8313E can be one of two inputs, SYS\_CLK\_IN or PCI\_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the system clock input (SYS\_CLK\_IN/PCI\_CLK) AC timing specifications for the MPC8313E.

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Note
SYS_CLK_IN/PCI_CLK frequency	fsys_clk_in	24	_	66.67	MHz	1
SYS_CLK_IN/PCI_CLK cycle time	<sup>t</sup> SYS_CLK_IN	15	_	_	ns	—
SYS_CLK_IN rise and fall time	t <sub>KH</sub> , t <sub>KL</sub>	0.6	0.8	4	ns	2
PCI_CLK rise and fall time	t <sub>PCH</sub> , t <sub>PCL</sub>	0.6	0.8	1.2	ns	2
SYS_CLK_IN/PCI_CLK duty cycle	t <sub>KHK</sub> /t <sub>SYS_CLK_IN</sub>	40	_	60	%	3
SYS_CLK_IN/PCI_CLK jitter	_	_	_	±150	ps	4, 5

### Table 8. SYS\_CLK\_IN AC Timing Specifications

Notes:

1. Caution: The system, core, security block must not exceed their respective maximum or minimum operating frequencies.

2. Rise and fall times for SYS\_CLK\_IN/PCI\_CLK are measured at 0.4 and 2.4 V.

3. Timing is guaranteed by design and characterization.

4. This represents the total input jitter-short term and long term-and is guaranteed by design.

5. The SYS\_CLK\_IN/PCI\_CLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS\_CLK\_IN drivers with the specified jitter.

# 5 **RESET** Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8313E.

### 5.1 **RESET DC Electrical Characteristics**

This table provides the DC electrical characteristics for the RESET pins.

Table 9. RESET Pins DC Electrical Characteristic
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Characteristic	Symbol	Condition	Min	Мах	Unit
Input high voltage	V <sub>IH</sub>	—	2.1	NV <sub>DD</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	—	-0.3	0.8	V
Input current	I <sub>IN</sub>	$0~V \leq V_{IN} \leq NV_{DD}$	—	±5	μA
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -8.0 mA	2.4	—	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0 mA	—	0.5	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	—	0.4	V



# 6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) when  $GV_{DD}(typ) = 1.8 \text{ V}.$ 

Parameter/Condition	Symbol	Min	Мах	Unit	Note
I/O supply voltage	GV <sub>DD</sub>	1.7	1.9	V	1
I/O reference voltage	MV <sub>REF</sub>	$0.49  imes GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V <sub>TT</sub>	MV <sub>REF</sub> – 0.04	MV <sub>REF</sub> + 0.04	V	3
Input high voltage	V <sub>IH</sub>	MV <sub>REF</sub> + 0.125	GV <sub>DD</sub> + 0.3	V	_
Input low voltage	V <sub>IL</sub>	-0.3	MV <sub>REF</sub> – 0.125	V	_
Output leakage current	I <sub>OZ</sub>	-9.9	9.9	μΑ	4
Output high current (V <sub>OUT</sub> = 1.420 V)	I <sub>OH</sub>	-13.4	—	mA	
Output low current (V <sub>OUT</sub> = 0.280 V)	I <sub>OL</sub>	13.4	_	mA	_

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV<sub>DD</sub>(typ) = 1.8 V

Notes:

1.  $GV_{DD}$  is expected to be within 50 mV of the DRAM  $GV_{DD}$  at all times.

2.  $MV_{REF}$  is expected to be equal to  $0.5 \times GV_{DD}$ , and to track  $GV_{DD}$  DC variations as measured at the receiver. Peak-to-peak noise on  $MV_{REF}$  may not exceed ±2% of the DC value.

3. V<sub>TT</sub> is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV<sub>REF</sub>. This rail should track variations in the DC level of MV<sub>REF</sub>.

4. Output leakage is measured with all outputs disabled, 0 V  $\leq$  V<sub>OUT</sub>  $\leq$  GV<sub>DD</sub>.

This table provides the DDR2 capacitance when  $GV_{DD}(typ) = 1.8$  V.

Table 13.	DDR2 SD	RAM Capa	citance for	GV <sub>DD</sub> (tvp) =	1.8 V
				~ ` ```````````````````````````````````	

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, DQS	CIO	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C <sub>DIO</sub>	_	0.5	pF	1

Note:

1. This parameter is sampled.  $GV_{DD}$  = 1.8 V ± 0.090 V, f = 1 MHz,  $T_A$  = 25°C,  $V_{OUT}$  =  $GV_{DD}/2$ ,  $V_{OUT}$  (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when  $GV_{DD}(typ) = 2.5 \text{ V}.$ 

Table 14. DDR SDRAM DC Electrical Characteristics for GV<sub>DD</sub>(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Note
I/O supply voltage	GV <sub>DD</sub>	2.3	2.7	V	1
I/O reference voltage	MV <sub>REF</sub>	$0.49  imes GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V <sub>TT</sub>	MV <sub>REF</sub> – 0.04	MV <sub>REF</sub> + 0.04	V	3
Input high voltage	V <sub>IH</sub>	MV <sub>REF</sub> + 0.15	GV <sub>DD</sub> + 0.3	V	—
Input low voltage	V <sub>IL</sub>	-0.3	MV <sub>REF</sub> – 0.15	V	—



Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Note
MCK[ <i>n</i> ] cycle time, MCK[ <i>n</i> ]/MCK[ <i>n</i> ] crossing	t <sub>MCK</sub>	6	10	ns	2
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz	t <sub>DDKHAS</sub>	2.1 2.5	_	ns	3
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz	t <sub>DDKHAX</sub>	2.0 2.7	_	ns	3
MCS[ <i>n</i> ] output setup with respect to MCK 333 MHz 266 MHz	t <sub>DDKHCS</sub>	2.1 3.15	_	ns	3
MCS[ <i>n</i> ] output hold with respect to MCK 333 MHz 266 MHz	t <sub>DDKHCX</sub>	2.0 2.7	_	ns	3
MCK to MDQS Skew	t <sub>DDKHMH</sub>	-0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS 333 MHz 266 MHz	<sup>t</sup> DDKHDS, <sup>t</sup> DDKLDS	800 900		ps	5
MDQ//MDM output hold with respect to MDQS 333 MHz 266 MHz	<sup>t</sup> DDKHDX, <sup>t</sup> DDKLDX	750 1000		ps	5
MDQS preamble start	t <sub>DDKHMP</sub>	$-0.5\times t_{MCK}-0.6$	$-0.5 \times t_{\text{MCK}} + 0.6$	ns	6
MDQS epilogue end	t <sub>DDKHME</sub>	-0.6	0.6	ns	6

### Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Silicon Rev 2.x or Later

#### Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t<sub>DDKHAS</sub> symbolizes DDR timing (DD) for the time t<sub>MCK</sub> memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t<sub>DDKLDX</sub> symbolizes DDR timing (DD) for the time t<sub>MCK</sub> memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
  </sub>
- 2. All MCK/MCK referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ//MDM/MDQS.
- 4. Note that t<sub>DDKHMH</sub> follows the symbol conventions described in note 1. For example, t<sub>DDKHMH</sub> describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t<sub>DDKHMH</sub> can be modified through control of the DQSS override bits in the TIMING\_CFG\_2 register. This is typically set to the same delay as the clock adjust in the CLK\_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual, for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t<sub>DDKHMP</sub> follows the symbol conventions described in note 1.



This figure shows the MII transmit AC timing diagram.



Figure 8. MII Transmit AC Timing Diagram

### 8.2.1.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 27. MII Receive AC Timing Specifications

At recommended operating conditions with  $\text{LV}_{\text{DDA}}/\text{LV}_{\text{DDB}}/\text{NV}_{\text{DD}}$  of 3.3 V  $\pm$  0.3 V.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
RX_CLK clock period 10 Mbps	t <sub>MRX</sub>	—	400	—	ns
RX_CLK clock period 100 Mbps	t <sub>MRX</sub>	—	40	—	ns
RX_CLK duty cycle	t <sub>MRXH</sub> /t <sub>MRX</sub>	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t <sub>MRDVKH</sub>	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t <sub>MRDXKH</sub>	10.0	—	—	ns
RX_CLK clock rise V <sub>IL</sub> (min) to V <sub>IH</sub> (max)	t <sub>MRXR</sub>	1.0	—	4.0	ns
RX_CLK clock fall time V <sub>IH</sub> (max) to V <sub>IL</sub> (min)	t <sub>MRXF</sub>	1.0	—	4.0	ns

Note:

- 1. The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>MRDVKH</sub> symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>MRX</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>MRDXKL</sub> symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>MRX</sub> clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t<sub>MRX</sub> represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).</sub>
- 2. The frequency of RX\_CLK should not exceed the TX\_CLK by more than 300 ppm

This figure provides the AC test load for TSEC.



Figure 9. TSEC AC Test Load



### 8.2.1.4 RMII Receive AC Timing Specifications

This table provides the RMII receive AC timing specifications.

### Table 29. RMII Receive AC Timing Specifications

At recommended operating conditions with NV<sub>DD</sub> of 3.3 V  $\pm$  0.3 V.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Мах	Unit
REF_CLK clock period	t <sub>RMX</sub>	_	20	—	ns
REF_CLK duty cycle	t <sub>RMXH</sub> /t <sub>RMX</sub>	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	t <sub>RMRDVKH</sub>	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	t <sub>RMRDXKH</sub>	2.0	—	—	ns
REF_CLK clock rise V <sub>IL</sub> (min) to V <sub>IH</sub> (max)	t <sub>RMXR</sub>	1.0	—	4.0	ns
REF_CLK clock fall time $V_{IH}(max)$ to $V_{IL}(min)$	t <sub>RMXF</sub>	1.0	—	4.0	ns

#### Note:

1. The symbols used for timing specifications follow the pattern of t<sub>(first three letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>RMRDVKH</sub> symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>RMX</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>RMRDXKL</sub> symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>RMX</sub> clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t<sub>RMX</sub> represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).</sub>

This table provides the AC test load.



Figure 12. AC Test Load

This table shows the RMII receive AC timing diagram.



Figure 13. RMII Receive AC Timing Diagram



### 8.2.2 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

### Table 30. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with  $LV_{DDA}/LV_{DDB}$  of 2.5 V ± 5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
Data to clock output skew (at transmitter)	t <sub>SKRGT</sub>	-0.5	_	0.5	ns
Data to clock input skew (at receiver) <sup>2</sup>	<sup>t</sup> skrgt	1.0	_	2.6	ns
Clock cycle duration <sup>3</sup>	t <sub>RGT</sub>	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T <sup>4, 5</sup>	t <sub>RGTH</sub> /t <sub>RGT</sub>	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX <sup>3, 5</sup>	t <sub>RGTH</sub> /t <sub>RGT</sub>	40	50	60	%
Rise time (20%–80%)	t <sub>RGTR</sub>		_	0.75	ns
Fall time (20%–80%)	t <sub>RGTF</sub>	_	_	0.75	ns
GTX_CLK125 reference clock period	t <sub>G12</sub> 6	_	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t <sub>G125H</sub> /t <sub>G125</sub>	47		53	%

Note:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t<sub>RGT</sub> represents the RTBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- 2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
- 3. For 10 and 100 Mbps,  $t_{RGT}$  scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t<sub>RGT</sub> of the lowest speed transitioned between.
- 5. Duty cycle reference is  $LV_{DDA}/2$  or  $LV_{DDB}/2$ .
- 6. This symbol is used to represent the external GTX\_CLK125 and does not follow the original symbol naming convention.
- 7. The frequency of RX\_CLK should not exceed the GTX\_CLK125 by more than 300 ppm



of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

- For external DC-coupled connection, as described in Section 9.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 24 shows the SerDes reference clock input requirement for the DC-coupled connection scheme.
- For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to  $XCOREV_{SS}$ . Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage ( $XCOREV_{SS}$ ). Figure 25 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- Single-ended mode
  - The reference clock can also be single-ended. The SD\_REF\_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-to-peak (from  $V_{min}$  to  $V_{max}$ ) with SD\_REF\_CLK either left unconnected or tied to ground.
  - The SD\_REF\_CLK input average voltage must be between 200 and 400 mV. Figure 26 shows the SerDes reference clock input requirement for the single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC coupled externally. For the best noise performance, the reference of the clock could be DC or AC coupled into the unused phase (SD\_REF\_CLK) through the same source impedance as the clock input (SD\_REF\_CLK) in use.



Figure 24. Differential Reference Clock Input DC Requirements (External DC-Coupled)





Figure 39. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4





# 12 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1<sup>TM</sup> (JTAG) interface.

# 12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE Std 1149.1 (JTAG) interface.

Characteristic	Symbol	Condition	Min	Мах	Unit
Input high voltage	V <sub>IH</sub>	_	2.1	NV <sub>DD</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	_	-0.3	0.8	V
Input current	I <sub>IN</sub>	_	_	±5	μΑ
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -8.0 mA	2.4	—	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0 mA	_	0.5	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	—	0.4	V

Table 46. JTAG Interface DC Electrical Characteristics

# 12.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std 1149.1 (JTAG) interface. This table provides the JTAG AC timing specifications as defined in Figure 41 through Figure 45.

Table 47. JTAG AC Timing Specifications (Independent of SYS\_CLK\_IN)<sup>1</sup>

At recommended operating conditions (see Table 2).

Parameter	Symbol <sup>2</sup>	Min	Мах	Unit	Note
JTAG external clock frequency of operation	f <sub>JTG</sub>	0	33.3	MHz	
JTAG external clock cycle time	t <sub>JTG</sub>	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t <sub>JTKHKL</sub>	15	—	ns	
JTAG external clock rise and fall times	t <sub>JTGR</sub> & t <sub>JTGF</sub>	0	2	ns	
TRST assert time	t <sub>TRST</sub>	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t <sub>JTDVKH</sub> t <sub>JTIVKH</sub>	4 4	_	ns	4
Input hold times: Boundary-scan data TMS, TDI	t <sub>JTDXKH</sub> t <sub>JTIXKH</sub>	10 10		ns	4
Valid times: Boundary-scan data TDO	t <sub>JTKLDV</sub> t <sub>JTKLOV</sub>	2 2	11 11	ns	5
Output hold times: Boundary-scan data TDO	t <sub>JTKLDX</sub> t <sub>JTKLOX</sub>	2 2		ns	5



### Table 49. I<sup>2</sup>C AC Electrical Specifications (continued)

All values refer to  $V_{IH}$  (min) and  $V_{IL}$  (max) levels (see Table 48).

Parameter	Symbol <sup>1</sup>	Min	Max	Unit
Data hold time: CBUS compatible masters I <sup>2</sup> C bus devices	t <sub>I2DXKL</sub>	$\overline{0^2}$		μs
Fall time of both SDA and SCL signals <sup>5</sup>	t <sub>I2CF</sub>	—	300	ns
Setup time for STOP condition	t <sub>I2PVKH</sub>	0.6	_	μs
Bus free time between a STOP and START condition	t <sub>I2KHDX</sub>	1.3	_	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V <sub>NL</sub>	$0.1 \times NV_{DD}$	_	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V <sub>NH</sub>	$0.2 \times \text{NV}_{\text{DD}}$	_	V

#### Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>12DVKH</sub> symbolizes I<sup>2</sup>C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>12C</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>12SXKL</sub> symbolizes I<sup>2</sup>C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t<sub>12C</sub> clock reference (K) going to the bigh (H) state or hold time. Also, t<sub>12PVKH</sub> symbolizes I<sup>2</sup>C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t<sub>12C</sub> clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t<sub>12C</sub> clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
  </sub>
- The MPC8313E provides a hold time of at least 300 ns for the SDA signal (referred to the V<sub>IHmin</sub> of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- 3. The maximum  $t_{12DVKH}$  has only to be met if the device does not stretch the LOW period ( $t_{12CL}$ ) of the SCL signal.
- 4.  $C_B$  = capacitance of one bus line in pF.
- 5. The MPC8313E does not follow the  $l^2C$ -BUS Specifications, Version 2.1, regarding the t<sub>I2CF</sub> AC parameter.

This figure provides the AC test load for the  $I^2C$ .



Figure 46. I<sup>2</sup>C AC Test Load



Parameter	Symbol <sup>1</sup>	Min	Мах	Unit	Note
Clock to output high impedance	t <sub>PCKHOZ</sub>	_	14	ns	2, 3
Input setup to clock	t <sub>PCIVKH</sub>	3.0	—	ns	2, 4
Input hold from clock	t <sub>PCIXKH</sub>	0	—	ns	2, 4

### Table 51. PCI AC Timing Specifications at 66 MHz (continued)

#### Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t<sub>PCIVKH</sub> symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI\_SYNC\_IN clock, t<sub>SYS</sub>, reference (K) going to the high (H) state or setup time. Also, t<sub>PCRHFV</sub> symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
</sub></sub>

2. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.

- 3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.

### This table shows the PCI AC timing specifications at 33 MHz.

### Table 52. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol <sup>1</sup>	Min	Мах	Unit	Note
Clock to output valid	<sup>t</sup> PCKHOV	—	11	ns	2
Output hold from clock	t <sub>PCKHOX</sub>	2	—	ns	2
Clock to output high impedance	t <sub>PCKHOZ</sub>	—	14	ns	2, 3
Input setup to clock	<sup>t</sup> PCIVKH	3.0	—	ns	2, 4
Input hold from clock	t <sub>PCIXKH</sub>	0	—	ns	2, 4

#### Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>PCIVKH</sub> symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI\_SYNC\_IN clock, t<sub>SYS</sub>, reference (K) going to the high (H) state or setup time. Also, t<sub>PCRHFV</sub> symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
</sub>

- 2. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.
- 3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.

This figure provides the AC test load for PCI.



Figure 48. PCI AC Test Load



Signal	Package Pin Number	Power Supply	Note	
V <sub>SS</sub>	B1,B2,B8,B9,B16,B17,C1, C2,C3,C4,C5,C24,C25, C26,D3,D4,D12,D13,D20, D21,F8,F11,F13,F16,F17, F21,G2,G25,H2,H6,H21, H25,L4,L6,L11,L12,L13, L14,L15,L16,L21,L23,M4, M11,M12,M13,M14,M15, M16,M23,N6,N11,N12, N13,N14,N15,N16, N21,N23,P11,P12,P13, P14,P15,P16,P23,P25, R11,R12,R13,R14,R15, R16,R25,T6,T11,T12,T13, T14,T15,T16,T21,T25,U5, U6,U21,W4,W23,Y4,Y23, AA8,AA11,AA13,AA16, AA17,AA21,AC4,AC5, AC12,AC13,AC20,AC21, AD1,AE2,AE8,AE9,AE16, AE17,AF2			
XCOREV <sub>DD</sub>	T1,U2,V2	Core power for SerDes transceivers (1.0 V)	_	_
XCOREV <sub>SS</sub>	P2,R2,T3	—		
XPADV <sub>DD</sub>	P5,U4	Pad power for SerDes transceivers (1.0 V)		
XPADV <sub>SS</sub>	P3,V4		—	

### Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Notes:

- 1. This pin is an open drain signal. A weak pull-up resistor (1 k $\Omega$ ) should be placed on this pin to NV<sub>DD</sub>.
- 2. This pin is an open drain signal. A weak pull-up resistor (2–10 k $\Omega$ ) should be placed on this pin to  $NV_{DD}$ .
- 3. This output is actively driven during reset rather than being three-stated during reset.
- 4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
- 6. This pin must always be tied to V<sub>SS</sub>.
- 7. Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.
- 8. 1588 signals are available on these pins only in MPC8313 Rev 2.x or later.
- 9. LB\_POR\_CFG\_BOOT\_ECC\_DIS is available only in MPC8313 Rev 2.x or later.
- 10. This pin has an internal pull-up.
- 11. This pin has an internal pull-down.
- 12. In MII mode, GTX\_CLK should be pulled down by  $300\Omega$  to V<sub>SS</sub>.



Table 69. Package Thermal Characteristics for TEPBGAII (continued)

Characteristic	Board Type	Symbol	TEPBGA II	Unit	Note
Junction-to-case	—	$R_{ ext{ heta}JC}$	8	°C/W	5
Junction-to-package top	Natural convection	$\Psi_{\text{JT}}$	7	°C/W	6

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

- 3. Per JEDEC JESD51-6 with the board horizontal.
- 4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- 6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

### 21.2 Thermal Management Information

For the following sections,  $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ , where  $P_{I/O}$  is the power dissipation of the I/O drivers.

### 21.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T<sub>J</sub>, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 $T_J$  = junction temperature (°C)  $T_A$  = ambient temperature for the package (°C)  $R_{\theta JA}$  = junction-to-ambient thermal resistance (°C/W)  $P_D$  = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity  $T_I - T_A$ ) are possible.

# 21.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter



 $R_{\theta JC}$  is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance,  $R_{\theta CA}$ . For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Heat Sink Assuming Thermal Grease	Airflow	Thermal Resistance (°C/W)
Wakefield 53 $\times$ 53 $\times$ 2.5 mm pin fin	Natural convection	13.0
	0.5 m/s	10.6
	1 m/s	9.7
	2 m/s	9.2
	4 m/s	8.9
Aavid 35 $\times~$ 31 $\times$ 23 mm pin fin	Natural convection	14.4
	0.5 m/s	11.3
	1 m/s	10.5
	2 m/s	9.9
	4 m/s	9.4
Aavid $30 \times 30 \times 9.4$ mm pin fin	Natural convection	16.5
	0.5 m/s	13.5
	1 m/s	12.1
	2 m/s	10.9
	4 m/s	10.0
Aavid 43 $\times$ 41 $\times$ 16.5 mm pin fin	Natural convection	14.5
	0.5 m/s	11.7
	1 m/s	10.5
	2 m/s	9.7
	4 m/s	9.2

Table 70. Thermal Resistance for TEPBGAII with Heat Sink in Open Flow

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in Table 70. More detailed thermal models can be made available on request.



• Third, between the device and any SerDes voltage regulator there should be a  $10-\mu$ F, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a  $100-\mu$ F, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

# 22.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to  $NV_{DD}$ ,  $GV_{DD}$ ,  $LV_{DD}$ ,  $LV_{DDA}$ , or  $LV_{DDB}$  as required. Unused active high inputs should be connected to  $V_{SS}$ . All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external  $V_{DD}$ ,  $NV_{DD}$ ,  $GV_{DD}$ ,  $LV_{DD}$ ,  $LV_{DDA}$ ,  $LV_{DDB}$ , and  $V_{SS}$  pins of the device.

# 22.6 Output Buffer DC Impedance

The MPC8313E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for  $I^2C$ ).

To measure  $Z_0$  for the single-ended drivers, an external resistor is connected from the chip pad to  $NV_{DD}$  or  $V_{SS}$ . Then, the value of each resistor is varied until the pad voltage is  $NV_{DD}/2$  (see Figure 60). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open), and  $R_p$  is trimmed until the voltage at the pad equals  $NV_{DD}/2$ .  $R_p$  then becomes the resistance of the pull-up devices.  $R_p$  and  $R_N$  are designed to be close to each other in value. Then,  $Z_0 = (R_p + R_N)/2$ .



Figure 60. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is  $V_1 = R_{source} \times I_{source}$ . Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value  $R_{term}$ . The measured voltage is  $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$ . Solving for the output impedance gives  $R_{source} = R_{term} \times (V_1/V_2 - 1)$ . The drive current is then  $I_{source} = V_1/R_{source}$ .



The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert TRST without causing PORESET. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 61 allows the COP to independently assert HRESET or TRST, while ensuring that the target can drive HRESET as well. If the JTAG interface and COP header are not used, TRST should be tied to PORESET so that it is asserted when the system reset signal (PORESET) is asserted.

The COP header shown in Figure 61 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header).

There is no standardized way to number the COP header shown in Figure 61; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 61 is common to all known emulators.



# 23.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the MPC8313E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

MPC	nnnn	е	t	рр	aa	а	X
Product Code	Part Identifier	Encryption Acceleration	Temperature Range <sup>3</sup>	Package <sup>1, 4</sup>	e300 core Frequency <sup>2</sup>	DDR Frequency	Revision Level
MPC	8313	Blank = Not included E = included	Blank = 0° to 105°C C= –40° to 105°C	ZQ = PB TEPBGAII VR = PB free TEPBGAII	AD = 266 MHz AF = 333 MHz AG = 400 MHz	D = 266 MHz F = 333 MHz	Blank = 1.0 A = 2.0 B = 2.1 C = 2.2

### Table 72. Part Numbering Nomenclature

Note:

1. See Section 19, "Package and Pin Listings," for more information on available package types.

- Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
- 3. Contact local Freescale office on availability of parts with °C temperature range.
- 4. ZQ package was available for Rev 1.0. For Rev 2.x, only VR package is available.

### 23.2 Part Marking

Parts are marked as shown in this figure.



Notes:

MPCnnnnetppaar is the orderable part number. ATWLYYWW is the standard assembly, test, year, and work week codes. CCCCC is the country code. MMMMM is the mask number.

Figure 62. Part Marking for TEPBGAII Device