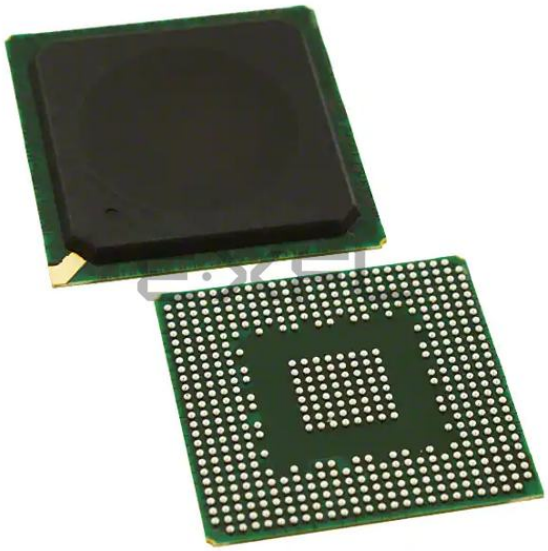

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	267MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8313zqadd

1.6 USB Dual-Role Controller

The MPC8313E USB controller includes the following features:

- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Compatible with *Universal Serial Bus Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI + low pin interface (ULPI) or on-chip USB 2.0 full-speed/high-speed PHY

1.7 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8313E eTSECs include the following features:

- Two RGMII/SGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3®, 802.3u®, 802.3x®, 802.3z®, 802.3au®, and 802.3ab®
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status
- Three-speed support (10/100/1000 Mbps)
- On-chip high-speed serial interface to external SGMII PHY interface
- Support for IEEE Std 1588™
- Support for two full-duplex FIFO interface modes
- Multiple PHY interface configuration
- TCP/IP acceleration and QoS features available
- IP v4 and IP v6 header recognition on receive
- IP v4 header checksum verification and generation
- TCP and UDP checksum verification and generation
- Per-packet configurable acceleration
- Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2®, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
- Transmission from up to eight physical queues.
- Reception to up to eight physical queues

4.2 AC Electrical Characteristics

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the system clock input (SYS_CLK_IN/PCI_CLK) AC timing specifications for the MPC8313E.

Table 8. SYS_CLK_IN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYS_CLK_IN/PCI_CLK frequency	$f_{SYS\_CLK\_IN}$	24	—	66.67	MHz	1
SYS_CLK_IN/PCI_CLK cycle time	$t_{SYS\_CLK\_IN}$	15	—	—	ns	—
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	0.6	0.8	4	ns	2
PCI_CLK rise and fall time	t_{PCH}, t_{PCL}	0.6	0.8	1.2	ns	2
SYS_CLK_IN/PCI_CLK duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3
SYS_CLK_IN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system, core, security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN/PCI_CLK are measured at 0.4 and 2.4 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8313E.

5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins.

Table 9. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications.

Table 10. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock and power applied to SYS_CLK_IN when the device is in PCI host mode	32	—	$t_{SYS\_CLK\_IN}$	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock and power applied to PCI_SYNC_IN when the device is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3] and $\overline{\text{CFG\_CLK\_IN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	$t_{SYS\_CLK\_IN}$	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR configuration signal drivers with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to turn on POR configuration signal drivers with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:
1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the SYS_CLK_IN input, and PCI_SYNC_IN period depends on the value of $\overline{\text{CFG\_CLKIN\_DIV}}$.
2. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. It is only valid when the device is in PCI host mode.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$.

This table provides the PLL lock times.

Table 11. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface. Note that DDR SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Note
Output leakage current	I_{OZ}	–9.9	–9.9	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Note:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 16. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM when GV_{DD}(typ) = 1.8 V.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	—

This table provides the input AC timing specifications for the DDR SDRAM when GV_{DD}(typ) = 2.5 V.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	—

This table provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions. with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ	t_{CISKEW}	—	—	ps	1, 2
333 MHz	—	–750	750	—	—
266 MHz	—	–750	750	—	—

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[*n*] and any corresponding bit that is captured with MDQS[*n*]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

This figure illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

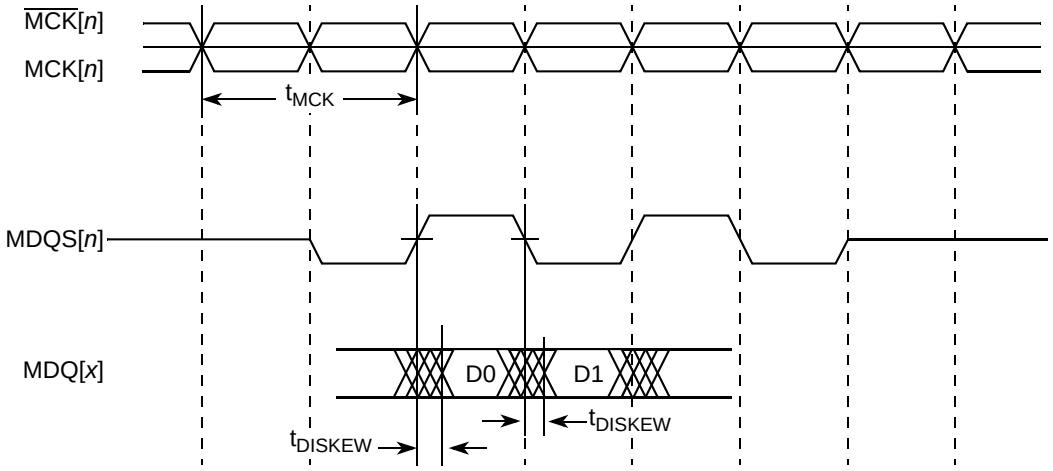

Figure 4. DDR Input Timing Diagram

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications for Rev. 1.0 Silicon

Parameter	Symbol [1]	Min	Max	Unit	Note
MCK[*n*] cycle time, MCK[*n*]/$\overline{\text{MCK}}$[*n*] crossing	t_{MCK}	6	10	ns	2
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz	t_{DDKHAS}	 2.1 2.5	 — —	ns	3
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz	t_{DDKHAX}	 2.4 3.15	 — —	ns	3
$\overline{\text{MCS}}$[*n*] output setup with respect to MCK 333 MHz 266 MHz	t_{DDKHCS}	 2.4 3.15	 — —	ns	3
$\overline{\text{MCS}}$[*n*] output hold with respect to MCK 333 MHz 266 MHz	t_{DDKHCX}	 2.4 3.15	 — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS 333 MHz 266 MHz	t_{DDKHDS}, t_{DDKLDS}	 800 900	 — —	ps	5
MDQ//MDM output hold with respect to MDQS 333 MHz 266 MHz	t_{DDKHDX}, t_{DDKLDX}	 900 1100	 — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

NOTE

For the ADDR/CMD setup and hold specifications in Table 21, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

This figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

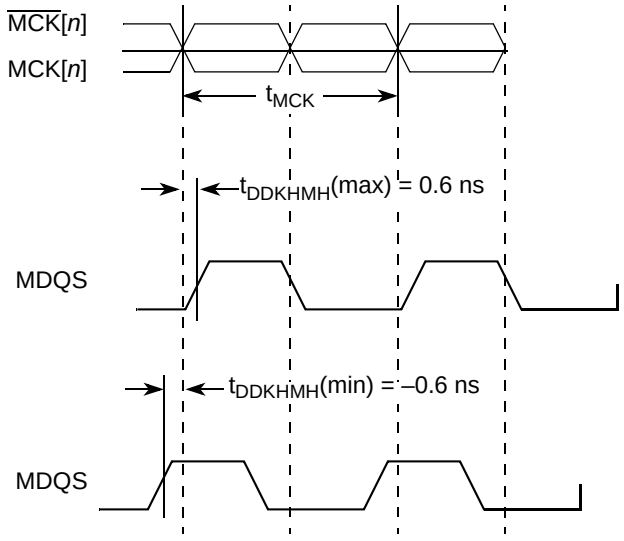

Figure 5. Timing Diagram for t_{DDKHMH}

This figure shows the DDR and DDR2 SDRAM output timing diagram.

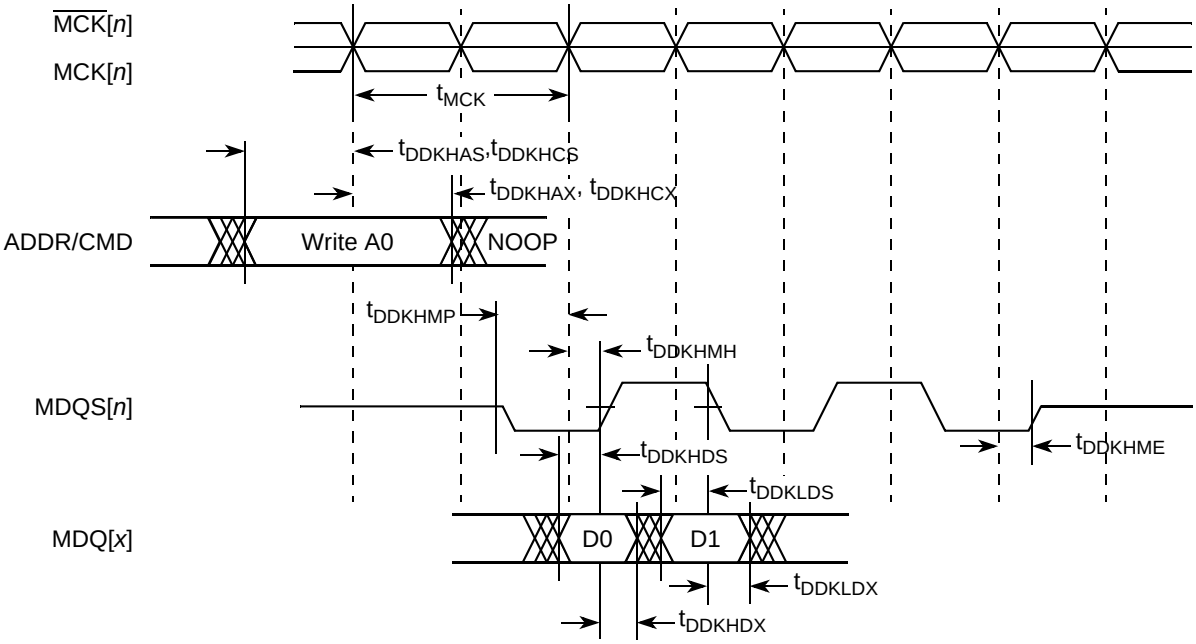

Figure 6. DDR and DDR2 SDRAM Output Timing Diagram

This figure shows the MII receive AC timing diagram.

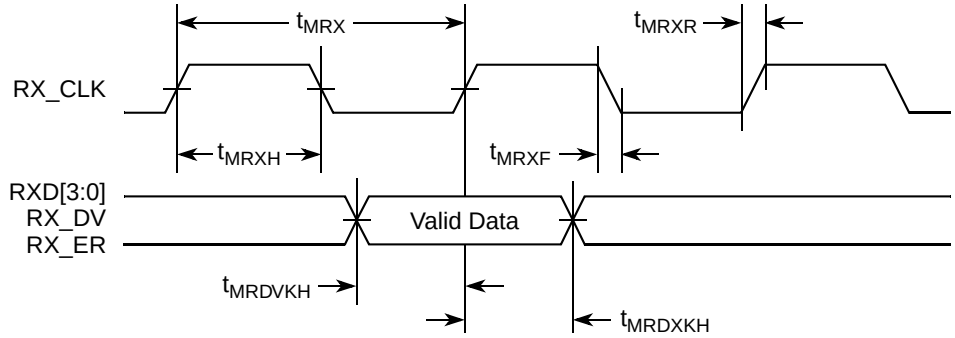

Figure 10. MII Receive AC Timing Diagram RMII AC Timing Specifications

8.2.1.3 RMII Transmit AC Timing Specifications

This table provides the RMII transmit AC timing specifications.

Table 28. RMII Transmit AC Timing Specifications

At recommended operating conditions with NV_{DD} of 3.3 V ± 0.3 V.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	10	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

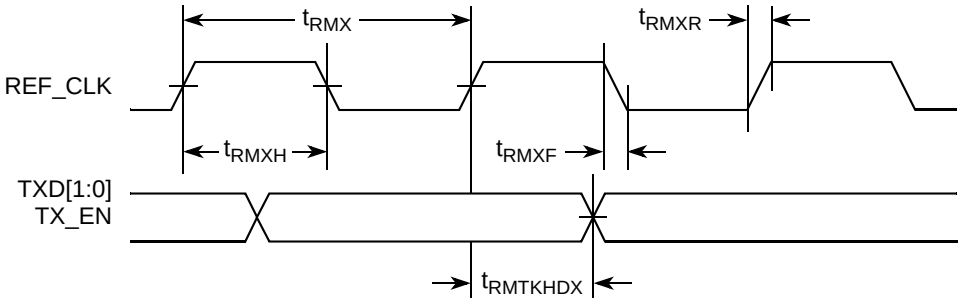

Figure 11. RMII Transmit AC Timing Diagram

— The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 23. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to XCOREV_{SS} followed by on-chip AC coupling.

— The external reference clock driver must be able to drive this termination.

— The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range:
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above XCOREV_{SS}. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  — If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 Ω to XCOREV_{SS} DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement. This requirement is described in detail in the following sections.

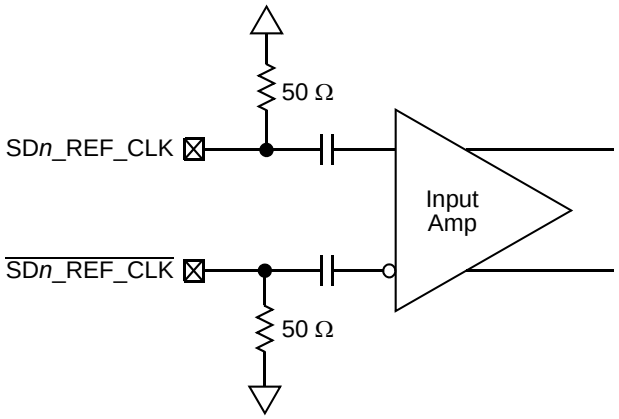

Figure 23. Receiver of SerDes Reference Clocks

9.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8313E SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- Differential mode
  — The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-to-peak (or between 200 and 800 mV differential peak). In other words, each signal wire

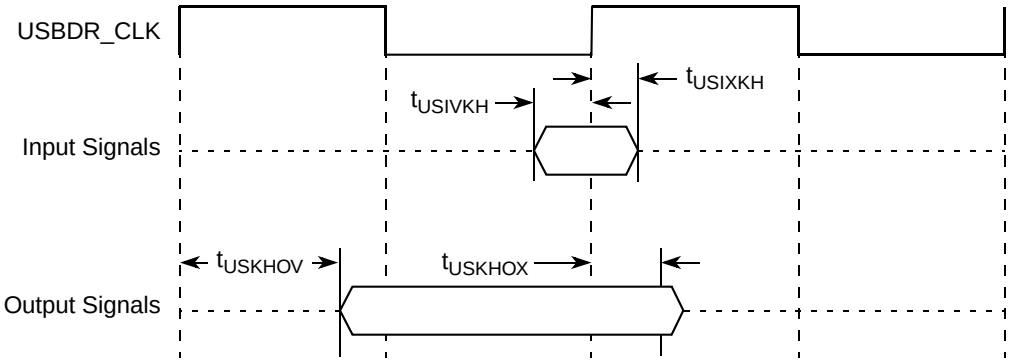

Figure 35. USB Signals

10.2 On-Chip USB PHY

This section describes the DC and AC electrical specifications for the on-chip USB PHY of the MPC8313E. See Chapter 7 in the *USB Specifications Rev. 2*, for more information.

This table provides the USB clock input (USB_CLK_IN) DC timing specifications.

Table 42. USB_CLK_IN DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2.7	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	–0.3	0.4	V

This table provides the USB clock input (USB_CLK_IN) AC timing specifications.

Table 43. USB_CLK_IN AC Timing Specifications

Parameter/Condition	Conditions	Symbol	Min	Typ	Max	Unit
Frequency range	—	$f_{USB\_CLK\_IN}$	—	24	48	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	–0.005	0	0.005	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/time interval error	Peak-to-peak value measured with a second order high-pass filter of 500 kHz bandwidth	t_{CLK_PJ}	—	—	200	ps

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE Std 1149.1 (JTAG) interface.

Table 46. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

12.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std 1149.1 (JTAG) interface. This table provides the JTAG AC timing specifications as defined in Figure 41 through Figure 45.

Table 47. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5

Table 47. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Note
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 34). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

This figure provides the AC test load for TDO and the boundary-scan outputs.

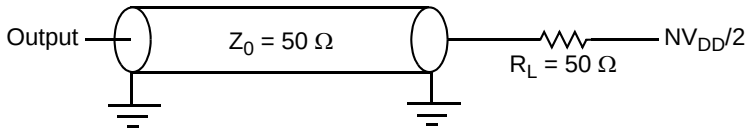

Figure 41. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

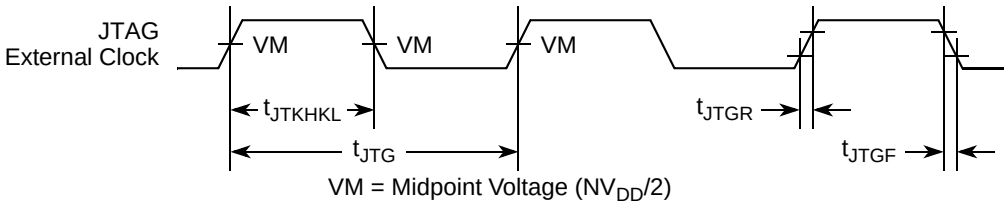

Figure 42. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

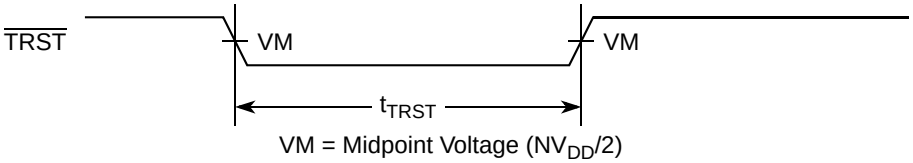

Figure 43. $\overline{\text{TRST}}$ Timing Diagram

Table 51. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol[1]	Min	Max	Unit	Note
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

This table shows the PCI AC timing specifications at 33 MHz.

Table 52. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol[1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

This figure provides the AC test load for PCI.

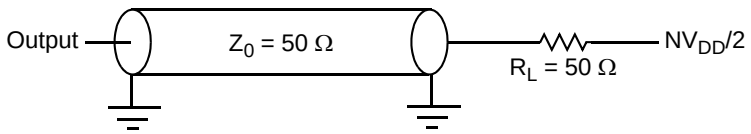

Figure 48. PCI AC Test Load

15.2 Timers AC Timing Specifications

This table provides the Timers input and output AC timing specifications.

Table 54. Timers Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

This figure provides the AC test load for the Timers.

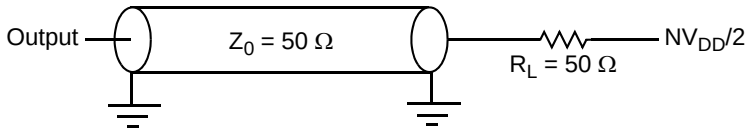

Figure 51. Timers AC Test Load

16 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

16.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO when the GPIO pins are operating from a 3.3-V supply.

Table 55. GPIO (When Operating at 3.3 V) DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	±5	μA

Note:
1. This specification only applies to GPIO pins that are operating from a 3.3-V supply. See Table 62 for the power supply listed for the individual GPIO signal.

17 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

17.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins.

Table 58. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

17.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 59. IPIC Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Note:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLK_IN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

18 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8313E.

18.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the MPC8313E SPI.

Table 60. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Table 60. SPI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le NV_{DD}$	—	±5	μA

18.2 SPI AC Timing Specifications

This table and provide the SPI input and output AC timing specifications.

Table 61. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs—master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—master mode (internal clock) input setup time	t_{NIIVKH}	6	—	ns
SPI inputs—master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Note:

1. Output specifications are measured from the 50% level of the rising edge of SYS_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

This figure provides the AC test load for the SPI.

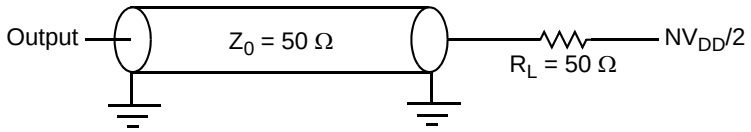

Figure 53. SPI AC Test Load

Figure 54 and Figure 55 represent the AC timing from Table 61. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LA24	E23	O	LV_{DD}	11
LA25	D22	O	LV_{DD}	11
$\overline{\text{LCS0}}$	D23	O	LV_{DD}	10
$\overline{\text{LCS1}}$	J26	O	LV_{DD}	10
$\overline{\text{LCS2}}$	F22	O	LV_{DD}	10
$\overline{\text{LCS3}}$	D26	O	LV_{DD}	10
$\overline{\text{LWE0}}$/$\overline{\text{LFWE}}$	E24	O	LV_{DD}	10
$\overline{\text{LWE1}}$	H26	O	LV_{DD}	10
LBCTL	L22	O	LV_{DD}	10
LALE/M1LALE/M2LALE	E26	O	LV_{DD}	11
LGPL0/LFCLE	AA23	O	LV_{DD}	—
LGPL1/LFALE	AA24	O	LV_{DD}	—
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	AA25	O	LV_{DD}	10
LGPL3/$\overline{\text{LFWP}}$	AA26	O	LV_{DD}	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/$\overline{\text{LFRB}}$	Y22	I/O	LV_{DD}	2
LGPL5	E21	O	LV_{DD}	10
LCLK0	H22	O	LV_{DD}	11
LCLK1	G26	O	LV_{DD}	11
LA0/GPIO0/MSRCID0	AC24	I/O	LV_{DD}	—
LA1/GPIO1//MSRCID1	Y24	I/O	LV_{DD}	—
LA2/GPIO2//MSRCID2	Y26	I/O	LV_{DD}	—
LA3/GPIO3//MSRCID3	W22	I/O	LV_{DD}	—
LA4/GPIO4//MSRCID4	W24	I/O	LV_{DD}	—
LA5/GPIO5/MDVAL	W26	I/O	LV_{DD}	—
LA6/GPIO6	V22	I/O	LV_{DD}	—
LA7/GPIO7/TSEC_1588_TRIG2	V23	I/O	LV_{DD}	8
LA8/GPIO13/TSEC_1588_ALARM1	V24	I/O	LV_{DD}	8
LA9/GPIO14/TSEC_1588_PP3	V25	I/O	LV_{DD}	8
LA10/TSEC_1588_CLK	V26	O	LV_{DD}	8
LA11/TSEC_1588_GCLK	U22	O	LV_{DD}	8
LA12/TSEC_1588_PP1	AD24	O	LV_{DD}	8
LA13/TSEC_1588_PP2	L25	O	LV_{DD}	8

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
SPI				
SPIMOSI/GTM1_TIN3/GTM2_TIN4/GPIO28/LSRCID4	H1	I/O	NV_{DD}	—
SPIMISO/$\overline{\text{GTM1\_TGATE3}}$/$\overline{\text{GTM2\_TGATE4}}$/GPIO29/ LDVAL	H3	I/O	NV_{DD}	—
SPICLK/$\overline{\text{GTM1\_TOUT3}}$/GPIO30	G1	I/O	NV_{DD}	—
SPISEL/GPIO31	G3	I/O	NV_{DD}	—
Power and Ground Supplies				
AV_{DD1}	F14	Power for e300 core APLL (1.0 V)	—	—
AV_{DD2}	P21	Power for system APLL (1.0 V)	—	—
GV_{DD}	A2,A3,A4,A24,A25,B3, B4,B5,B12,B13,B20,B21, B24,B25,B26,D1,D2,D8, D9,D16,D17	Power for DDR1 and DDR2 DRAM I/O voltage (1.8/2.5 V)	—	—
LV_{DD}	D24,D25,G23,H23,R23, T23,W25,Y25,AA22,AC23	Power for local bus (3.3 V)	—	—
LV_{DDA}	W2,Y2	Power for eTSEC2 (2.5 V, 3.3 V)	—	—
LV_{DDB}	AC8,AC9,AE4,AE5	Power for eTSEC1/ USB DR (2.5 V, 3.3 V)	—	—
MV_{REF}	C14,D14	Reference voltage signal for DDR	—	—
NV_{DD}	G4,H4,L2,M2,AC16,AC17, AD25,AD26,AE12,AE13, AE20,AE21,AE24,AE25, AE26,AF24,AF25	Standard I/O voltage (3.3 V)	—	—
V_{DD}	K11,K12,K13,K14,K15, K16,L10,L17,M10,M17, N10,N17,U12,U13,	Power for core (1.0 V)	—	—
V_{DDC}	F6,F10,F19,K6,K10,K17, K21,P6,P10,P17,R10,R17, T10,T17,U10,U11,U14, U15,U16,U17,W6,W21, AA6,AA10,AA14,AA19	Internal core logic constant power (1.0 V)	—	—

The primary clock source for the MPC8313E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICOE*n*] parameters select whether the PCI_SYNC_OUT is driven out on the PCI_CLK_OUT*n* signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the SYS_CLK_IN signal should be tied to VSS.

As shown in Figure 57, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbc_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{\text{PCI\_SYNC\_IN} \times (1 + \sim\overline{\text{CFG\_CLKIN\_DIV}})\} \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~$\overline{\text{CFG\_CLKIN\_DIV}}$) is the SYS_CLK_IN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual*, for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + \text{RCWL[DDRCM]})$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbc_clk* frequency is determined by the following equation:

$$lbc\_clk = csb\_clk \times (1 + \text{RCWL[LBCM]})$$

Note that *lbc_clk* is not the external local bus frequency; *lbc_clk* passes through the a LBC clock divider to create the external local bus clock outputs (LCLK[0:1]). The LBC clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 63 specifies which units have a configurable clock frequency.

20.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in this table should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider. The VCO divider, which is determined by RCWLR[COREPLL], must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

Table 67. e300 Core PLL Configuration

RCWL[COREPLL]			***core_clk* : *csb_clk* Ratio**[1]	**VCO Divider (VCOD)**[3]
0–1	**2–5**	**6**		
nn	**0000**	0	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
11	***nnnn***	n	n/a	n/a
00	**0001**	0	1:1	2
01	**0001**	0	1:1	4
10	**0001**	0	1:1	8
00	**0001**	1	1.5:1	2
01	**0001**	1	1.5:1	4
10	**0001**	1	1.5:1	8
00	**0010**	0	2:1	2
01	**0010**	0	2:1	4
10	**0010**	0	2:1	8
00	**0010**	1	2.5:1	2
01	**0010**	1	2.5:1	4
10	**0010**	1	2.5:1	8
00	**0011**	0	3:1	2
01	**0011**	0	3:1	4
10	**0011**	0	3:1	8

Note:

1. For *core_clk:csb_clk* ratios of 2.5:1 and 3:1, the *core_clk* must not exceed its maximum operating frequency of 333 MHz.
2. Core VCO frequency = core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 400–800 MHz.