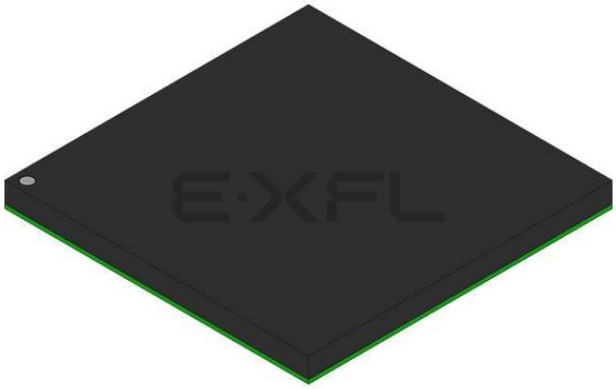

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

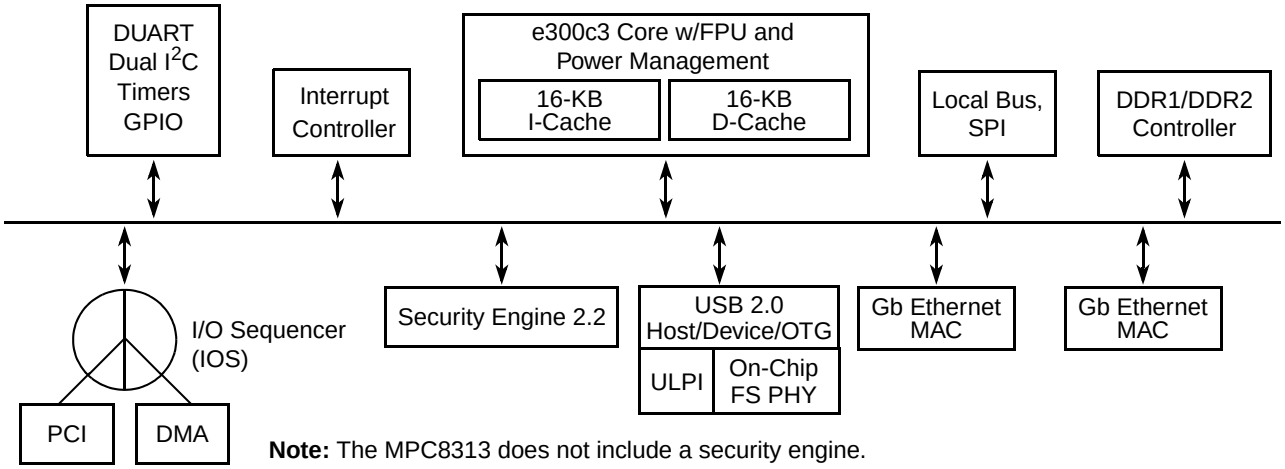
Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	267MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA Exposed Pad
Supplier Device Package	516-TEPBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8313zqaddb

1 Overview

The MPC8313E incorporates the e300c3 core, which includes 16 Kbytes of L1 instruction and data caches and on-chip memory management units (MMUs). The MPC8313E has interfaces to dual enhanced three-speed 10/100/1000 Mbps Ethernet controllers, a DDR1/DDR2 SDRAM memory controller, an enhanced local bus controller, a 32-bit PCI controller, a dedicated security engine, a USB 2.0 dual-role controller and an on-chip high-speed PHY, a programmable interrupt controller, dual I^2C controllers, a 4-channel DMA controller, and a general-purpose I/O port. This figure shows a block diagram of the MPC8313E.



Note: The MPC8313 does not include a security engine.

Figure 1. MPC8313E Block Diagram

The MPC8313E security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

1.1 MPC8313E Features

The following features are supported in the MPC8313E:

- Embedded PowerPC™ e300 processor core built on Power Architecture™ technology; operates at up to 333 MHz.
- High-performance, low-power, and cost-effective host processor
- DDR1/DDR2 memory controller—one 16-/32-bit interface at up to 333 MHz supporting both DDR1 and DDR2
- 16-Kbyte instruction cache and 16-Kbyte data cache, a floating point unit, and two integer units
- Peripheral interfaces such as 32-bit PCI interface with up to 66-MHz operation, 16-bit enhanced local bus interface with up to 66-MHz operation, and USB 2.0 (high speed) with an on-chip PHY.
- Security engine provides acceleration for control and data plane security protocols
- Power management controller for low-power consumption
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Note
Core supply voltage		V_{DD}	–0.3 to 1.26	V	—
PLL supply voltage		AV_{DD}	–0.3 to 1.26	V	—
Core power supply for SerDes transceivers		$XCOREV_{DD}$	–0.3 to 1.26	V	—
Pad power supply for SerDes transceivers		$XPADV_{DD}$	–0.3 to 1.26	V	—
DDR and DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		NV_{DD}/LV_{DD}	–0.3 to 3.6	V	—
eTSEC, USB		LV_{DDA}/LV_{DDB}	–0.3 to 3.6	V	—
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Enhanced three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DDA} + 0.3) or –0.3 to (LV_{DDB} + 0.3)	V	4, 5
	Local bus, DUART, SYS_CLK_IN, system control, and power management, I^2C, and JTAG signals	NV_{IN}	–0.3 to (NV_{DD} + 0.3)	V	3, 5
	PCI	NV_{IN}	–0.3 to (NV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** NV_{IN} must not exceed NV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** LV_{IN} must not exceed LV_{DDA}/LV_{DDB} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the MPC8313E. Note that the values in this table are the recommended and tested operating conditions. If a particular block is given a voltage falling within the range in the Recommended Value column, the MPC8313E is capable of delivering the amount of current listed in the Current Requirement column; this is the maximum current possible. Proper device operation outside of these conditions is not guaranteed.

5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications.

Table 10. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock and power applied to SYS_CLK_IN when the device is in PCI host mode	32	—	$t_{SYS\_CLK\_IN}$	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock and power applied to PCI_SYNC_IN when the device is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:3] and $\overline{\text{CFG\_CLK\_IN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	$t_{SYS\_CLK\_IN}$	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR configuration signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR configuration signal drivers with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to turn on POR configuration signal drivers with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:
1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the SYS_CLK_IN input, and PCI_SYNC_IN period depends on the value of $\overline{\text{CFG\_CLKIN\_DIV}}$.
2. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. It is only valid when the device is in PCI host mode.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:2] and $\overline{\text{CFG\_CLKIN\_DIV}}$.

This table provides the PLL lock times.

Table 11. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface. Note that DDR SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

This table provides the input AC timing specifications for the DDR SDRAM when GV_{DD}(typ) = 2.5 V.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	—

This table provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions. with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ	t_{CISKEW}	—	—	ps	1, 2
333 MHz	—	–750	750	—	—
266 MHz	—	–750	750	—	—

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[*n*] and any corresponding bit that is captured with MDQS[*n*]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

This figure illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

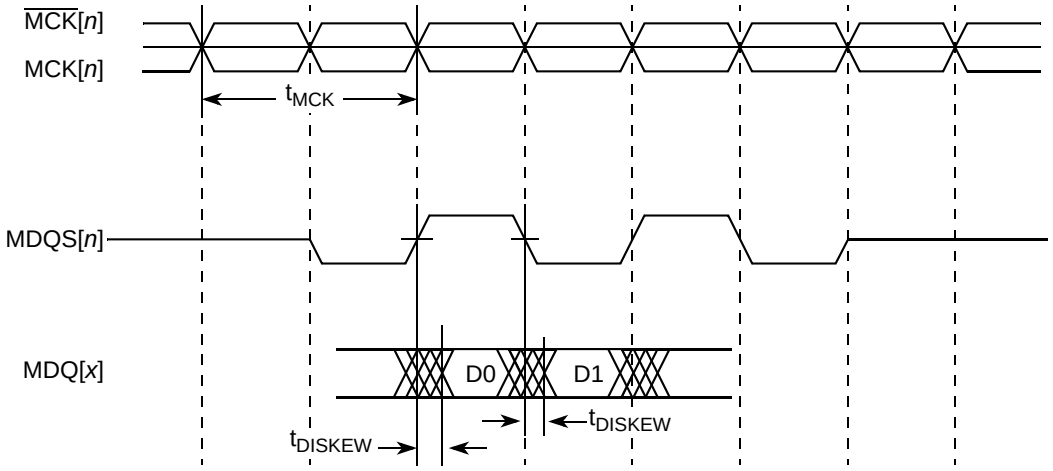


Figure 4. DDR Input Timing Diagram

8.2.1.4 RMII Receive AC Timing Specifications

This table provides the RMII receive AC timing specifications.

Table 29. RMII Receive AC Timing Specifications

At recommended operating conditions with NV_{DD} of 3.3 V ± 0.3 V.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This table provides the AC test load.

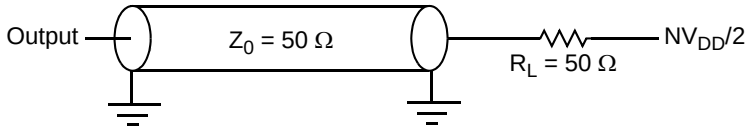


Figure 12. AC Test Load

This table shows the RMII receive AC timing diagram.

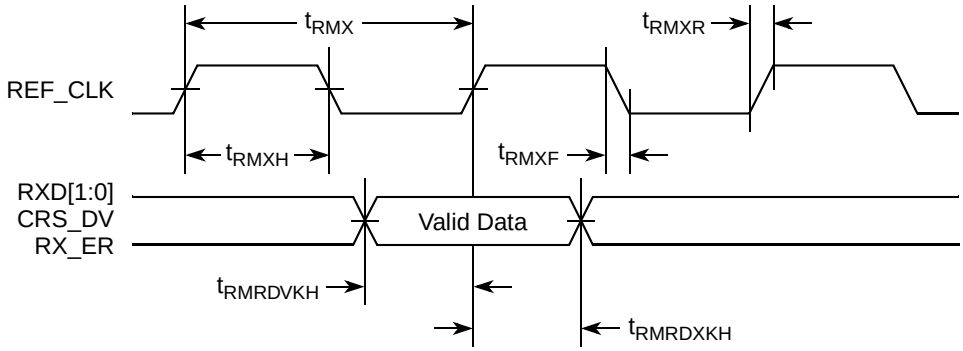


Figure 13. RMII Receive AC Timing Diagram

Table 36. eTSEC IEEE 1588 AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	—	—	ns	2

Notes:
1. T_{RX_CLK} is the max clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for a description of TMR_CTRL registers.
2. It need to be at least two times of clock period of clock selected by TMR_CTRL[CKSEL]. See the *MPC8313E PowerQUICC II Pro Integrated Processor Family Reference Manual,* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 3600, 280, and 56 ns, respectively.

8.5 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for MII, RMII, RGMII, SGMII, and RTBI are specified in Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics."

8.5.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. Table 37 provide the DC electrical characteristics for MDIO and MDC.

Table 37. MII Management DC Electrical Characteristics When Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	NV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	NV_{DD} = Min	2.10	NV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	NV_{DD} = Min	V_{SS}	0.50	V
Input high voltage	V_{IH}	—		2.0	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input high current	I_{IH}	NV_{DD} = Max	V_{IN}[1] = 2.1 V	—	40	μA
Input low current	I_{IL}	NV_{DD} = Max	V_{IN} = 0.5 V	–600	—	μA

— The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 23. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to XCOREV_{SS} followed by on-chip AC coupling.

— The external reference clock driver must be able to drive this termination.

— The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range:
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above XCOREV_{SS}. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  — If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 Ω to XCOREV_{SS} DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement. This requirement is described in detail in the following sections.

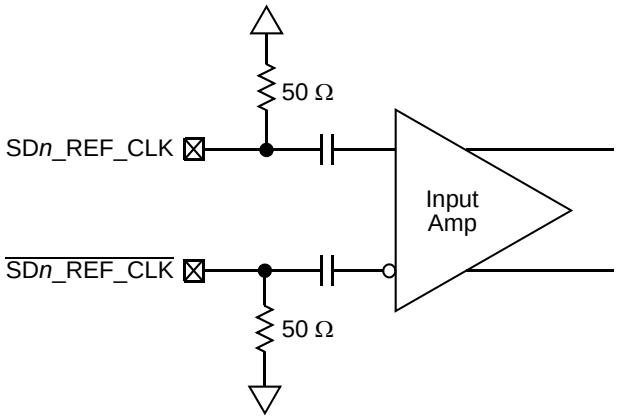


Figure 23. Receiver of SerDes Reference Clocks

9.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8313E SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- Differential mode
  — The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-to-peak (or between 200 and 800 mV differential peak). In other words, each signal wire

of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

— For external DC-coupled connection, as described in Section 9.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 24 shows the SerDes reference clock input requirement for the DC-coupled connection scheme.

— For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to $XCOREV_{SS}$. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage ($XCOREV_{SS}$). Figure 25 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- Single-ended mode

— The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-to-peak (from V_{min} to V_{max}) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.

— The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 26 shows the SerDes reference clock input requirement for the single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC coupled externally. For the best noise performance, the reference of the clock could be DC or AC coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

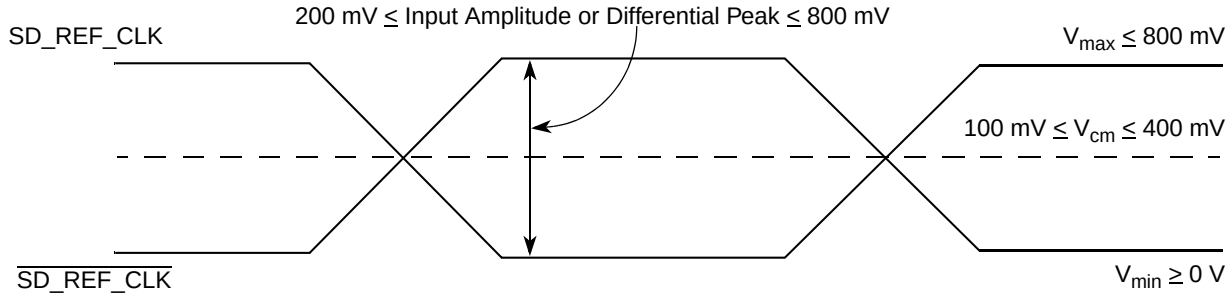


Figure 24. Differential Reference Clock Input DC Requirements (External DC-Coupled)

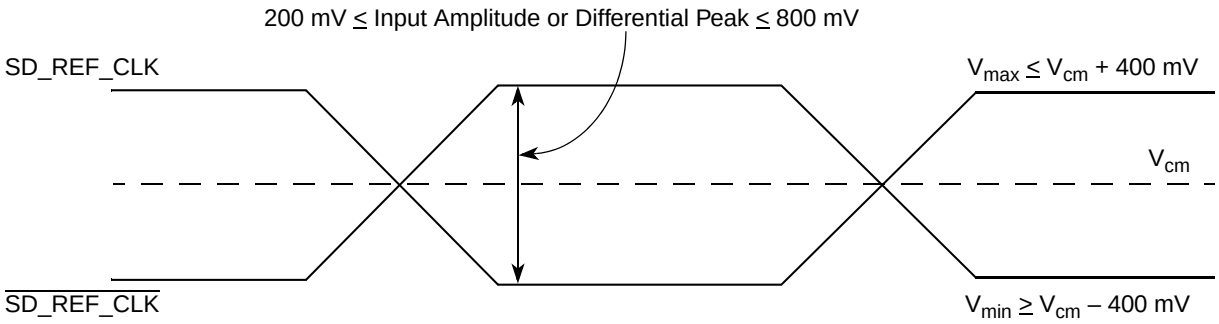


Figure 25. Differential Reference Clock Input DC Requirements (External AC-Coupled)

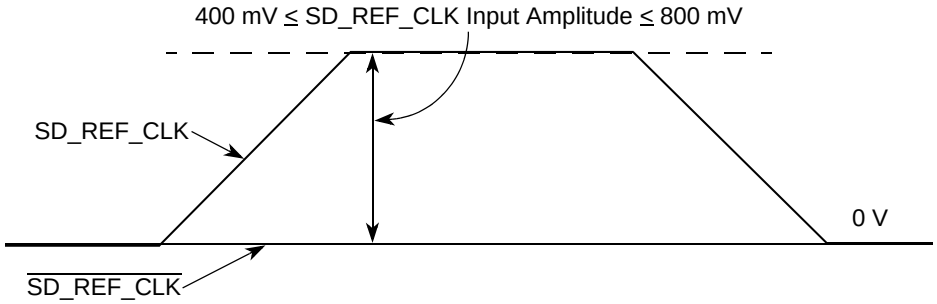


Figure 26. Single-Ended Reference Clock Input DC Requirements

9.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to $XCOREV_{SS}$, the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce a signal with too large of an amplitude and may need to be DC-biased at the clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC coupling.

NOTE

Figure 27 through Figure 30 are for conceptual reference only. Due to the fact that the clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is possible that the clock circuit reference designs provided by clock driver chip vendors are different from what is shown in the figures. They might also vary from one vendor to the other. Therefore, Freescale can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. It is recommended that the system designer contact the selected clock driver chip vendor for the optimal reference circuits for the MPC8313E SerDes reference clock receiver requirement provided in this document.

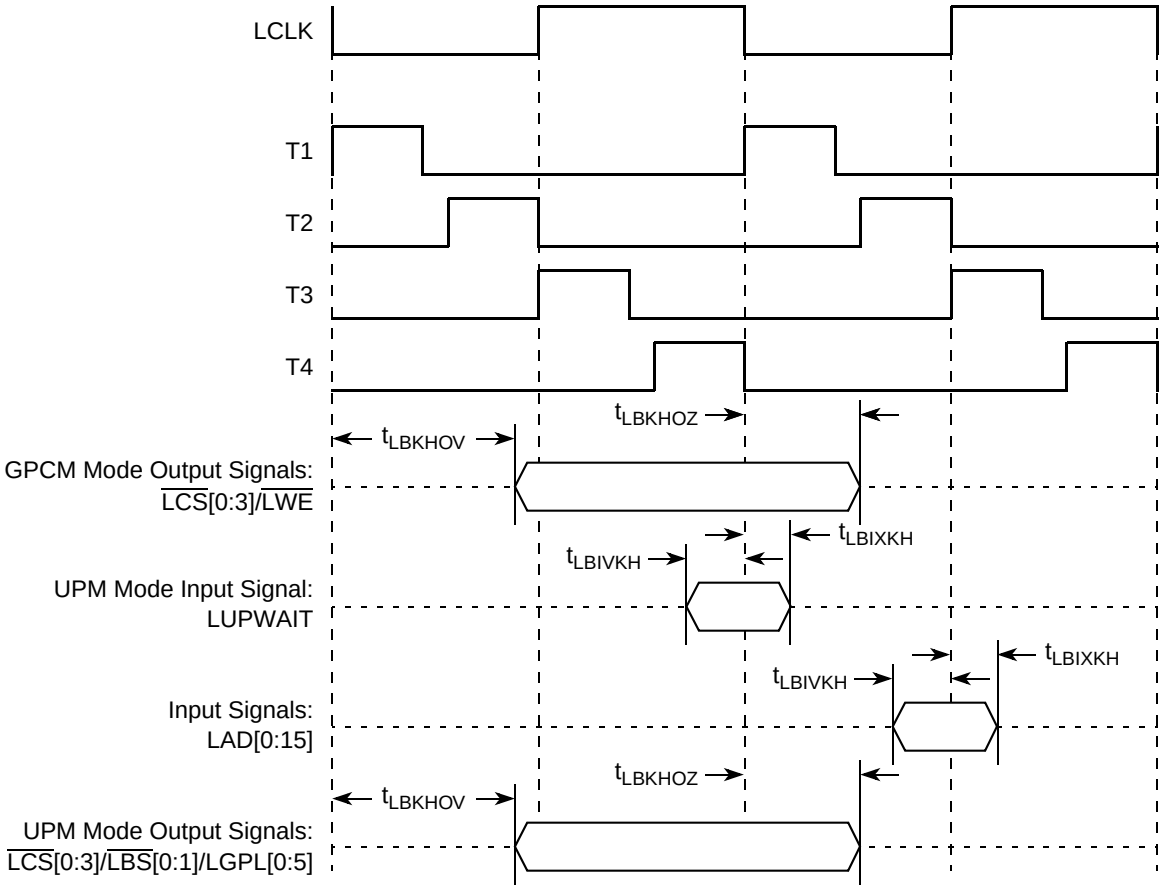


Figure 39. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

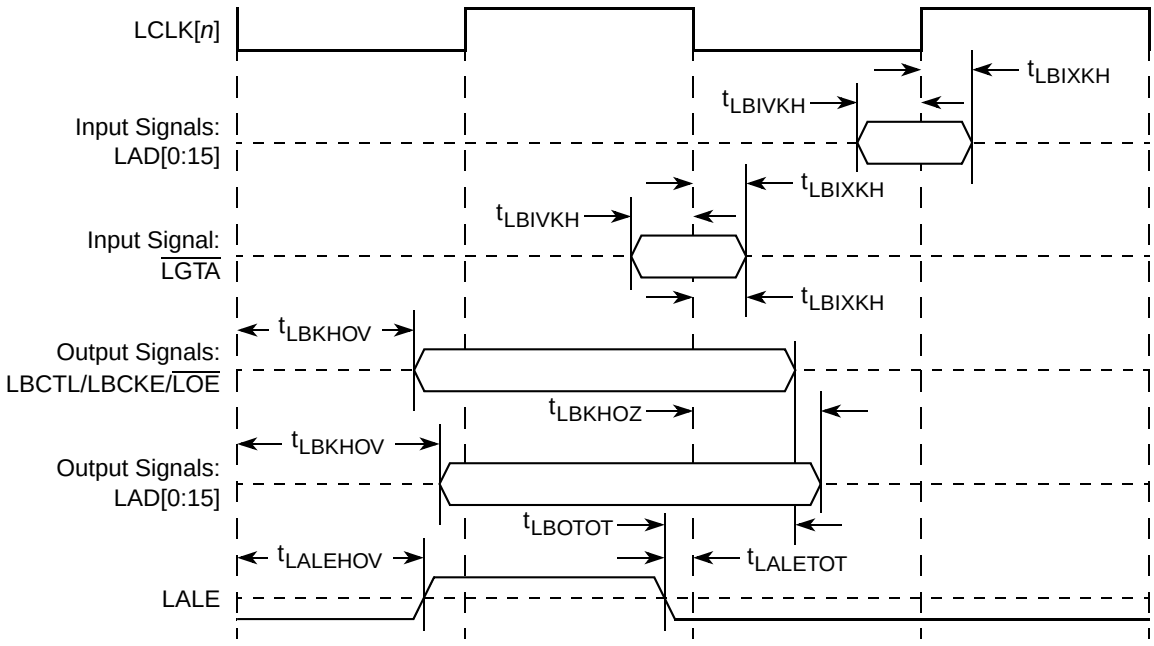


Figure 40. Local Bus Signals, LALE with Respect to LCLK

Table 49. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 48).

Parameter	Symbol[1]	Min	Max	Unit
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0[2]	 — 0.9[3]	µs
Fall time of both SDA and SCL signals[5]	t_{I2CF}	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times NV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times NV_{DD}$	—	V

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The MPC8313E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5. The MPC8313E does not follow the *I²C-BUS Specifications, Version 2.1,* regarding the t_{I2CF} AC parameter.

This figure provides the AC test load for the I²C.

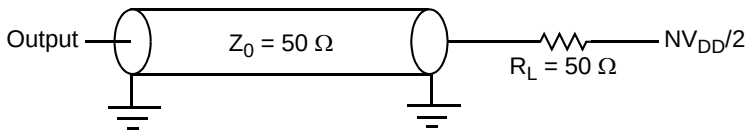


Figure 46. I²C AC Test Load

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MEMC_MDQ29	A20	I/O	GV_{DD}	—
MEMC_MDQ30	C22	I/O	GV_{DD}	—
MEMC_MDQ31	B22	I/O	GV_{DD}	—
MEMC_MDM0	B7	O	GV_{DD}	—
MEMC_MDM1	E6	O	GV_{DD}	—
MEMC_MDM2	E18	O	GV_{DD}	—
MEMC_MDM3	E20	O	GV_{DD}	—
MEMC_MDQS0	A7	I/O	GV_{DD}	—
MEMC_MDQS1	E7	I/O	GV_{DD}	—
MEMC_MDQS2	B19	I/O	GV_{DD}	—
MEMC_MDQS3	A23	I/O	GV_{DD}	—
MEMC_MBA0	D15	O	GV_{DD}	—
MEMC_MBA1	A18	O	GV_{DD}	—
MEMC_MBA2	A15	O	GV_{DD}	—
MEMC_MA0	E12	O	GV_{DD}	—
MEMC_MA1	D11	O	GV_{DD}	—
MEMC_MA2	B11	O	GV_{DD}	—
MEMC_MA3	A11	O	GV_{DD}	—
MEMC_MA4	A12	O	GV_{DD}	—
MEMC_MA5	E13	O	GV_{DD}	—
MEMC_MA6	C12	O	GV_{DD}	—
MEMC_MA7	E14	O	GV_{DD}	—
MEMC_MA8	B15	O	GV_{DD}	—
MEMC_MA9	C17	O	GV_{DD}	—
MEMC_MA10	C13	O	GV_{DD}	—
MEMC_MA11	A16	O	GV_{DD}	—
MEMC_MA12	C15	O	GV_{DD}	—
MEMC_MA13	C16	O	GV_{DD}	—
MEMC_MA14	E15	O	GV_{DD}	—
$\overline{\text{MEMC\_MWE}}$	B18	O	GV_{DD}	—
$\overline{\text{MEMC\_MRAS}}$	C11	O	GV_{DD}	—
$\overline{\text{MEMC\_MCAS}}$	B10	O	GV_{DD}	—

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
$\overline{\text{MEMC\_MCS0}}$	D10	O	GV_{DD}	—
$\overline{\text{MEMC\_MCS1}}$	A10	O	GV_{DD}	—
MEMC_MCKE	B14	O	GV_{DD}	3
MEMC_MCK	A13	O	GV_{DD}	—
$\overline{\text{MEMC\_MCK}}$	A14	O	GV_{DD}	—
MEMC_MODT0	B23	O	GV_{DD}	—
MEMC_MODT1	C23	O	GV_{DD}	—
Local Bus Controller Interface				
LAD0	K25	I/O	LV_{DD}	11
LAD1	K24	I/O	LV_{DD}	11
LAD2	K23	I/O	LV_{DD}	11
LAD3	K22	I/O	LV_{DD}	11
LAD4	J25	I/O	LV_{DD}	11
LAD5	J24	I/O	LV_{DD}	11
LAD6	J23	I/O	LV_{DD}	11
LAD7	J22	I/O	LV_{DD}	11
LAD8	H24	I/O	LV_{DD}	11
LAD9	F26	I/O	LV_{DD}	11
LAD10	G24	I/O	LV_{DD}	11
LAD11	F25	I/O	LV_{DD}	11
LAD12	E25	I/O	LV_{DD}	11
LAD13	F24	I/O	LV_{DD}	11
LAD14	G22	I/O	LV_{DD}	11
LAD15	F23	I/O	LV_{DD}	11
LA16	AC25	O	LV_{DD}	11
LA17	AC26	O	LV_{DD}	11
LA18	AB22	O	LV_{DD}	11
LA19	AB23	O	LV_{DD}	11
LA20	AB24	O	LV_{DD}	11
LA21	AB25	O	LV_{DD}	11
LA22	AB26	O	LV_{DD}	11
LA23	E22	O	LV_{DD}	11

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
RXB	R1	I		—
$\overline{\text{RXB}}$	P1	I		—
SD_IMP_CAL_RX	V5	I		200 Ω ± 10% to GND
$\overline{\text{SD\_REF\_CLK}}$	T5	I		—
SD_REF_CLK	T4	I		—
SD_PLL_TPD	T2	O		—
SD_IMP_CAL_TX	N5	I		100 Ω ± 10% to GND
SDAVDD	R5	I/O		—
SD_PLL_TPA_ANA	R4	O		—
SDAVSS	R3	I/O		—
USB PHY				
USB_DP	P26	I/O		—
USB_DM	N26	I/O		—
USB_VBUS	P24	I/O		—
USB_TPA	L26	I/O		—
USB_RBIAS	M24	I/O		—
USB_PLL_PWR3	M26	I/O		—
USB_PLL_GND	N24	I/O		—
USB_PLL_PWR1	N25	I/O		—
USB_VSSA_BIAS	M25	I/O		—
USB_VDDA_BIAS	M22	I/O		—
USB_VSSA	N22	I/O		—
USB_VDDA	P22	I/O		—
GTM/USB				
USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2/LSRCID0	AD23	I/O	NV_{DD}	—
USBDR_PWRFAULT/$\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$/ LSRCID1	AE23	I/O	NV_{DD}	—
USBDR_PCTL0/$\overline{\text{GTM1\_TOUT1}}$/LSRCID2	AC22	O	NV_{DD}	—
USBDR_PCTL1/LBC_PM_REF_10/LSRCID3	AB21	O	NV_{DD}	—

Table 62. MPC8313E TEPBGAII Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
SPI				
SPIMOSI/GTM1_TIN3/GTM2_TIN4/GPIO28/LSRCID4	H1	I/O	NV_{DD}	—
SPIMISO/$\overline{\text{GTM1\_TGATE3}}$/$\overline{\text{GTM2\_TGATE4}}$/GPIO29/ LDVAL	H3	I/O	NV_{DD}	—
SPICLK/$\overline{\text{GTM1\_TOUT3}}$/GPIO30	G1	I/O	NV_{DD}	—
SPISEL/GPIO31	G3	I/O	NV_{DD}	—
Power and Ground Supplies				
AV_{DD1}	F14	Power for e300 core APLL (1.0 V)	—	—
AV_{DD2}	P21	Power for system APLL (1.0 V)	—	—
GV_{DD}	A2,A3,A4,A24,A25,B3, B4,B5,B12,B13,B20,B21, B24,B25,B26,D1,D2,D8, D9,D16,D17	Power for DDR1 and DDR2 DRAM I/O voltage (1.8/2.5 V)	—	—
LV_{DD}	D24,D25,G23,H23,R23, T23,W25,Y25,AA22,AC23	Power for local bus (3.3 V)	—	—
LV_{DDA}	W2,Y2	Power for eTSEC2 (2.5 V, 3.3 V)	—	—
LV_{DDB}	AC8,AC9,AE4,AE5	Power for eTSEC1/ USB DR (2.5 V, 3.3 V)	—	—
MV_{REF}	C14,D14	Reference voltage signal for DDR	—	—
NV_{DD}	G4,H4,L2,M2,AC16,AC17, AD25,AD26,AE12,AE13, AE20,AE21,AE24,AE25, AE26,AF24,AF25	Standard I/O voltage (3.3 V)	—	—
V_{DD}	K11,K12,K13,K14,K15, K16,L10,L17,M10,M17, N10,N17,U12,U13,	Power for core (1.0 V)	—	—
V_{DDC}	F6,F10,F19,K6,K10,K17, K21,P6,P10,P17,R10,R17, T10,T17,U10,U11,U14, U15,U16,U17,W6,W21, AA6,AA10,AA14,AA19	Internal core logic constant power (1.0 V)	—	—

20.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in this table should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider. The VCO divider, which is determined by RCWLR[COREPLL], must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

Table 67. e300 Core PLL Configuration

RCWL[COREPLL]			***core_clk* : *csb_clk* Ratio**[1]	**VCO Divider (VCOD)**[3]
0–1	**2–5**	**6**		
nn	**0000**	0	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
11	***nnnn***	n	n/a	n/a
00	**0001**	0	1:1	2
01	**0001**	0	1:1	4
10	**0001**	0	1:1	8
00	**0001**	1	1.5:1	2
01	**0001**	1	1.5:1	4
10	**0001**	1	1.5:1	8
00	**0010**	0	2:1	2
01	**0010**	0	2:1	4
10	**0010**	0	2:1	8
00	**0010**	1	2.5:1	2
01	**0010**	1	2.5:1	4
10	**0010**	1	2.5:1	8
00	**0011**	0	3:1	2
01	**0011**	0	3:1	4
10	**0011**	0	3:1	8

Note:

1. For *core_clk:csb_clk* ratios of 2.5:1 and 3:1, the *core_clk* must not exceed its maximum operating frequency of 333 MHz.
2. Core VCO frequency = core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 400–800 MHz.

- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

22.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA}, or LV_{DDB} as required. Unused active high inputs should be connected to V_{SS}. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, NV_{DD}, GV_{DD}, LV_{DD}, LV_{DDA}, LV_{DDB}, and V_{SS} pins of the device.

22.6 Output Buffer DC Impedance

The MPC8313E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to NV_{DD} or V_{SS}. Then, the value of each resistor is varied until the pad voltage is $NV_{DD}/2$ (see Figure 60). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $NV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

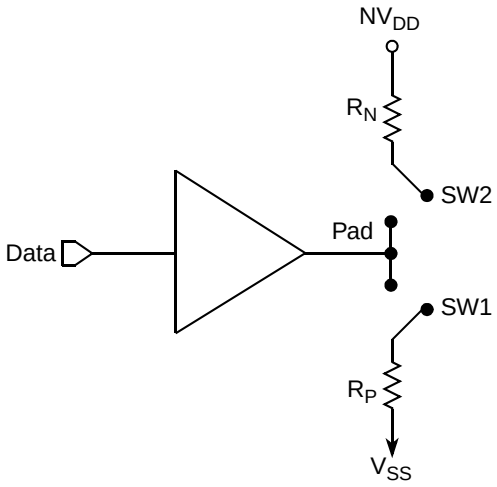


Figure 60. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 73. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
2	10/2008	• Added Note “The information in this document is accurate for revision 1.0, and 2.x and later. See Section 24.1, “Part Numbers Fully Addressed by this Document,” before Section 1, “Overview.” • Added part numbering details for all the silicon revisions in Table 74. • Changed V_{IH} from 2.7 V to 2.4 V in Table 7. • Added a row for V_{IH} level for Rev 2.x or later in Table 45. • Added a column for maximum power dissipation in low power mode for Rev 2.x or later silicon in Table 6. • Added a column for Power Nos for Rev 2.x or later silicon and added a row for 400 MHz in Table 4. • Removed footnote, “These are preliminary estimates.” from Table 4. • Added Table 21 for DDR AC Specs on Rev 2.x or later silicon. • Added Section 9, “High-Speed Serial Interfaces (HSSI).” • Added $\overline{\text{LFWE}}$, LFCLE, LFALE, $\overline{\text{LOE}}$, $\overline{\text{LFRE}}$, $\overline{\text{LFWP}}$, $\overline{\text{LGTA}}$, LUPWAIT, and $\overline{\text{LFRB}}$ in Table 63. • In Table 39, added note 2: “This parameter is dependent on the csb_clk speed. (The MIIMCFG[Mgmt Clock Select] field determines the clock frequency of the Mgmt Clock EC_MDC.)” • Removed mentions of SGMII (SGMII has separate specs) from Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics.” • Corrected Section 8.1, “Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII/RTBI Electrical Characteristics,” to state that RGMII/RTBI interfaces only operate at 2.5 V, not 3.3 V. • Added ZQ package to ordering information In Table 74 and Section 19.1, “Package Parameters for the MPC8313E TEPBGAII” (applicable to both silicon rev. 1.0 and 2.1) • Removed footnotes 5 and 6 from Table 1 (left over when the PCI undershoot/overshoot voltages and maximum AC waveforms were removed from Section 2.1.2, “Power Supply Voltage Specification”). • Removed SD_PLL_TPD (T2) and SD_PLL_TPA_ANA (R4) from Table 63. • Added Section 8.3, “SGMII Interface Electrical Characteristics.” Removed Section 8.5.3 SGMII DC Electrical Characteristics. • Removed “HRESET negation to SRESET negation (output)” spec and changed “HRESET/SRESET assertion (output)” spec to “HRESET assertion (output)” in Table 10. • Clarified POR configuration signal specs to “Time for the device to turn off POR configuration signal drivers with respect to the assertion of HRESET” and “Time for the device to turn on POR configuration signal drivers with respect to the negation of HRESET” in Table 10. • Added Section 24.2, “Part Marking,” and Figure 62.

Table 73. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
1	3/2008	• Replaced OVDD with NV_{DD} everywhere • Added XCOREVDD and XPADVDD to Table 1 • Moved VDD and VDDC to the top of the table before SerDes supplies in Table 2 • In Table 2 split DDR row into two from total current requirement of 425 mA. One for DDR1 (131 mA) and other for DDR2 (140 mA). • In Table 2 corrected current requirement numbers for NV_{DD} from 27 mA to 74 mA, LV_{DD} from 60 mA to 16 mA, LV_{DDA} from 85 mA to 22 mA and LV_{DDB} from 85 mA to 44 mA. • In Table 2 corrected Vdd and Vddc current requirements from 560 mA and 454 mA to 469 and 377 mA, respectively. Corrected Avdd1 and Avdd2 current requirements from 10 mA to 2–3 mA, and XCOREVDD from 100 mA to 170 mA. • In Table 2, added row stating junction temperature range of 0 to 105°C. Added footnote 2 stating GPIO pins may operate from 2.5-V supply as well when configured for different functionality. • In Section 2.1.2, “Power Supply Voltage Specification,” added a note describing the purpose of Table 2. • In Section 3, “Power Characteristics,” added a note describing the purpose of Table 5. • Rewrote Section 2.2, “Power Sequencing,” and added Figure 3. • In Table 4, added “but do include core, USB PLL, and a portion of SerDes digital power...” to Note 1. • In Table 4 corrected “Typical power” to “Maximum power” in note 2 and added a note for Typical Power. • In Table 4 removed 266-MHz row as 266-MHz core parts are not offered. • In Table 5, moved Local bus typical power dissipation under LVdd. • Added Table 6 to show the low power mode power dissipation for D3warm mode. • In Table 8 corrected SYS_CLK_IN frequency range from 25–66 MHz to 24–66.67 MHz. • Added Section 8.4, “eTSEC IEEE 1588 AC Specifications” • In Table 42 changed minimum value of USB input hold t_{USIXKH} from 0 to 1ns • Added Table 43 and Table 44 showing USB clock in specifications • In Table 46, added rows for $t_{LALEHOV}$, $t_{LALETOT1}$, $t_{LALETOT2}$, and $t_{LALETOT3}$ parameters. Added Figure 40. • In Table 50, removed row for rise time (t_{I2CR}). Removed minimum value of t_{I2CF}. Added note 5 stating that the device does not follow the I2C-BUS Specifications version 2.1 regarding the t_{I2CF} AC parameter. • In Table 56, added a note stating: “This specification only applies to GPIO pins that are operating from a 3.3-V supply. See Table 63 for the power supply listed for the individual GPIO signal.” [• Added Table 57 to show DC characteristics for GPIO pins supplied by a 2.5-V supply. Same as eTSEC DC characteristics when operating at 2.5 V. • In Section 20, “Clocking,” corrected the sentence “When the device is configured as a PCI agent device, PCI_SYNC_IN is the primary input clock.” to state “When the device is configured as a PCI agent device, PCI_CLK is the primary input clock.” • Added “Value is decided by RCWLR[COREPLL]” to note 1 of Figure 57 • Added paragraph and Figure 59 to Section 22.2, “PLL Power Supply Filtering.” • Added Section 22.4, “SerDes Block Power Supply Decoupling Recommendations • Removed the two figures on PCI undershoot/overshoot voltages and maximum AC waveforms from Section 2.1.2, “Power Supply Voltage Specification,”

Table 73. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
1	3/2008	• In Table 63, added LBC_PM_REF_10 & LSRCID3 as muxed with USBDR_PCTL1 • In Table 63, added LSRCID2 as muxed with USBDR_PCTL0 • In Table 63, added LSRCID1 as muxed with USBDR_PWRFAULT • In Table 63, added LSRCID0 as muxed with USBDR_DRIVE_VBUS • In Table 63, moved T1, U2,& V2 from V_{DD} to XCOREVDD. • In Table 63, moved P2, R2, & T3 from V_{SS} to XCOREVSS. • In Table 63, moved P5, & U4 from V_{DD} to XPADVDD. • In Table 63, moved P3, & V4 from V_{SS} to XPADVSS. • In Table 63, removed “Double with pad” for AV_{DD1} and AV_{DD2} and moved AV_{DD1} and AV_{DD2} to Power and Ground Supplies section • In Table 63, added impedance control requirements for SD_IMP_CAL_TX (100 ohms to GND) and SD_IMP_CAL_RX (200 ohms to GND). • In Table 63, updated muxing in pinout to show new options for selecting IEEE 1588 functionality. Added footnote 8 • In Table 63, updated muxing in pinout to show new LBC ECC boot enable control muxed with eTSEC1_MDC • Added pin type information for power supplies. • Removed N1 and N3 from Vss section of Table 63. Added Therm0 and Therm1 (N1 and N3, respectively). Added note 7 to state: “Internal thermally sensitive resistor, resistor value varies linearly with temperature. Useful for determining the junction temperature.” • In Table 65 corrected maximum frequency of Local Bus Frequency from “33–66” to 66 MHz • In Table 65 corrected maximum frequency of PCI from “24–66” to 66 MHz • Added “which is determined by RCWLR[COREPLL],” to the note in Section 20.2, “Core PLL Configuration” about the VCO divider. • Added “(VCOD)” next to VCO divider column in Table 68. Added footnote stating that core_clk frequency must not exceed its maximum, so 2.5:1 and 3:1 *core_clk:csb_clk* ratios are invalid for certain *csb_clk* values. • In Table 69, notes were confusing. Added note 3 for VCO column, note 4 for CSB (*csb_clk*) column, note 5 for USB ref column, and note 6 to replace “Note 1”. Clarified note 4 to explain erratum eTSEC40. • In Table 69, updated note 6 to specify USB reference clock frequencies limited to 24 and 48 for rev. 2 silicon. • Replaced Table 71 “Thermal Resistance for TEPBGAII with Heat Sink in Open Flow”. • Removed last row of Table 19. • Removed 200 MHz rows from Table 21 and Table 5. • Changed VIH minimum spec from 2.0 to 2.1 for clock, PIC, JTAG, SPI, and reset pins in Table 9, Table 47, Table 54, Table 59, and Table 61. • Added Figure 4 showing the DDR input timing diagram. • In Table 19, removed “MDM” from the “MDQS-MDQ/MECC/MDM” text under the Parameter column for the tCISKEW parameter. MDM is an output signal and should be removed from the input AC timing spec table (tCISKEW). • Added “and power” to rows 2 and 3 in Table 10 • Added the sentence “Once both the power supplies...” and PORESET to Section 2.2, “Power Sequencing,” and Figure 3. • In Figure 35, corrected “USB0_CLK/USB1_CLK/DR_CLK” with “USBDR_CLK” • In Table 42, clarified that AC specs are for ULPI only.
0	6/2007	Initial release.