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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	10200
Number of Logic Elements/Cells	255000
Total RAM Bits	16672768
Number of I/O	744
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3se260f1152c4n

OCT Calibration Block Specifications

Table 1–34 lists the on-chip termination calibration block specifications for Stratix III devices.

Table 1–34. On-Chip Termination Calibration Block Specification

Symbol	Description	Min	Typical	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
t_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT Rs and Rt calibration	—	1000	—	cycles
$t_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out per OCT calibration block	—	28	—	cycles
t_{RS_RT}	Time required to dynamically switch from Rs to Rt	—	2.5	—	ns

DCD Specifications

Table 1–35 lists the worst case duty cycle distortion for Stratix III devices.

Table 1–35. Duty Cycle Distortion on Stratix III I/O Pins *(Note 1)*

Symbol	C2		C3		C4		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

Note to Table 1–35:

(1) The DCD specification applies to clock outputs from the PLLs, global clock tree, and IOE driving dedicated and general-purpose I/O pins.

I/O Timing

The following sections describe the timing models, preliminary and final timings, I/O timing measurement methodology, I/O default capacitive loading, programmable IOE delay, programmable output buffer delay, user I/O timing, and dedicated clock pin timing.

Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix III device densities and speed grades. This section describes the performance of the Stratix III device I/Os.

All specifications except the fast model are representative of worst-case supply voltage and junction temperature conditions. Fast model specifications are representative of best case process, supply voltage, and junction temperature conditions.

The timing numbers listed in this section are extracted from the Quartus II software version 8.1.

Table 1–47 lists the EP3SL50 column pins output timing parameters for differential I/O standards.

Table 1–47. EP3SL50 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
LVDS_E_1R	—	GCLK	t_{co}	3.029	3.246	4.575	4.976	5.487	5.347	5.565	5.101	5.612	5.474	5.631	ns
		GCLK PLL	t_{co}	3.025	3.249	4.622	5.031	5.549	5.409	5.627	5.160	5.678	5.540	5.697	ns
LVDS_E_3R	—	GCLK	t_{co}	3.029	3.246	4.575	4.976	5.487	5.347	5.565	5.101	5.612	5.474	5.631	ns
		GCLK PLL	t_{co}	3.025	3.249	4.622	5.031	5.549	5.409	5.627	5.160	5.678	5.540	5.697	ns
MINI-LVDS_E_1R	—	GCLK	t_{co}	3.029	3.246	4.575	4.976	5.487	5.347	5.565	5.101	5.612	5.474	5.631	ns
		GCLK PLL	t_{co}	3.025	3.249	4.622	5.031	5.549	5.409	5.627	5.160	5.678	5.540	5.697	ns
MINI-LVDS_E_3R	—	GCLK	t_{co}	3.056	3.279	4.646	5.054	5.571	5.431	5.649	5.181	5.698	5.560	5.717	ns
		GCLK PLL	t_{co}	3.046	3.269	4.636	5.043	5.561	5.421	5.639	5.170	5.688	5.550	5.707	ns
RSDS_E_1R	—	GCLK	t_{co}	3.046	3.269	4.639	5.047	5.565	5.425	5.643	5.175	5.693	5.555	5.712	ns
		GCLK PLL	t_{co}	3.039	3.263	4.632	5.041	5.559	5.419	5.637	5.168	5.687	5.549	5.706	ns
RSDS_E_3R	—	GCLK	t_{co}	3.038	3.261	4.629	5.038	5.556	5.416	5.634	5.165	5.683	5.545	5.702	ns
		GCLK PLL	t_{co}	3.060	3.283	4.650	5.058	5.575	5.435	5.653	5.185	5.703	5.565	5.722	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{co}	3.050	3.272	4.629	5.035	5.550	5.410	5.628	5.161	5.676	5.538	5.695	ns
		GCLK PLL	t_{co}	3.045	3.268	4.629	5.035	5.551	5.411	5.629	5.162	5.678	5.540	5.697	ns
	6mA	GCLK	t_{co}	3.043	3.266	4.628	5.034	5.549	5.409	5.627	5.161	5.677	5.539	5.696	ns
		GCLK PLL	t_{co}	3.035	3.257	4.618	5.024	5.540	5.400	5.618	5.151	5.667	5.529	5.686	ns
	8mA	GCLK	t_{co}	3.036	3.259	4.624	5.031	5.548	5.408	5.626	5.159	5.676	5.538	5.695	ns
		GCLK PLL	t_{co}	3.035	3.256	4.607	5.012	5.526	5.386	5.604	5.138	5.652	5.514	5.671	ns
	10mA	GCLK	t_{co}	3.047	3.269	4.625	5.030	5.544	5.404	5.622	5.157	5.671	5.533	5.690	ns
		GCLK PLL	t_{co}	3.043	3.266	4.626	5.032	5.548	5.408	5.626	5.159	5.675	5.537	5.694	ns
	12mA	GCLK	t_{co}	3.033	3.255	4.615	5.021	5.536	5.396	5.614	5.148	5.663	5.525	5.682	ns
		GCLK PLL	t_{co}	3.031	3.253	4.613	5.018	5.534	5.394	5.612	5.146	5.661	5.523	5.680	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	16mA	GCLK	t_{co}	3.031	3.254	4.616	5.023	5.539	5.399	5.617	5.150	5.667	5.529	5.686	ns
		GCLK PLL	t_{co}	3.035	3.257	4.613	5.018	5.533	5.393	5.611	5.145	5.660	5.522	5.679	ns

Table 1–53 lists the EP3SL70 column pins output timing parameters for single-ended I/O standards.

Table 1–53. EP3SL70 Column Pins Output Timing Parameters (Part 1 of 7)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
3.3-V LVTTL	4mA	GCLK	t_{co}	3.187	3.187	4.411	4.765	5.226	5.105	5.313	4.765	5.226	5.105	5.313	ns
		GCLK PLL	t_{co}	3.514	3.514	4.895	5.293	5.823	5.680	5.963	5.293	5.823	5.680	5.963	ns
	8mA	GCLK	t_{co}	3.120	3.120	4.302	4.654	5.113	4.992	5.200	4.654	5.113	4.992	5.200	ns
		GCLK PLL	t_{co}	3.447	3.447	4.786	5.182	5.710	5.567	5.850	5.182	5.710	5.567	5.850	ns
	12mA	GCLK	t_{co}	3.034	3.034	4.198	4.556	5.021	4.900	5.108	4.556	5.021	4.900	5.108	ns
		GCLK PLL	t_{co}	3.361	3.361	4.682	5.083	5.618	5.475	5.760	5.083	5.618	5.475	5.760	ns
	16mA	GCLK	t_{co}	3.028	3.028	4.182	4.528	4.980	4.859	5.067	4.528	4.980	4.859	5.067	ns
		GCLK PLL	t_{co}	3.354	3.354	4.665	5.055	5.577	5.434	5.718	5.055	5.577	5.434	5.718	ns
3.3-V LVCMOS	4mA	GCLK	t_{co}	3.193	3.193	4.415	4.770	5.233	5.112	5.320	4.770	5.233	5.112	5.320	ns
		GCLK PLL	t_{co}	3.520	3.520	4.899	5.298	5.830	5.687	5.971	5.298	5.830	5.687	5.971	ns
	8mA	GCLK	t_{co}	3.038	3.038	4.209	4.573	5.032	4.911	5.119	4.573	5.032	4.911	5.119	ns
		GCLK PLL	t_{co}	3.365	3.365	4.692	5.100	5.629	5.486	5.770	5.100	5.629	5.486	5.770	ns
	12mA	GCLK	t_{co}	3.045	3.045	4.203	4.552	5.006	4.885	5.093	4.552	5.006	4.885	5.093	ns
		GCLK PLL	t_{co}	3.372	3.372	4.686	5.079	5.603	5.460	5.746	5.079	5.603	5.460	5.746	ns
	16mA	GCLK	t_{co}	3.029	3.029	4.180	4.527	4.977	4.856	5.064	4.527	4.977	4.856	5.064	ns
		GCLK PLL	t_{co}	3.356	3.356	4.664	5.054	5.574	5.431	5.717	5.054	5.574	5.431	5.717	ns
3.0-V LVTTL	4mA	GCLK	t_{co}	3.150	3.150	4.378	4.733	5.193	5.072	5.280	4.733	5.193	5.072	5.280	ns
		GCLK PLL	t_{co}	3.478	3.478	4.862	5.261	5.790	5.647	5.954	5.261	5.790	5.647	5.954	ns
	8mA	GCLK	t_{co}	3.043	3.043	4.250	4.602	5.056	4.936	5.142	4.602	5.056	4.936	5.142	ns
		GCLK PLL	t_{co}	3.367	3.367	4.732	5.127	5.652	5.510	5.837	5.127	5.652	5.510	5.837	ns
	12mA	GCLK	t_{co}	3.005	3.005	4.184	4.530	4.982	4.862	5.068	4.530	4.982	4.862	5.068	ns
		GCLK PLL	t_{co}	3.331	3.331	4.669	5.058	5.578	5.436	5.773	5.058	5.578	5.436	5.773	ns
	16mA	GCLK	t_{co}	2.986	2.986	4.156	4.503	4.953	4.832	5.040	4.503	4.953	4.832	5.040	ns
		GCLK PLL	t_{co}	3.313	3.313	4.640	5.030	5.550	5.407	5.750	5.030	5.550	5.407	5.750	ns

Table 1–57. EP3SL70 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{co}	3.056	3.279	4.646	5.054	5.571	5.431	5.649	5.181	5.698	5.560	5.717	ns
		GCLK PLL	t_{co}	3.046	3.269	4.636	5.043	5.561	5.421	5.639	5.170	5.688	5.550	5.707	ns
	6mA	GCLK	t_{co}	3.046	3.269	4.639	5.047	5.565	5.425	5.643	5.175	5.693	5.555	5.712	ns
		GCLK PLL	t_{co}	3.039	3.263	4.632	5.041	5.559	5.419	5.637	5.168	5.687	5.549	5.706	ns
	8mA	GCLK	t_{co}	3.038	3.261	4.629	5.038	5.556	5.416	5.634	5.165	5.683	5.545	5.702	ns
		GCLK PLL	t_{co}	3.060	3.283	4.650	5.058	5.575	5.435	5.653	5.185	5.703	5.565	5.722	ns
	10mA	GCLK	t_{co}	3.050	3.272	4.629	5.035	5.550	5.410	5.628	5.161	5.676	5.538	5.695	ns
		GCLK PLL	t_{co}	3.045	3.268	4.629	5.035	5.551	5.411	5.629	5.162	5.678	5.540	5.697	ns
	12mA	GCLK	t_{co}	3.043	3.266	4.628	5.034	5.549	5.409	5.627	5.161	5.677	5.539	5.696	ns
		GCLK PLL	t_{co}	3.035	3.257	4.618	5.024	5.540	5.400	5.618	5.151	5.667	5.529	5.686	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	8mA	GCLK	t_{co}	3.036	3.259	4.624	5.031	5.548	5.408	5.626	5.159	5.676	5.538	5.695	ns
		GCLK PLL	t_{co}	3.035	3.256	4.607	5.012	5.526	5.386	5.604	5.138	5.652	5.514	5.671	ns
	16mA	GCLK	t_{co}	3.047	3.269	4.625	5.030	5.544	5.404	5.622	5.157	5.671	5.533	5.690	ns
		GCLK PLL	t_{co}	3.043	3.266	4.626	5.032	5.548	5.408	5.626	5.159	5.675	5.537	5.694	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{co}	3.033	3.255	4.615	5.021	5.536	5.396	5.614	5.148	5.663	5.525	5.682	ns
		GCLK PLL	t_{co}	3.031	3.253	4.613	5.018	5.534	5.394	5.612	5.146	5.661	5.523	5.680	ns
	6mA	GCLK	t_{co}	3.031	3.254	4.616	5.023	5.539	5.399	5.617	5.150	5.667	5.529	5.686	ns
		GCLK PLL	t_{co}	3.035	3.257	4.613	5.018	5.533	5.393	5.611	5.145	5.660	5.522	5.679	ns
	8mA	GCLK	t_{co}	3.061	3.286	4.658	5.066	5.583	5.443	5.661	5.193	5.710	5.572	5.729	ns
		GCLK PLL	t_{co}	3.047	3.272	4.646	5.055	5.573	5.433	5.651	5.183	5.701	5.563	5.720	ns
	10mA	GCLK	t_{co}	3.035	3.259	4.629	5.037	5.555	5.415	5.633	5.165	5.683	5.545	5.702	ns
		GCLK PLL	t_{co}	3.035	3.259	4.632	5.041	5.559	5.419	5.637	5.169	5.688	5.550	5.707	ns
	12mA	GCLK	t_{co}	3.031	3.255	4.625	5.033	5.552	5.412	5.630	5.162	5.680	5.542	5.699	ns
		GCLK PLL	t_{co}	3.035	3.257	4.618	5.024	5.540	5.400	5.618	5.151	5.667	5.529	5.686	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	t_{co}	3.036	3.259	4.626	5.034	5.551	5.411	5.629	5.161	5.679	5.541	5.698	ns
		GCLK PLL	t_{co}	3.064	3.289	4.657	5.064	5.581	5.441	5.659	5.192	5.708	5.570	5.727	ns
	16mA	GCLK	t_{co}	3.053	3.277	4.645	5.052	5.569	5.429	5.647	5.180	5.696	5.558	5.715	ns
		GCLK PLL	t_{co}	3.048	3.273	4.645	5.053	5.570	5.430	5.648	5.181	5.698	5.560	5.717	ns

Table 1–58. EP3SL70 Row Pins Output Timing Parameters (Part 2 of 3)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	t_{co}	3.091	3.326	4.733	5.149	5.676	5.532	5.731	5.284	5.815	5.671	5.800	ns
		GCLK PLL	t_{co}	3.071	3.306	4.710	5.125	5.653	5.509	5.708	5.261	5.791	5.647	5.776	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	t_{co}	3.068	3.302	4.706	5.122	5.649	5.505	5.704	5.257	5.788	5.644	5.773	ns
		GCLK PLL	t_{co}	3.073	3.306	4.697	5.110	5.635	5.491	5.690	5.244	5.772	5.628	5.757	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{co}	3.066	3.299	4.696	5.111	5.638	5.494	5.693	5.247	5.777	5.633	5.762	ns
		GCLK PLL	t_{co}	3.094	3.328	4.724	5.138	5.664	5.520	5.719	5.273	5.802	5.658	5.787	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	t_{co}	3.076	3.311	4.709	5.123	5.649	5.505	5.704	5.258	5.787	5.643	5.772	ns
		GCLK PLL	t_{co}	3.062	3.295	4.686	5.099	5.624	5.480	5.679	5.234	5.762	5.618	5.747	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	t_{co}	2.668	2.842	3.979	4.346	4.821	4.685	4.892	4.453	4.930	4.795	4.940	ns
		GCLK PLL	t_{co}	3.062	3.288	4.646	5.055	5.575	5.431	5.630	5.186	5.709	5.565	5.694	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	t_{co}	3.044	3.278	4.684	5.101	5.629	5.485	5.684	5.237	5.770	5.626	5.755	ns
		GCLK PLL	t_{co}	2.668	2.842	3.979	4.346	4.821	4.685	4.892	4.453	4.930	4.795	4.940	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	t_{co}	3.062	3.288	4.646	5.055	5.575	5.431	5.630	5.186	5.709	5.565	5.694	ns
		GCLK PLL	t_{co}	3.044	3.278	4.684	5.101	5.629	5.485	5.684	5.237	5.770	5.626	5.755	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{co}	2.668	2.842	3.979	4.346	4.821	4.685	4.892	4.453	4.930	4.795	4.940	ns
		GCLK PLL	t_{co}	3.062	3.288	4.646	5.055	5.575	5.431	5.630	5.186	5.709	5.565	5.694	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{co}	3.044	3.278	4.684	5.101	5.629	5.485	5.684	5.237	5.770	5.626	5.755	ns
		GCLK PLL	t_{co}	3.098	3.331	4.730	5.145	5.672	5.528	5.727	5.280	5.809	5.665	5.794	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	6mA	GCLK	t_{co}	3.084	3.317	4.717	5.132	5.659	5.515	5.714	5.266	5.796	5.652	5.781	ns
		GCLK PLL	t_{co}	3.080	3.313	4.715	5.132	5.660	5.516	5.715	5.266	5.798	5.654	5.783	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	8mA	GCLK	t_{co}	3.096	3.328	4.716	5.129	5.654	5.510	5.709	5.263	5.791	5.647	5.776	ns
		GCLK PLL	t_{co}	3.085	3.318	4.712	5.125	5.651	5.507	5.706	5.260	5.788	5.644	5.773	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{co}	3.082	3.315	4.710	5.123	5.649	5.505	5.704	5.258	5.787	5.643	5.772	ns
		GCLK PLL	t_{co}	3.093	3.325	4.711	5.124	5.648	5.504	5.703	5.257	5.785	5.641	5.770	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	6mA	GCLK	t_{co}	3.083	3.316	4.709	5.122	5.647	5.503	5.702	5.257	5.785	5.641	5.770	ns
		GCLK PLL	t_{co}	3.069	3.302	4.694	5.107	5.633	5.489	5.688	5.242	5.770	5.626	5.755	ns

Table 1–67. EP3SL110 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{co}	3.118	3.353	4.737	5.133	5.643	5.504	5.788	5.256	5.765	5.629	5.862	ns
		GCLK PLL	t_{co}	1.326	1.503	1.935	2.032	2.245	2.256	2.283	2.137	2.352	2.362	2.270	ns
	6mA	GCLK	t_{co}	3.114	3.350	4.738	5.135	5.647	5.508	5.792	5.258	5.769	5.633	5.866	ns
		GCLK PLL	t_{co}	1.322	1.500	1.936	2.034	2.249	2.260	2.287	2.139	2.356	2.366	2.274	ns
	8mA	GCLK	t_{co}	3.104	3.339	4.727	5.124	5.635	5.496	5.780	5.247	5.757	5.621	5.854	ns
		GCLK PLL	t_{co}	1.312	1.489	1.925	2.023	2.237	2.248	2.275	2.128	2.344	2.354	2.262	ns
	10mA	GCLK	t_{co}	3.102	3.337	4.725	5.121	5.633	5.494	5.778	5.245	5.755	5.619	5.852	ns
		GCLK PLL	t_{co}	1.310	1.487	1.923	2.020	2.235	2.246	2.273	2.126	2.342	2.352	2.260	ns
	12mA	GCLK	t_{co}	3.102	3.338	4.728	5.126	5.638	5.499	5.783	5.249	5.761	5.625	5.858	ns
		GCLK PLL	t_{co}	1.310	1.488	1.926	2.025	2.240	2.251	2.278	2.130	2.348	2.358	2.266	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{co}	3.106	3.341	4.725	5.121	5.632	5.493	5.777	5.244	5.754	5.618	5.851	ns
		GCLK PLL	t_{co}	1.314	1.491	1.923	2.020	2.234	2.245	2.272	2.125	2.341	2.351	2.259	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{co}	3.132	3.370	4.770	5.169	5.682	5.543	5.827	5.292	5.804	5.668	5.901	ns
		GCLK PLL	t_{co}	1.340	1.520	1.968	2.068	2.284	2.295	2.322	2.173	2.391	2.401	2.309	ns
	6mA	GCLK	t_{co}	3.118	3.356	4.758	5.158	5.672	5.533	5.817	5.282	5.795	5.659	5.892	ns
		GCLK PLL	t_{co}	1.326	1.506	1.956	2.057	2.274	2.285	2.312	2.163	2.382	2.392	2.300	ns
	8mA	GCLK	t_{co}	3.106	3.343	4.741	5.140	5.654	5.515	5.799	5.264	5.777	5.641	5.874	ns
		GCLK PLL	t_{co}	1.314	1.493	1.939	2.039	2.256	2.267	2.294	2.145	2.364	2.374	2.282	ns
	10mA	GCLK	t_{co}	3.106	3.343	4.744	5.144	5.658	5.519	5.803	5.268	5.782	5.646	5.879	ns
		GCLK PLL	t_{co}	1.314	1.493	1.942	2.043	2.260	2.271	2.298	2.149	2.369	2.379	2.287	ns
	12mA	GCLK	t_{co}	3.102	3.339	4.737	5.136	5.651	5.512	5.796	5.261	5.774	5.638	5.871	ns
		GCLK PLL	t_{co}	1.310	1.489	1.935	2.035	2.253	2.264	2.291	2.142	2.361	2.371	2.279	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	8mA	GCLK	t_{co}	3.106	3.341	4.730	5.127	5.639	5.500	5.784	5.250	5.761	5.625	5.858	ns
		GCLK PLL	t_{co}	1.314	1.491	1.928	2.026	2.241	2.252	2.279	2.131	2.348	2.358	2.266	ns
	16mA	GCLK	t_{co}	3.107	3.343	4.738	5.137	5.650	5.511	5.795	5.260	5.773	5.637	5.870	ns
		GCLK PLL	t_{co}	1.315	1.493	1.936	2.036	2.252	2.263	2.290	2.141	2.360	2.370	2.278	ns

Table 1–71. EP3SL150 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
1.8-V HSTL CLASS II	GCLK	t_{su}	-0.917	-0.895	-1.309	-1.453	-1.586	-1.565	-1.896	-1.453	-1.586	-1.565	-1.896	ns
		t_h	1.052	1.026	1.491	1.659	1.813	1.782	2.112	1.659	1.813	1.782	2.112	ns
	GCLK PLL	t_{su}	-1.209	-1.152	-1.678	-1.879	-1.986	-1.910	-2.332	-1.879	-1.986	-1.910	-2.332	ns
		t_h	1.489	1.432	2.082	2.331	2.483	2.384	2.819	2.331	2.483	2.384	2.819	ns
1.5-V HSTL CLASS I	GCLK	t_{su}	-0.917	-0.895	-1.309	-1.453	-1.586	-1.565	-1.896	-1.453	-1.586	-1.565	-1.896	ns
		t_h	1.052	1.026	1.491	1.659	1.813	1.782	2.112	1.659	1.813	1.782	2.112	ns
	GCLK PLL	t_{su}	-1.209	-1.152	-1.678	-1.879	-1.986	-1.910	-2.332	-1.879	-1.986	-1.910	-2.332	ns
		t_h	1.489	1.432	2.082	2.331	2.483	2.384	2.819	2.331	2.483	2.384	2.819	ns
1.5-V HSTL CLASS II	GCLK	t_{su}	-0.906	-0.884	-1.298	-1.442	-1.567	-1.546	-1.877	-1.442	-1.567	-1.546	-1.877	ns
		t_h	1.041	1.015	1.479	1.648	1.794	1.763	2.093	1.648	1.794	1.763	2.093	ns
	GCLK PLL	t_{su}	-1.198	-1.141	-1.667	-1.868	-1.967	-1.891	-2.313	-1.868	-1.967	-1.891	-2.313	ns
		t_h	1.478	1.421	2.070	2.320	2.464	2.365	2.800	2.320	2.464	2.365	2.800	ns
1.2-V HSTL CLASS I	GCLK	t_{su}	-0.906	-0.884	-1.298	-1.442	-1.567	-1.546	-1.877	-1.442	-1.567	-1.546	-1.877	ns
		t_h	1.041	1.015	1.479	1.648	1.794	1.763	2.093	1.648	1.794	1.763	2.093	ns
	GCLK PLL	t_{su}	-1.198	-1.141	-1.667	-1.868	-1.967	-1.891	-2.313	-1.868	-1.967	-1.891	-2.313	ns
		t_h	1.478	1.421	2.070	2.320	2.464	2.365	2.800	2.320	2.464	2.365	2.800	ns
1.2-V HSTL CLASS II	GCLK	t_{su}	-0.894	-0.872	-1.288	-1.431	-1.551	-1.530	-1.861	-1.431	-1.551	-1.530	-1.861	ns
		t_h	1.029	1.003	1.469	1.637	1.778	1.747	2.077	1.637	1.778	1.747	2.077	ns
	GCLK PLL	t_{su}	-1.186	-1.129	-1.657	-1.857	-1.951	-1.875	-2.297	-1.857	-1.951	-1.875	-2.297	ns
		t_h	1.466	1.409	2.060	2.309	2.448	2.349	2.784	2.309	2.448	2.349	2.784	ns
3.0-V PCI	GCLK	t_{su}	-0.894	-0.872	-1.288	-1.431	-1.551	-1.530	-1.861	-1.431	-1.551	-1.530	-1.861	ns
		t_h	1.029	1.003	1.469	1.637	1.778	1.747	2.077	1.637	1.778	1.747	2.077	ns
	GCLK PLL	t_{su}	-1.186	-1.129	-1.657	-1.857	-1.951	-1.875	-2.297	-1.857	-1.951	-1.875	-2.297	ns
		t_h	1.466	1.409	2.060	2.309	2.448	2.349	2.784	2.309	2.448	2.349	2.784	ns
3.0-V PCI-X	GCLK	t_{su}	-0.997	-0.975	-1.401	-1.560	-1.796	-1.777	-2.105	-1.560	-1.796	-1.777	-2.105	ns
		t_h	1.130	1.104	1.583	1.769	2.026	1.995	2.326	1.769	2.026	1.995	2.326	ns
	GCLK PLL	t_{su}	-1.289	-1.232	-1.770	-1.986	-2.196	-2.122	-2.541	-1.986	-2.196	-2.122	-2.541	ns
		t_h	1.567	1.510	2.174	2.441	2.696	2.597	3.033	2.441	2.696	2.597	3.033	ns

Table 1–73. EP3SL150 Column Pins Output Timing Parameters (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
1.5-V HSTL CLASS II	16mA	GCLK	t_{co}	3.250	3.267	4.605	4.969	5.470	5.318	5.653	4.969	5.470	5.318	5.653	ns
		GCLK PLL	t_{co}	3.673	3.669	5.192	5.634	6.186	6.006	6.388	5.634	6.186	6.006	6.388	ns
1.2-V HSTL CLASS I	4mA	GCLK	t_{co}	3.269	3.286	4.641	5.010	5.516	5.364	5.699	5.010	5.516	5.364	5.699	ns
		GCLK PLL	t_{co}	3.692	3.688	5.228	5.675	6.232	6.052	6.434	5.675	6.232	6.052	6.434	ns
	6mA	GCLK	t_{co}	3.261	3.278	4.632	5.001	5.507	5.355	5.690	5.001	5.507	5.355	5.690	ns
		GCLK PLL	t_{co}	3.684	3.680	5.219	5.666	6.223	6.043	6.425	5.666	6.223	6.043	6.425	ns
	8mA	GCLK	t_{co}	3.262	3.279	4.640	5.010	5.516	5.364	5.699	5.010	5.516	5.364	5.699	ns
		GCLK PLL	t_{co}	3.685	3.681	5.227	5.675	6.232	6.052	6.434	5.675	6.232	6.052	6.434	ns
	10mA	GCLK	t_{co}	3.251	3.268	4.627	4.996	5.502	5.350	5.685	4.996	5.502	5.350	5.685	ns
		GCLK PLL	t_{co}	3.674	3.670	5.214	5.661	6.218	6.038	6.420	5.661	6.218	6.038	6.420	ns
	12mA	GCLK	t_{co}	3.251	3.268	4.627	4.996	5.503	5.351	5.686	4.996	5.503	5.351	5.686	ns
		GCLK PLL	t_{co}	3.674	3.670	5.214	5.661	6.219	6.039	6.421	5.661	6.219	6.039	6.421	ns
1.2-V HSTL CLASS II	16mA	GCLK	t_{co}	3.272	3.289	4.643	5.011	5.516	5.364	5.699	5.011	5.516	5.364	5.699	ns
		GCLK PLL	t_{co}	3.695	3.691	5.230	5.676	6.233	6.052	6.434	5.676	6.233	6.052	6.434	ns
3.0-V PCI	—	GCLK	t_{co}	3.375	3.392	4.688	5.045	5.541	5.389	5.724	5.045	5.541	5.389	5.724	ns
		GCLK PLL	t_{co}	3.798	3.794	5.275	5.710	6.264	6.077	6.459	5.710	6.264	6.077	6.459	ns
3.0-V PCI-X	—	GCLK	t_{co}	3.375	3.392	4.688	5.045	5.541	5.389	5.724	5.045	5.541	5.389	5.724	ns
		GCLK PLL	t_{co}	3.798	3.794	5.275	5.710	6.264	6.077	6.459	5.710	6.264	6.077	6.459	ns

Table 1–75 through Table 1–75 list the maximum I/O timing parameters for EP3SL150 devices for differential I/O standards.

Table 1–75 lists the EP3SL150 column pins input timing parameters for differential I/O standards.

Table 1–75. EP3SL150 Column Pins Input Timing Parameters (Part 1 of 2)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
LVDS	GCLK	t_{su}	-0.978	-1.006	-1.151	-1.135	-1.286	-1.233	-1.594	-1.098	-1.339	-1.193	-1.632	ns
		t_h	1.104	1.152	1.371	1.387	1.564	1.502	1.860	1.361	1.634	1.471	1.898	ns
	GCLK PLL	t_{su}	0.967	1.001	1.885	2.230	2.404	2.293	2.197	2.284	2.556	2.353	2.249	ns
		t_h	-0.707	-0.719	-1.450	-1.735	-1.855	-1.769	-1.669	-1.780	-1.984	-1.818	-1.718	ns
MINI-LVDS	GCLK	t_{su}	-0.978	-1.006	-1.151	-1.135	-1.286	-1.233	-1.594	-1.098	-1.339	-1.193	-1.632	ns
		t_h	1.104	1.152	1.371	1.387	1.564	1.502	1.860	1.361	1.634	1.471	1.898	ns
	GCLK PLL	t_{su}	0.967	1.001	1.885	2.230	2.404	2.293	2.197	2.284	2.556	2.353	2.249	ns
		t_h	-0.707	-0.719	-1.450	-1.735	-1.855	-1.769	-1.669	-1.780	-1.984	-1.818	-1.718	ns
RSDS	GCLK	t_{su}	-0.978	-1.006	-1.151	-1.135	-1.286	-1.233	-1.594	-1.098	-1.339	-1.193	-1.632	ns
		t_h	1.104	1.152	1.371	1.387	1.564	1.502	1.860	1.361	1.634	1.471	1.898	ns
	GCLK PLL	t_{su}	0.967	1.001	1.885	2.230	2.404	2.293	2.197	2.284	2.556	2.353	2.249	ns
		t_h	-0.707	-0.719	-1.450	-1.735	-1.855	-1.769	-1.669	-1.780	-1.984	-1.818	-1.718	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	GCLK	t_{su}	-0.794	-0.829	-1.228	-1.334	-1.445	-1.387	-1.743	-1.333	-1.443	-1.391	-1.786	ns
		t_h	0.913	0.967	1.416	1.546	1.677	1.610	1.964	1.554	1.684	1.621	2.007	ns
	GCLK PLL	t_{su}	1.151	1.178	1.808	2.031	2.245	2.139	2.048	2.049	2.266	2.155	2.095	ns
		t_h	-0.898	-0.904	-1.405	-1.576	-1.742	-1.661	-1.565	-1.587	-1.753	-1.668	-1.609	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	GCLK	t_{su}	-0.794	-0.829	-1.228	-1.334	-1.445	-1.387	-1.743	-1.333	-1.443	-1.391	-1.786	ns
		t_h	0.913	0.967	1.416	1.546	1.677	1.610	1.964	1.554	1.684	1.621	2.007	ns
	GCLK PLL	t_{su}	1.151	1.178	1.808	2.031	2.245	2.139	2.048	2.049	2.266	2.155	2.095	ns
		t_h	-0.898	-0.904	-1.405	-1.576	-1.742	-1.661	-1.565	-1.587	-1.753	-1.668	-1.609	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{su}	-0.802	-0.841	-1.238	-1.345	-1.461	-1.403	-1.759	-1.344	-1.458	-1.406	-1.801	ns
		t_h	0.921	0.979	1.426	1.557	1.693	1.626	1.980	1.565	1.699	1.636	2.022	ns
	GCLK PLL	t_{su}	1.143	1.166	1.798	2.020	2.229	2.123	2.032	2.038	2.251	2.140	2.080	ns
		t_h	-0.890	-0.892	-1.395	-1.565	-1.726	-1.645	-1.549	-1.576	-1.738	-1.653	-1.594	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{su}	-0.802	-0.841	-1.238	-1.345	-1.461	-1.403	-1.759	-1.344	-1.458	-1.406	-1.801	ns
		t_h	0.921	0.979	1.426	1.557	1.693	1.626	1.980	1.565	1.699	1.636	2.022	ns
	GCLK PLL	t_{su}	1.143	1.166	1.798	2.020	2.229	2.123	2.032	2.038	2.251	2.140	2.080	ns
		t_h	-0.890	-0.892	-1.395	-1.565	-1.726	-1.645	-1.549	-1.576	-1.738	-1.653	-1.594	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{su}	-0.814	-0.852	-1.247	-1.356	-1.480	-1.422	-1.778	-1.355	-1.476	-1.424	-1.819	ns
		t_h	0.933	0.990	1.436	1.568	1.712	1.645	1.999	1.576	1.717	1.654	2.040	ns
	GCLK PLL	t_{su}	1.131	1.155	1.789	2.009	2.210	2.104	2.013	2.027	2.233	2.122	2.062	ns
		t_h	-0.878	-0.881	-1.385	-1.554	-1.707	-1.626	-1.530	-1.565	-1.720	-1.635	-1.576	ns

Table 1–84 lists the EP3SL200 row pins output timing parameters for single-ended I/O standards.

Table 1–84. EP3SL200 Row Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
3.3-V LVTTL	4mA	GCLK	t_{co}	3.639	3.902	5.663	5.916	6.397	6.238	6.709	6.053	6.634	6.238	6.709	ns
		GCLK PLL	t_{co}	1.551	1.768	2.210	2.317	2.505	2.518	2.444	2.409	2.649	2.518	2.444	ns
	8mA	GCLK	t_{co}	3.548	3.813	5.533	5.778	6.283	6.124	6.565	5.912	6.485	6.124	6.565	ns
		GCLK PLL	t_{co}	1.468	1.663	2.080	2.179	2.361	2.374	2.300	2.268	2.500	2.374	2.300	ns
	12mA	GCLK	t_{co}	3.469	3.724	5.414	5.655	6.187	6.028	6.437	5.785	6.353	6.028	6.437	ns
		GCLK PLL	t_{co}	1.389	1.560	1.961	2.056	2.233	2.246	2.172	2.147	2.368	2.246	2.172	ns
3.3-V LVCMOS	4mA	GCLK	t_{co}	3.649	3.906	5.671	5.921	6.406	6.247	6.714	6.059	6.639	6.247	6.714	ns
		GCLK PLL	t_{co}	1.561	1.772	2.218	2.322	2.510	2.523	2.449	2.415	2.654	2.523	2.449	ns
	8mA	GCLK	t_{co}	3.473	3.728	5.420	5.661	6.197	6.038	6.443	5.794	6.360	6.038	6.443	ns
		GCLK PLL	t_{co}	1.393	1.564	1.967	2.062	2.239	2.252	2.178	2.159	2.375	2.252	2.178	ns
3.0-V LVTTL	4mA	GCLK	t_{co}	3.593	3.848	5.615	5.869	6.363	6.204	6.666	6.010	6.592	6.204	6.666	ns
		GCLK PLL	t_{co}	1.505	1.714	2.162	2.270	2.462	2.475	2.401	2.366	2.607	2.475	2.401	ns
	8mA	GCLK	t_{co}	3.474	3.733	5.463	5.710	6.218	6.059	6.502	5.848	6.428	6.059	6.502	ns
		GCLK PLL	t_{co}	1.394	1.587	2.010	2.111	2.298	2.311	2.237	2.204	2.443	2.311	2.237	ns
	12mA	GCLK	t_{co}	3.437	3.695	5.395	5.627	6.148	5.989	6.414	5.762	6.335	5.989	6.414	ns
		GCLK PLL	t_{co}	1.357	1.536	1.928	2.028	2.210	2.223	2.149	2.118	2.350	2.223	2.149	ns
3.0-V LVCMOS	4mA	GCLK	t_{co}	3.507	3.767	5.510	5.762	6.254	6.095	6.555	5.902	6.481	6.095	6.555	ns
		GCLK PLL	t_{co}	1.419	1.633	2.057	2.163	2.351	2.364	2.290	2.258	2.496	2.364	2.290	ns
	8mA	GCLK	t_{co}	3.424	3.679	5.368	5.588	6.120	5.961	6.375	5.722	6.295	5.961	6.375	ns
		GCLK PLL	t_{co}	1.344	1.515	1.893	1.989	2.171	2.184	2.110	2.087	2.310	2.184	2.110	ns
2.5 V	4mA	GCLK	t_{co}	3.619	3.884	5.748	6.023	6.508	6.349	6.838	6.170	6.771	6.349	6.838	ns
		GCLK PLL	t_{co}	1.531	1.750	2.295	2.424	2.634	2.647	2.573	2.526	2.786	2.647	2.573	ns
	8mA	GCLK	t_{co}	3.516	3.785	5.593	5.860	6.366	6.207	6.668	6.003	6.597	6.207	6.668	ns
		GCLK PLL	t_{co}	1.436	1.651	2.140	2.261	2.464	2.477	2.403	2.359	2.612	2.477	2.403	ns
	12mA	GCLK	t_{co}	3.463	3.735	5.492	5.741	6.275	6.116	6.542	5.880	6.467	6.116	6.542	ns
		GCLK PLL	t_{co}	1.379	1.575	2.029	2.142	2.338	2.351	2.277	2.236	2.482	2.351	2.277	ns

Table 1–92. EP3SL340 Row Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
1.5 V	GCLK	t_{su}	-1.241	-1.332	-1.956	-1.963	-2.136	-2.070	-2.514	-1.972	-2.143	-2.088	-2.556	ns
		t_h	1.367	1.471	2.169	2.184	2.379	2.301	2.749	2.203	2.396	2.328	2.794	ns
	GCLK PLL	t_{su}	0.837	0.921	1.648	1.666	1.925	1.810	1.633	1.651	1.951	1.827	1.684	ns
		t_h	-0.572	-0.635	-1.194	-1.196	-1.398	-1.314	-1.128	-1.171	-1.412	-1.320	-1.172	ns
1.2 V	GCLK	t_{su}	-1.181	-1.279	-1.877	-1.862	-1.977	-1.911	-2.355	-1.876	-1.988	-1.933	-2.401	ns
		t_h	1.307	1.418	2.090	2.083	2.220	2.142	2.590	2.107	2.241	2.173	2.639	ns
	GCLK PLL	t_{su}	0.897	0.974	1.727	1.767	2.084	1.969	1.792	1.747	2.106	1.982	1.839	ns
		t_h	-0.632	-0.688	-1.273	-1.297	-1.557	-1.473	-1.287	-1.267	-1.567	-1.475	-1.327	ns
SSTL-2 CLASS I	GCLK	t_{su}	-1.176	-1.242	-1.845	-1.861	-1.997	-1.933	-2.385	-1.869	-2.002	-1.940	-2.320	ns
		t_h	1.300	1.382	2.057	2.082	2.240	2.164	2.620	2.101	2.254	2.180	2.561	ns
	GCLK PLL	t_{su}	0.942	1.000	1.750	1.782	1.988	1.882	1.891	1.793	2.009	1.897	1.948	ns
		t_h	-0.677	-0.714	-1.296	-1.312	-1.465	-1.390	-1.380	-1.312	-1.475	-1.395	-1.433	ns
SSTL-2 CLASS II	GCLK	t_{su}	-1.176	-1.242	-1.845	-1.861	-1.997	-1.933	-2.385	-1.869	-2.002	-1.940	-2.320	ns
		t_h	1.300	1.382	2.057	2.082	2.240	2.164	2.620	2.101	2.254	2.180	2.561	ns
	GCLK PLL	t_{su}	0.942	1.000	1.750	1.782	1.988	1.882	1.891	1.793	2.009	1.897	1.948	ns
		t_h	-0.677	-0.714	-1.296	-1.312	-1.465	-1.390	-1.380	-1.312	-1.475	-1.395	-1.433	ns
SSTL-18 CLASS I	GCLK	t_{su}	-1.155	-1.244	-1.839	-1.835	-1.972	-1.905	-2.351	-1.844	-1.981	-1.925	-2.394	ns
		t_h	1.281	1.383	2.052	2.054	2.213	2.135	2.582	2.073	2.231	2.164	2.628	ns
	GCLK PLL	t_{su}	0.923	1.009	1.765	1.794	2.086	1.972	1.796	1.779	2.110	1.988	1.846	ns
		t_h	-0.658	-0.723	-1.311	-1.326	-1.562	-1.478	-1.295	-1.301	-1.574	-1.482	-1.338	ns
SSTL-18 CLASS II	GCLK	t_{su}	-1.155	-1.244	-1.839	-1.835	-1.972	-1.905	-2.351	-1.844	-1.981	-1.925	-2.394	ns
		t_h	1.281	1.383	2.052	2.054	2.213	2.135	2.582	2.073	2.231	2.164	2.628	ns
	GCLK PLL	t_{su}	0.923	1.009	1.765	1.794	2.086	1.972	1.796	1.779	2.110	1.988	1.846	ns
		t_h	-0.658	-0.723	-1.311	-1.326	-1.562	-1.478	-1.295	-1.301	-1.574	-1.482	-1.338	ns
SSTL-15 CLASS I	GCLK	t_{su}	-1.141	-1.232	-1.824	-1.825	-1.954	-1.887	-2.333	-1.833	-1.964	-1.908	-2.377	ns
		t_h	1.267	1.371	2.038	2.044	2.195	2.117	2.564	2.062	2.214	2.147	2.611	ns
	GCLK PLL	t_{su}	0.937	1.021	1.778	1.804	2.104	1.990	1.814	1.790	2.127	2.005	1.863	ns
		t_h	-0.672	-0.735	-1.323	-1.336	-1.580	-1.496	-1.313	-1.312	-1.591	-1.499	-1.355	ns
1.8-V HSTL CLASS I	GCLK	t_{su}	-1.155	-1.244	-1.839	-1.835	-1.972	-1.905	-2.351	-1.844	-1.981	-1.925	-2.394	ns
		t_h	1.281	1.383	2.052	2.054	2.213	2.135	2.582	2.073	2.231	2.164	2.628	ns
	GCLK PLL	t_{su}	0.923	1.009	1.765	1.794	2.086	1.972	1.796	1.779	2.110	1.988	1.846	ns
		t_h	-0.658	-0.723	-1.311	-1.326	-1.562	-1.478	-1.295	-1.301	-1.574	-1.482	-1.338	ns
1.8-V HSTL CLASS II	GCLK	t_{su}	-1.155	-1.244	-1.839	-1.835	-1.972	-1.905	-2.351	-1.844	-1.981	-1.925	-2.394	ns
		t_h	1.281	1.383	2.052	2.054	2.213	2.135	2.582	2.073	2.231	2.164	2.628	ns
	GCLK PLL	t_{su}	0.923	1.009	1.765	1.794	2.086	1.972	1.796	1.779	2.110	1.988	1.846	ns
		t_h	-0.658	-0.723	-1.311	-1.326	-1.562	-1.478	-1.295	-1.301	-1.574	-1.482	-1.338	ns

Table 1–113. EP3SE80 Column Pins Output Timing Parameters (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
1.8 V	2mA	GCLK	t_{co}	3.822	3.822	5.464	5.917	6.154	6.369	6.381	5.917	6.154	6.369	6.381	ns
		GCLK PLL	t_{co}	4.050	4.056	5.793	6.281	6.912	6.726	7.147	6.281	6.912	6.726	7.147	ns
	4mA	GCLK	t_{co}	3.581	3.581	5.104	5.511	5.807	5.909	6.032	5.511	5.807	5.909	6.032	ns
		GCLK PLL	t_{co}	3.869	3.875	5.514	5.972	6.564	6.380	6.798	5.972	6.564	6.380	6.798	ns
	6mA	GCLK	t_{co}	3.463	3.463	4.914	5.321	5.696	5.734	5.923	5.321	5.696	5.734	5.923	ns
		GCLK PLL	t_{co}	3.787	3.793	5.407	5.857	6.454	6.268	6.689	5.857	6.454	6.268	6.689	ns
	8mA	GCLK	t_{co}	3.409	3.409	4.814	5.223	5.630	5.622	5.857	5.223	5.630	5.622	5.857	ns
		GCLK PLL	t_{co}	3.767	3.773	5.349	5.803	6.388	6.202	6.623	5.803	6.388	6.202	6.623	ns
	10mA	GCLK	t_{co}	3.341	3.341	4.718	5.125	5.549	5.508	5.776	5.125	5.549	5.508	5.776	ns
		GCLK PLL	t_{co}	3.704	3.710	5.288	5.728	6.307	6.121	6.542	5.728	6.307	6.121	6.542	ns
	12mA	GCLK	t_{co}	3.317	3.317	4.685	5.078	5.526	5.470	5.753	5.078	5.526	5.470	5.753	ns
		GCLK PLL	t_{co}	3.686	3.692	5.267	5.707	6.284	6.098	6.519	5.707	6.284	6.098	6.519	ns
1.5 V	2mA	GCLK	t_{co}	3.730	3.730	5.357	5.827	6.092	6.286	6.319	5.827	6.092	6.286	6.319	ns
		GCLK PLL	t_{co}	3.996	4.002	5.722	6.213	6.850	6.664	7.085	6.213	6.850	6.664	7.085	ns
	4mA	GCLK	t_{co}	3.447	3.447	4.903	5.314	5.700	5.730	5.927	5.314	5.700	5.730	5.927	ns
		GCLK PLL	t_{co}	3.784	3.790	5.403	5.857	6.458	6.272	6.693	5.857	6.458	6.272	6.693	ns
	6mA	GCLK	t_{co}	3.369	3.369	4.803	5.206	5.633	5.613	5.860	5.206	5.633	5.613	5.860	ns
		GCLK PLL	t_{co}	3.759	3.765	5.336	5.797	6.391	6.205	6.626	5.797	6.391	6.205	6.626	ns
	8mA	GCLK	t_{co}	3.359	3.359	4.785	5.185	5.613	5.581	5.840	5.185	5.613	5.581	5.840	ns
		GCLK PLL	t_{co}	3.748	3.754	5.319	5.772	6.371	6.185	6.606	5.772	6.371	6.185	6.606	ns
	10mA	GCLK	t_{co}	3.329	3.329	4.701	5.107	5.543	5.499	5.770	5.107	5.543	5.499	5.770	ns
		GCLK PLL	t_{co}	3.693	3.699	5.281	5.721	6.301	6.115	6.536	5.721	6.301	6.115	6.536	ns
	12mA	GCLK	t_{co}	3.280	3.280	4.679	5.072	5.532	5.457	5.759	5.072	5.532	5.457	5.759	ns
		GCLK PLL	t_{co}	3.688	3.694	5.264	5.710	6.290	6.104	6.525	5.710	6.290	6.104	6.525	ns

Table 1–118 lists the EP3SE80 row pins output timing parameters for differential I/O standards.

Table 1–118. EP3SE80 Row Pins Output Timing Parameters (Part 1 of 3)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
LVDS	—	GCLK	t_{co}	2.744	2.932	4.083	4.440	4.901	4.771	5.049	4.540	5.002	4.873	5.107	ns
		GCLK PLL	t_{co}	0.931	1.057	1.249	1.300	1.458	1.480	1.486	1.382	1.545	1.563	1.456	ns
LVDS_E_1R	—	GCLK	t_{co}	3.136	3.376	4.754	5.156	5.664	5.526	5.797	5.281	5.790	5.652	5.871	ns
		GCLK PLL	t_{co}	1.333	1.511	1.930	2.026	2.231	2.245	2.243	2.133	2.343	2.352	2.229	ns
LVDS_E_3R	—	GCLK	t_{co}	3.118	3.366	4.792	5.202	5.718	5.580	5.851	5.332	5.851	5.713	5.932	ns
		GCLK PLL	t_{co}	1.315	1.501	1.968	2.072	2.285	2.299	2.297	2.184	2.404	2.413	2.290	ns
MINI-LVDS	—	GCLK	t_{co}	2.744	2.932	4.083	4.440	4.901	4.771	5.049	4.540	5.002	4.873	5.107	ns
		GCLK PLL	t_{co}	0.931	1.057	1.249	1.300	1.458	1.480	1.486	1.382	1.545	1.563	1.456	ns
MINI-LVDS_E_1R	—	GCLK	t_{co}	3.136	3.376	4.754	5.156	5.664	5.526	5.797	5.281	5.790	5.652	5.871	ns
		GCLK PLL	t_{co}	1.333	1.511	1.930	2.026	2.231	2.245	2.243	2.133	2.343	2.352	2.229	ns
MINI-LVDS_E_3R	—	GCLK	t_{co}	3.118	3.366	4.792	5.202	5.718	5.580	5.851	5.332	5.851	5.713	5.932	ns
		GCLK PLL	t_{co}	1.315	1.501	1.968	2.072	2.285	2.299	2.297	2.184	2.404	2.413	2.290	ns
RSDS	—	GCLK	t_{co}	2.744	2.932	4.083	4.440	4.901	4.771	5.049	4.540	5.002	4.873	5.107	ns
		GCLK PLL	t_{co}	0.931	1.057	1.249	1.300	1.458	1.480	1.486	1.382	1.545	1.563	1.456	ns
RSDS_E_1R	—	GCLK	t_{co}	3.136	3.376	4.754	5.156	5.664	5.526	5.797	5.281	5.790	5.652	5.871	ns
		GCLK PLL	t_{co}	1.333	1.511	1.930	2.026	2.231	2.245	2.243	2.133	2.343	2.352	2.229	ns
RSDS_E_3R	—	GCLK	t_{co}	3.118	3.366	4.792	5.202	5.718	5.580	5.851	5.332	5.851	5.713	5.932	ns
		GCLK PLL	t_{co}	1.315	1.501	1.968	2.072	2.285	2.299	2.297	2.184	2.404	2.413	2.290	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{co}	3.162	3.409	4.828	5.236	5.751	5.613	5.884	5.365	5.880	5.742	5.961	ns
		GCLK PLL	t_{co}	1.359	1.544	2.004	2.106	2.318	2.332	2.330	2.217	2.433	2.442	2.319	ns
	6mA	GCLK	t_{co}	3.148	3.395	4.815	5.223	5.738	5.600	5.871	5.351	5.867	5.729	5.948	ns
		GCLK PLL	t_{co}	1.345	1.530	1.991	2.093	2.305	2.319	2.317	2.203	2.420	2.429	2.306	ns
	8mA	GCLK	t_{co}	3.144	3.391	4.813	5.223	5.739	5.601	5.872	5.351	5.869	5.731	5.950	ns
		GCLK PLL	t_{co}	1.341	1.526	1.989	2.093	2.306	2.320	2.318	2.203	2.422	2.431	2.308	ns

Table 1–123. EP3SE110 Column Pins Output Timing Parameters (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		UnitS
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
1.2-V HSTL CLASS I	4mA	GCLK	t_{co}	3.336	3.336	4.703	5.096	5.577	5.442	5.754	5.096	5.577	5.442	5.754	ns
		GCLK PLL	t_{co}	3.716	3.728	5.289	5.719	6.333	6.169	6.571	5.719	6.333	6.169	6.571	ns
	6mA	GCLK	t_{co}	3.328	3.328	4.694	5.087	5.568	5.433	5.745	5.087	5.568	5.433	5.745	ns
		GCLK PLL	t_{co}	3.707	3.720	5.280	5.710	6.324	6.160	6.562	5.710	6.324	6.160	6.562	ns
	8mA	GCLK	t_{co}	3.329	3.329	4.702	5.095	5.577	5.442	5.754	5.095	5.577	5.442	5.754	ns
		GCLK PLL	t_{co}	3.707	3.721	5.287	5.718	6.333	6.169	6.571	5.718	6.333	6.169	6.571	ns
	10mA	GCLK	t_{co}	3.318	3.318	4.689	5.082	5.563	5.428	5.740	5.082	5.563	5.428	5.740	ns
		GCLK PLL	t_{co}	3.697	3.710	5.274	5.704	6.319	6.155	6.557	5.704	6.319	6.155	6.557	ns
	12mA	GCLK	t_{co}	3.318	3.318	4.689	5.082	5.564	5.429	5.741	5.082	5.564	5.429	5.741	ns
		GCLK PLL	t_{co}	3.697	3.710	5.274	5.705	6.320	6.156	6.558	5.705	6.320	6.156	6.558	ns
1.2-V HSTL CLASS II	16mA	GCLK	t_{co}	3.339	3.339	4.705	5.097	5.577	5.442	5.754	5.097	5.577	5.442	5.754	ns
		GCLK PLL	t_{co}	3.718	3.731	5.290	5.720	6.333	6.169	6.571	5.720	6.333	6.169	6.571	ns
3.0-V PCI	—	GCLK	t_{co}	3.442	3.442	4.750	5.131	5.602	5.467	5.779	5.131	5.602	5.467	5.779	ns
		GCLK PLL	t_{co}	3.821	3.834	5.335	5.756	6.358	6.194	6.596	5.756	6.358	6.194	6.596	ns
3.0-V PCI-X	—	GCLK	t_{co}	3.442	3.442	4.750	5.131	5.602	5.467	5.779	5.131	5.602	5.467	5.779	ns
		GCLK PLL	t_{co}	3.821	3.834	5.335	5.756	6.358	6.194	6.596	5.756	6.358	6.194	6.596	ns

Table 1–124 lists the EP3SE110 row pins output timing parameters for single-ended I/O standards.

Table 1–124. EP3SE110 Row Pins Output Timing Parameters (Part 1 of 5)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
3.3-V LVTTL	4mA	GCLK	t_{co}	3.208	3.456	4.797	5.180	5.703	5.543	5.850	5.304	5.827	5.696	5.930	ns
		GCLK PLL	t_{co}	1.452	1.625	2.008	2.086	2.326	2.346	2.347	2.239	2.435	2.455	2.342	ns
	8mA	GCLK	t_{co}	3.142	3.385	4.687	5.069	5.589	5.429	5.736	5.191	5.712	5.581	5.815	ns
		GCLK PLL	t_{co}	1.359	1.554	1.898	1.975	2.181	2.201	2.202	2.098	2.286	2.306	2.193	ns
	12mA	GCLK	t_{co}	3.063	3.296	4.581	4.969	5.493	5.333	5.640	5.092	5.612	5.481	5.715	ns
		GCLK PLL	t_{co}	1.260	1.465	1.792	1.875	2.053	2.073	2.074	1.971	2.154	2.174	2.061	ns

Table 1–132. EP3SE260 Row Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
SSTL-15 CLASS I	GCLK	t_{su}	1.064	0.995	-1.974	-1.378	-1.541	-1.455	-1.458	-1.477	-1.526	-1.455	-1.458	ns
		t_h	1.325	1.487	2.209	-2.007	-2.128	-2.081	-2.534	-1.932	-2.182	-2.081	-2.534	ns
	GCLK PLL	t_{su}	-1.173	-1.324	1.773	2.248	2.393	2.331	2.783	2.185	2.457	2.331	2.783	ns
		t_h	1.078	1.007	-1.294	1.874	2.092	1.974	1.990	1.986	2.088	1.974	1.990	ns
1.8-V HSTL CLASS I	GCLK	t_{su}	1.311	1.475	-1.974	-1.378	-1.541	-1.455	-1.458	-1.477	-1.526	-1.455	-1.458	ns
		t_h	-1.173	-1.324	-1.303	1.884	2.110	1.992	2.008	1.997	2.105	1.992	2.008	ns
	GCLK PLL	t_{su}	1.078	1.007	-1.965	-1.388	-1.559	-1.473	-1.476	-1.488	-1.543	-1.473	-1.476	ns
		t_h	1.311	1.475	2.200	-1.997	-2.110	-2.063	-2.516	-1.921	-2.165	-2.063	-2.516	ns
1.8-V HSTL CLASS II	GCLK	t_{su}	-1.164	-1.312	1.782	2.238	2.375	2.313	2.765	2.174	2.440	2.313	2.765	ns
		t_h	1.087	1.019	-1.303	1.884	2.110	1.992	2.008	1.997	2.105	1.992	2.008	ns
	GCLK PLL	t_{su}	1.302	1.463	-1.965	-1.388	-1.559	-1.473	-1.476	-1.488	-1.543	-1.473	-1.476	ns
		t_h	-1.164	-1.312	-1.303	1.894	2.126	2.008	2.024	2.006	2.121	2.008	2.024	ns
1.5-V HSTL CLASS I	GCLK	t_{su}	1.087	1.019	-2.056	-1.398	-1.575	-1.489	-1.492	-1.497	-1.559	-1.489	-1.492	ns
		t_h	1.302	1.463	1.752	-1.987	-2.094	-2.047	-2.500	-1.912	-2.149	-2.047	-2.500	ns
	GCLK PLL	t_{su}	-1.225	-1.385	2.290	2.228	2.359	2.297	2.749	2.165	2.424	2.297	2.749	ns
		t_h	1.361	1.535	-2.056	1.894	2.126	2.008	2.024	2.006	2.121	2.008	2.024	ns
1.5-V HSTL CLASS II	GCLK	t_{su}	0.977	0.972	1.752	-1.398	-1.575	-1.489	-1.492	-1.497	-1.559	-1.489	-1.492	ns
		t_h	-0.698	-0.674	2.290	-1.987	-2.094	-2.047	-2.500	-1.912	-2.149	-2.047	-2.500	ns
	GCLK PLL	t_{su}	-1.225	-1.385	2.290	2.228	2.359	2.297	2.749	2.165	2.424	2.297	2.749	ns
		t_h	1.361	1.535	2.290	1.894	2.126	2.008	2.024	2.006	2.121	2.008	2.024	ns
1.2-V HSTL CLASS I	GCLK	t_{su}	0.977	0.972	2.290	-1.398	-1.575	-1.489	-1.492	-1.497	-1.559	-1.489	-1.492	ns
		t_h	-0.698	-0.674	2.290	-1.987	-2.094	-2.047	-2.500	-1.912	-2.149	-2.047	-2.500	ns
	GCLK PLL	t_{su}	-1.219	-1.374	-2.059	-1.988	-2.283	-2.177	-2.643	-2.003	-2.382	-2.177	-2.643	ns
		t_h	1.355	1.524	1.749	1.864	1.862	1.767	1.884	1.864	1.883	1.767	1.884	ns
1.2-V HSTL CLASS II	GCLK	t_{su}	0.983	0.983	2.293	2.233	2.553	2.431	2.902	2.260	2.659	2.431	2.902	ns
		t_h	-0.704	-0.685	-2.059	-1.988	-2.283	-2.177	-2.643	-2.003	-2.382	-2.177	-2.643	ns
	GCLK PLL	t_{su}	-1.219	-1.374	-2.059	-1.988	-2.283	-2.177	-2.643	-2.003	-2.382	-2.177	-2.643	ns
		t_h	1.355	1.524	1.749	1.864	1.862	1.767	1.884	1.864	1.883	1.767	1.884	ns
3.0-V PCI	GCLK	t_{su}	0.983	0.983	2.293	2.233	2.553	2.431	2.902	2.260	2.659	2.431	2.902	ns
		t_h	-0.704	-0.685	-2.056	-1.989	-2.286	-2.180	-2.646	-2.002	-2.387	-2.180	-2.646	ns
	GCLK PLL	t_{su}	-1.225	-1.385	2.290	2.234	2.556	2.434	2.905	2.259	2.664	2.434	2.905	ns
		t_h	1.361	1.535	-2.056	-1.989	-2.286	-2.180	-2.646	-2.002	-2.387	-2.180	-2.646	ns
3.0-V PCI-X	GCLK	t_{su}	0.977	0.972	1.752	1.863	1.859	1.764	1.881	1.865	1.878	1.764	1.881	ns
		t_h	-0.698	-0.674	2.290	2.234	2.556	2.434	2.905	2.259	2.664	2.434	2.905	ns
	GCLK PLL	t_{su}	-1.225	-1.385	2.299	2.247	2.571	2.449	2.920	2.268	2.674	2.449	2.920	ns
		t_h	1.361	1.535	-2.065	-2.002	-2.301	-2.195	-2.661	-2.011	-2.397	-2.195	-2.661	ns

Table 1–136. EP3SE260 Row Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{su}	-1.169	-1.249	-1.881	-1.908	-2.071	-1.995	-2.440	-1.928	-2.086	-1.995	-2.440	ns
		t_h	1.306	1.402	2.121	2.156	2.341	2.250	2.701	2.186	2.369	2.250	2.701	ns
	GCLK PLL	t_{su}	1.032	1.038	1.829	1.945	2.171	2.052	2.073	1.954	2.182	2.052	2.073	ns
		t_h	-0.751	-0.739	-1.348	-1.445	-1.615	-1.528	-1.532	-1.440	-1.612	-1.528	-1.532	ns

Table 1–137 lists the EP3SE260 column pins output timing parameters for differential I/O standards.

Table 1–137. EP3SE260 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
LVDS_E_1R	—	GCLK	t_{co}	3.479	3.750	5.506	5.712	6.270	6.106	6.513	5.854	6.411	6.106	6.513	ns
		GCLK PLL	t_{co}	3.475	3.753	5.553	5.767	6.332	6.168	6.575	5.913	6.477	6.168	6.575	ns
LVDS_E_3R	—	GCLK	t_{co}	3.479	3.750	5.506	5.712	6.270	6.106	6.513	5.854	6.411	6.106	6.513	ns
		GCLK PLL	t_{co}	3.475	3.753	5.553	5.767	6.332	6.168	6.575	5.913	6.477	6.168	6.575	ns
MINI-LVDS_E_1R	—	GCLK	t_{co}	3.479	3.750	5.506	5.712	6.270	6.106	6.513	5.854	6.411	6.106	6.513	ns
		GCLK PLL	t_{co}	3.475	3.753	5.553	5.767	6.332	6.168	6.575	5.913	6.477	6.168	6.575	ns
MINI-LVDS_E_3R	—	GCLK	t_{co}	3.506	3.783	5.577	5.790	6.354	6.190	6.597	5.934	6.497	6.190	6.597	ns
		GCLK PLL	t_{co}	3.496	3.773	5.567	5.779	6.344	6.180	6.587	5.923	6.487	6.180	6.587	ns
RSDS_E_1R	—	GCLK	t_{co}	3.496	3.773	5.570	5.783	6.348	6.184	6.591	5.928	6.492	6.184	6.591	ns
		GCLK PLL	t_{co}	3.489	3.767	5.563	5.777	6.342	6.178	6.585	5.921	6.486	6.178	6.585	ns
RSDS_E_3R	—	GCLK	t_{co}	3.488	3.765	5.560	5.774	6.339	6.175	6.582	5.918	6.482	6.175	6.582	ns
		GCLK PLL	t_{co}	3.510	3.787	5.581	5.794	6.358	6.194	6.601	5.938	6.502	6.194	6.601	ns

Table 1–168 and Table 1–169 list the regional clock timing parameters for EP3SL200.

Table 1–168. EP3SL200 Column Pin Regional Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	2.006	2.035	3.020	3.113	3.494	3.213	3.743	3.113	3.531	3.213	3.743	ns
t_{COUT}	2.006	2.035	3.020	3.113	3.494	3.213	3.743	3.113	3.531	3.213	3.743	ns
t_{PLLCIN}	0.059	0.086	-0.150	-0.191	-0.109	-0.094	0.116	-0.191	0.291	-0.094	0.116	ns
$t_{PLLCOUT}$	0.059	0.086	-0.150	-0.191	-0.109	-0.094	0.116	-0.191	0.291	-0.094	0.116	ns

Table 1–169. EP3SL200 Row Pin Regional Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.937	2.065	3.000	3.070	3.414	3.275	3.597	3.139	3.479	3.275	3.597	ns
t_{COUT}	1.855	1.974	2.848	2.910	3.233	3.104	3.438	2.971	3.290	3.104	3.438	ns
t_{PLLCIN}	0.126	0.197	-0.059	-0.091	-0.051	-0.036	-0.041	-0.043	0.410	-0.036	-0.041	ns
$t_{PLLCOUT}$	0.044	0.106	-0.211	-0.254	-0.232	-0.207	-0.200	-0.213	0.221	-0.207	-0.200	ns

Table 1–170 and Table 1–171 list the periphery clock timing parameters for EP3SL200 devices.

Table 1–170. EP3SL200 Column Pin Periphery Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.720	1.712	2.615	2.776	3.177	3.044	3.660	2.776	3.177	3.044	3.660	ns
t_{COUT}	1.720	1.712	2.615	2.776	3.177	3.044	3.660	2.776	3.177	3.044	3.660	ns
t_{PLLCIN}	0.037	0.064	-0.173	-0.213	-0.135	-0.118	0.090	-0.213	0.292	-0.118	0.090	ns
$t_{PLLCOUT}$	0.037	0.064	-0.173	-0.213	-0.135	-0.118	0.090	-0.213	0.292	-0.118	0.090	ns

Table 1–171. EP3SL200 Row Pin Periphery Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.501	1.575	2.380	2.518	2.892	2.761	3.077	2.567	2.938	2.761	3.077	ns
t_{COUT}	1.419	1.484	2.225	2.355	2.711	2.590	2.918	2.397	2.749	2.590	2.918	ns
t_{PLLCIN}	0.105	0.174	-0.081	-0.118	-0.077	-0.061	-0.063	-0.067	0.411	-0.061	-0.063	ns
$t_{PLLCOUT}$	0.023	0.083	-0.233	-0.281	-0.258	-0.232	-0.222	-0.237	0.222	-0.232	-0.222	ns

Table 1–176 and Table 1–177 list the periphery clock timing parameters for EP3SL340 devices.

Table 1–176. EP3SL340 Column Pin Periphery Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.778	1.760	2.687	2.847	3.240	3.099	3.718	2.847	3.240	3.099	3.718	ns
t_{COUT}	1.778	1.760	2.687	2.847	3.240	3.099	3.718	2.847	3.240	3.099	3.718	ns
t_{PLLCIN}	0.086	0.061	-0.164	-0.161	-0.140	-0.097	0.101	-0.161	-0.140	-0.097	0.101	ns
$t_{PLLCOUT}$	0.086	0.061	-0.164	-0.161	-0.140	-0.097	0.101	-0.161	-0.140	-0.097	0.101	ns

Table 1–177. EP3SL340 Row Pin Periphery Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.524	1.616	2.435	2.567	2.958	2.823	3.141	2.605	3.002	2.861	3.165	ns
t_{COUT}	1.442	1.525	2.280	2.404	2.777	2.652	2.982	2.435	2.813	2.682	3.006	ns
t_{PLLCIN}	0.116	0.211	-0.039	-0.116	-0.055	-0.030	-0.051	-0.040	-0.006	0.050	-0.098	ns
$t_{PLLCOUT}$	0.034	0.120	-0.191	-0.279	-0.236	-0.201	-0.210	-0.210	-0.195	-0.129	-0.257	ns

EP3SE50 Clock Timing Parameters

Table 1–178 and Table 1–179 list the global clock timing parameters for EP3SE50 devices.

Table 1–178. EP3SE50 Column Pin Global Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.786	1.789	2.495	2.748	3.111	2.993	3.489	2.748	3.105	2.993	3.489	ns
t_{COUT}	1.786	1.789	2.495	2.748	3.111	2.993	3.489	2.748	3.105	2.993	3.489	ns
t_{PLLCIN}	0.023	0.027	-0.204	-0.268	-0.226	-0.180	0.025	-0.268	0.249	-0.180	0.025	ns
$t_{PLLCOUT}$	0.083	0.103	-0.068	-0.131	-0.226	-0.010	0.025	-0.131	0.249	-0.010	0.025	ns

Table 1–179. EP3SE50 Row Pin Global Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.739	1.849	2.536	2.769	3.112	3.010	3.250	2.830	3.171	3.069	3.276	ns
t_{COUT}	1.657	1.758	2.394	2.606	2.931	2.839	3.091	2.660	2.982	2.890	3.117	ns
t_{PLLCIN}	0.044	0.117	-0.143	-0.220	-0.183	-0.135	-0.189	-0.171	0.345	-0.088	-0.242	ns
$t_{PLLCOUT}$	-0.038	0.026	-0.285	-0.383	-0.364	-0.306	-0.348	-0.341	0.156	-0.267	-0.401	ns

Chapter Revision History

Table 1–202 lists the revision history for this chapter.

Table 1–202. Chapter Revision History (Part 1 of 2)

Date	Version	Changes Made
July 2010	2.3	Updated Table 1–11, Table 1–20, Table 1–25, and Table 1–33.
March 2010	2.2	Updated for the Quartus II software version 9.1 SP2 release: ■ Updated Table 1–7, Table 1–8, Table 1–11, Table 1–19, Table 1–23, Table 1–25, Table 1–28, Table 1–29, and Table 1–33. ■ Updated the "Sinusoidal Maximum Allowed Overshoot/Undershoot Voltage" and "External Memory Interface Specifications" sections. ■ Minor text edits.
July 2009	2.1	Minor text edits.
May 2009	2.0	■ Updated Table 1–1, Table 1–7, Table 1–9, Table 1–18, Table 1–21, Table 1–22, Table 1–23, Table 1–25, Table 1–26, Table 1–28, Table 1–29, Table 1–30, Table 1–33, Table 1–35, Table 1–41, Table 1–43, Table 1–51, Table 1–53, Table 1–61, Table 1–63, Table 1–71, Table 1–73, Table 1–81, Table 1–83, Table 1–91, Table 1–93, Table 1–101, Table 1–103, Table 1–111, Table 1–113, Table 1–121, Table 1–123, Table 1–131, and Table 1–133. ■ Updated Equation 1–1.
February 2009	1.9	■ Updated "Programmable IOE Delay", "PLL Specifications", "DSP Block Specifications", "TriMatrix Memory Block Specifications", "External Memory Interface Specifications", and "High-Speed I/O Specifications" sections. ■ Updated all Timing Information Tables in "User I/O Pin Timing" and "Dedicated Clock Pin Timing" sections. ■ Removed "Referenced Documents" and "Maximum Input and Output Toggle Rate" sections.
October 2008	1.8	■ Updated "Operating Conditions". ■ Added "Bus Hold Specifications". ■ Updated Table 1–3, Table 1–6, Table 1–7, Table 1–11, and Table 1–14. ■ Updated Table 1–17 to Table 1–25. ■ Updated Table 1–39 to Table 1–47. ■ Updated Table 1–50 to Table 1–210. ■ Added (Note 3) to Table 1–11. ■ Added (Note 1) to Table 1–14. ■ Added (Note 6) to Table 1–17. ■ Added (Note 1) to Table 1–47. ■ Added Table 1–26. ■ Added Figure 1–2.