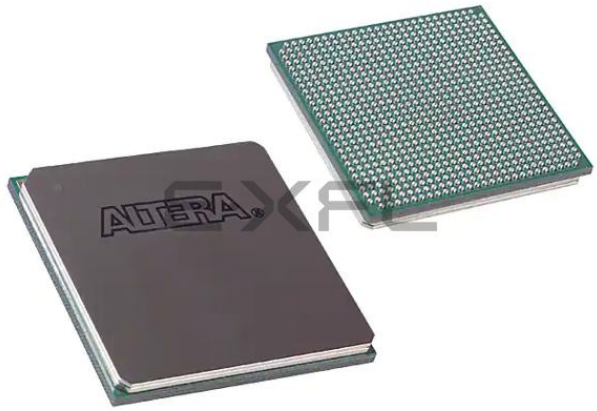

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1900
Number of Logic Elements/Cells	47500
Total RAM Bits	5760000
Number of I/O	488
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3se50f780c4n

Table 1–41. EP3SL50 Column Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
SSTL-15 CLASS I	GCLK	t_{su}	-0.608	-0.607	-0.903	-0.990	-1.084	-1.037	-1.398	-0.990	-1.084	-1.037	-1.398	ns
		t_h	0.736	0.734	1.079	1.188	1.301	1.245	1.596	1.188	1.301	1.245	1.596	ns
	GCLK PLL	t_{su}	-0.895	-0.895	-1.301	-1.416	-1.543	-1.481	-1.797	-1.416	-1.543	-1.481	-1.797	ns
		t_h	1.148	1.148	1.669	1.828	1.999	1.915	2.237	1.828	1.999	1.915	2.237	ns
1.8-V HSTL CLASS I	GCLK	t_{su}	-0.608	-0.607	-0.903	-0.990	-1.084	-1.037	-1.398	-0.990	-1.084	-1.037	-1.398	ns
		t_h	0.736	0.734	1.079	1.188	1.301	1.245	1.596	1.188	1.301	1.245	1.596	ns
	GCLK PLL	t_{su}	-0.895	-0.895	-1.301	-1.416	-1.543	-1.481	-1.797	-1.416	-1.543	-1.481	-1.797	ns
		t_h	1.148	1.148	1.669	1.828	1.999	1.915	2.237	1.828	1.999	1.915	2.237	ns
1.8-V HSTL CLASS II	GCLK	t_{su}	-0.619	-0.618	-0.912	-1.001	-1.103	-1.056	-1.417	-1.001	-1.103	-1.056	-1.417	ns
		t_h	0.747	0.745	1.089	1.199	1.320	1.264	1.615	1.199	1.320	1.264	1.615	ns
	GCLK PLL	t_{su}	-0.906	-0.906	-1.312	-1.427	-1.562	-1.500	-1.816	-1.427	-1.562	-1.500	-1.816	ns
		t_h	1.159	1.159	1.681	1.839	2.018	1.934	2.256	1.839	2.018	1.934	2.256	ns
1.5-V HSTL CLASS I	GCLK	t_{su}	-0.619	-0.618	-0.912	-1.001	-1.103	-1.056	-1.417	-1.001	-1.103	-1.056	-1.417	ns
		t_h	0.747	0.745	1.089	1.199	1.320	1.264	1.615	1.199	1.320	1.264	1.615	ns
	GCLK PLL	t_{su}	-0.906	-0.906	-1.312	-1.427	-1.562	-1.500	-1.816	-1.427	-1.562	-1.500	-1.816	ns
		t_h	1.159	1.159	1.681	1.839	2.018	1.934	2.256	1.839	2.018	1.934	2.256	ns
1.5-V HSTL CLASS II	GCLK	t_{su}	-0.608	-0.607	-0.903	-0.990	-1.084	-1.037	-1.398	-0.990	-1.084	-1.037	-1.398	ns
		t_h	0.736	0.734	1.079	1.188	1.301	1.245	1.596	1.188	1.301	1.245	1.596	ns
	GCLK PLL	t_{su}	-0.895	-0.895	-1.301	-1.416	-1.543	-1.481	-1.797	-1.416	-1.543	-1.481	-1.797	ns
		t_h	1.148	1.148	1.669	1.828	1.999	1.915	2.237	1.828	1.999	1.915	2.237	ns
1.2-V HSTL CLASS I	GCLK	t_{su}	-0.608	-0.607	-0.903	-0.990	-1.084	-1.037	-1.398	-0.990	-1.084	-1.037	-1.398	ns
		t_h	0.736	0.734	1.079	1.188	1.301	1.245	1.596	1.188	1.301	1.245	1.596	ns
	GCLK PLL	t_{su}	-0.895	-0.895	-1.301	-1.416	-1.543	-1.481	-1.797	-1.416	-1.543	-1.481	-1.797	ns
		t_h	1.148	1.148	1.669	1.828	1.999	1.915	2.237	1.828	1.999	1.915	2.237	ns
1.2-V HSTL CLASS II	GCLK	t_{su}	-0.596	-0.595	-0.893	-0.979	-1.068	-1.021	-1.382	-0.979	-1.068	-1.021	-1.382	ns
		t_h	0.724	0.722	1.069	1.177	1.285	1.229	1.580	1.177	1.285	1.229	1.580	ns
	GCLK PLL	t_{su}	-0.883	-0.883	-1.291	-1.405	-1.527	-1.465	-1.781	-1.405	-1.527	-1.465	-1.781	ns
		t_h	1.136	1.136	1.659	1.817	1.983	1.899	2.221	1.817	1.983	1.899	2.221	ns
3.0-V PCI	GCLK	t_{su}	-0.596	-0.595	-0.893	-0.979	-1.068	-1.021	-1.382	-0.979	-1.068	-1.021	-1.382	ns
		t_h	0.724	0.722	1.069	1.177	1.285	1.229	1.580	1.177	1.285	1.229	1.580	ns
	GCLK PLL	t_{su}	-0.883	-0.883	-1.291	-1.405	-1.527	-1.465	-1.781	-1.405	-1.527	-1.465	-1.781	ns
		t_h	1.136	1.136	1.659	1.817	1.983	1.899	2.221	1.817	1.983	1.899	2.221	ns
3.0-V PCI-X	GCLK	t_{su}	-0.701	-0.700	-1.003	-1.105	-1.310	-1.265	-1.626	-1.105	-1.310	-1.265	-1.626	ns
		t_h	0.827	0.825	1.181	1.306	1.530	1.474	1.829	1.306	1.530	1.474	1.829	ns
	GCLK PLL	t_{su}	-0.986	-0.986	-1.404	-1.534	-1.772	-1.712	-2.025	-1.534	-1.772	-1.712	-2.025	ns
		t_h	1.237	1.237	1.773	1.949	2.231	2.147	2.470	1.949	2.231	2.147	2.470	ns

Table 1–42. EP3SL50 Row Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
1.2-V HSTL CLASS I	GCLK	t_{su}	0.904	0.906	1.473	-1.503	-1.682	-1.598	-1.620	-1.497	-1.674	-1.587	-1.665	ns
		t_h	-0.655	-0.645	1.473	-1.311	-1.418	-1.362	-1.630	-1.322	-1.428	-1.374	-1.666	ns
	GCLK PLL	t_{su}	-0.884	-0.914	-1.291	-1.412	-1.634	-1.580	-1.842	-1.428	-1.639	-1.588	-1.875	ns
		t_h	0.997	1.040	1.554	1.774	1.924	1.808	1.834	1.768	1.931	1.777	1.885	ns
1.2-V HSTL CLASS II	GCLK	t_{su}	0.910	0.917	1.476	1.619	1.864	1.796	2.057	1.645	1.878	1.814	2.090	ns
		t_h	-0.661	-0.656	-1.291	-1.412	-1.634	-1.580	-1.842	-1.428	-1.639	-1.588	-1.875	ns
	GCLK PLL	t_{su}	-0.884	-0.914	-1.291	-1.412	-1.634	-1.580	-1.842	-1.428	-1.639	-1.588	-1.875	ns
		t_h	0.997	1.040	1.554	1.774	1.924	1.808	1.834	1.768	1.931	1.777	1.885	ns
3.0-V PCI	GCLK	t_{su}	0.910	0.917	1.476	1.619	1.864	1.796	2.057	1.645	1.878	1.814	2.090	ns
		t_h	-0.661	-0.656	-1.288	-1.413	-1.637	-1.583	-1.845	-1.427	-1.644	-1.593	-1.880	ns
	GCLK PLL	t_{su}	-0.890	-0.925	1.473	1.620	1.867	1.799	2.060	1.644	1.883	1.819	2.095	ns
		t_h	1.003	1.051	-1.288	-1.413	-1.637	-1.583	-1.845	-1.427	-1.644	-1.593	-1.880	ns
3.0-V PCI-X	GCLK	t_{su}	0.904	0.906	1.557	1.773	1.921	1.805	1.831	1.769	1.926	1.772	1.880	ns
		t_h	-0.655	-0.645	1.473	1.620	1.867	1.799	2.060	1.644	1.883	1.819	2.095	ns
	GCLK PLL	t_{su}	-0.890	-0.925	1.482	1.633	1.882	1.814	2.075	1.653	1.893	1.829	2.105	ns
		t_h	1.003	1.051	-1.297	-1.426	-1.652	-1.598	-1.860	-1.436	-1.654	-1.603	-1.890	ns

Table 1–43. EP3SL50 Column Pins output Timing Parameters (Part 2 of 7)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
3.0-V LVCMOS	4mA	GCLK	t_{co}	3.046	3.034	4.253	4.610	5.075	4.958	5.157	4.610	5.075	4.958	5.157	ns
		GCLK PLL	t_{co}	3.402	3.402	4.776	5.172	5.685	5.543	5.808	5.172	5.685	5.543	5.808	ns
	8mA	GCLK	t_{co}	2.967	2.955	4.130	4.481	4.940	4.823	5.022	4.481	4.940	4.823	5.022	ns
		GCLK PLL	t_{co}	3.323	3.323	4.652	5.043	5.550	5.408	5.673	5.043	5.550	5.408	5.673	ns
	12mA	GCLK	t_{co}	2.962	2.950	4.122	4.474	4.931	4.813	5.015	4.474	4.931	4.813	5.015	ns
		GCLK PLL	t_{co}	3.318	3.318	4.645	5.036	5.541	5.398	5.665	5.036	5.541	5.398	5.665	ns
	16mA	GCLK	t_{co}	2.953	2.941	4.108	4.459	4.916	4.798	5.000	4.459	4.916	4.798	5.000	ns
		GCLK PLL	t_{co}	3.309	3.309	4.631	5.021	5.526	5.383	5.650	5.021	5.526	5.383	5.650	ns
2.5 V	4mA	GCLK	t_{co}	3.168	3.156	4.460	4.837	5.322	5.205	5.405	4.837	5.322	5.205	5.405	ns
		GCLK PLL	t_{co}	3.524	3.524	4.983	5.399	5.932	5.790	6.055	5.399	5.932	5.790	6.055	ns
	8mA	GCLK	t_{co}	3.068	3.056	4.341	4.711	5.190	5.073	5.272	4.711	5.190	5.073	5.272	ns
		GCLK PLL	t_{co}	3.424	3.424	4.864	5.273	5.800	5.658	5.923	5.273	5.800	5.658	5.923	ns
	12mA	GCLK	t_{co}	3.024	3.012	4.254	4.620	5.094	4.976	5.178	4.620	5.094	4.976	5.178	ns
		GCLK PLL	t_{co}	3.380	3.380	4.777	5.182	5.704	5.561	5.828	5.182	5.704	5.561	5.828	ns
	16mA	GCLK	t_{co}	2.986	2.974	4.215	4.578	5.051	4.933	5.135	4.578	5.051	4.933	5.135	ns
		GCLK PLL	t_{co}	3.342	3.342	4.738	5.140	5.661	5.518	5.785	5.140	5.661	5.518	5.785	ns

Table 1–44 lists the EP3SL50 row pins output timing parameters for single-ended I/O standards.

Table 1–44. EP3SL50 Row Pins output Timing Parameters (Part 1 of 4)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
3.3-V LVTTL	4mA	GCLK	t_{co}	3.197	3.438	4.781	5.176	5.684	5.549	5.751	5.305	5.818	5.682	5.828	ns
		GCLK PLL	t_{co}	1.482	1.677	2.061	2.175	2.372	2.388	2.308	2.295	2.495	2.512	2.303	ns
	8mA	GCLK	t_{co}	3.104	3.333	4.651	5.038	5.540	5.405	5.607	5.164	5.669	5.533	5.679	ns
		GCLK PLL	t_{co}	1.415	1.606	1.951	2.037	2.228	2.244	2.164	2.154	2.346	2.363	2.154	ns
	12mA	GCLK	t_{co}	3.014	3.233	4.532	4.915	5.412	5.277	5.479	5.037	5.537	5.401	5.547	ns
		GCLK PLL	t_{co}	1.336	1.517	1.845	1.930	2.100	2.116	2.036	2.046	2.214	2.260	2.022	ns
3.3-V LVCMOS	4mA	GCLK	t_{co}	3.207	3.442	4.789	5.181	5.689	5.554	5.756	5.311	5.823	5.687	5.833	ns
		GCLK PLL	t_{co}	1.492	1.684	2.065	2.180	2.377	2.393	2.313	2.301	2.500	2.517	2.308	ns
	8mA	GCLK	t_{co}	3.018	3.237	4.538	4.921	5.418	5.283	5.485	5.043	5.544	5.408	5.554	ns
		GCLK PLL	t_{co}	1.340	1.521	1.856	1.945	2.106	2.122	2.042	2.058	2.221	2.269	2.029	ns
3.0-V LVTTL	4mA	GCLK	t_{co}	3.151	3.384	4.733	5.129	5.641	5.506	5.708	5.262	5.776	5.640	5.786	ns
		GCLK PLL	t_{co}	1.442	1.638	2.028	2.128	2.329	2.345	2.265	2.252	2.453	2.470	2.261	ns
	8mA	GCLK	t_{co}	3.026	3.257	4.580	4.970	5.477	5.342	5.544	5.100	5.612	5.475	5.621	ns
		GCLK PLL	t_{co}	1.341	1.526	1.891	1.969	2.165	2.181	2.101	2.090	2.289	2.305	2.096	ns
	12mA	GCLK	t_{co}	2.987	3.206	4.498	4.887	5.389	5.254	5.456	5.014	5.519	5.382	5.528	ns
		GCLK PLL	t_{co}	1.304	1.488	1.831	1.903	2.077	2.093	2.013	2.016	2.196	2.222	2.003	ns
3.0-V LVCMOS	4mA	GCLK	t_{co}	3.065	3.303	4.627	5.022	5.530	5.395	5.597	5.154	5.665	5.528	5.674	ns
		GCLK PLL	t_{co}	1.363	1.550	1.926	2.021	2.218	2.234	2.154	2.144	2.342	2.358	2.149	ns
	8mA	GCLK	t_{co}	2.969	3.188	4.463	4.848	5.350	5.215	5.417	4.974	5.479	5.342	5.488	ns
		GCLK PLL	t_{co}	1.291	1.472	1.803	1.874	2.038	2.054	1.974	1.986	2.156	2.193	1.963	ns
2.5 V	4mA	GCLK	t_{co}	3.177	3.420	4.865	5.283	5.813	5.678	5.880	5.422	5.955	5.818	5.964	ns
		GCLK PLL	t_{co}	1.468	1.675	2.136	2.282	2.501	2.517	2.437	2.412	2.632	2.648	2.439	ns
	8mA	GCLK	t_{co}	3.067	3.321	4.710	5.120	5.643	5.508	5.710	5.255	5.781	5.644	5.790	ns
		GCLK PLL	t_{co}	1.383	1.572	2.012	2.119	2.331	2.347	2.267	2.245	2.458	2.474	2.265	ns
	12mA	GCLK	t_{co}	3.021	3.245	4.599	5.001	5.517	5.382	5.584	5.132	5.651	5.514	5.660	ns
		GCLK PLL	t_{co}	1.326	1.528	1.928	2.015	2.205	2.221	2.141	2.132	2.328	2.354	2.135	ns

Table 1–52. EP3SL70 Row Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
SSTL-15 CLASS I	GCLK	t_{su}	1.010	0.990	-1.105	-1.472	-1.722	-1.633	-1.557	-1.461	-1.635	-1.548	-1.601	ns
		t_h	0.964	0.929	1.294	-1.309	-1.430	-1.374	-1.667	-1.348	-1.467	-1.413	-1.704	ns
	GCLK PLL	t_{su}	-0.836	-0.788	1.674	1.514	1.658	1.589	1.879	1.562	1.703	1.638	1.915	ns
		t_h	1.024	1.002	-1.276	1.918	2.223	2.104	2.029	1.917	2.144	2.026	2.076	ns
1.8-V HSTL CLASS I	GCLK	t_{su}	0.950	0.917	-1.105	-1.472	-1.722	-1.633	-1.557	-1.461	-1.635	-1.548	-1.601	ns
		t_h	-0.836	-0.788	-1.285	1.928	2.241	2.122	2.047	1.928	2.161	2.043	2.093	ns
	GCLK PLL	t_{su}	1.024	1.002	-1.096	-1.482	-1.740	-1.651	-1.575	-1.472	-1.652	-1.565	-1.618	ns
		t_h	0.950	0.917	1.285	-1.299	-1.412	-1.356	-1.649	-1.337	-1.450	-1.396	-1.687	ns
1.8-V HSTL CLASS II	GCLK	t_{su}	-0.827	-0.776	1.683	1.504	1.640	1.571	1.861	1.551	1.686	1.621	1.898	ns
		t_h	1.033	1.014	-1.285	1.928	2.241	2.122	2.047	1.928	2.161	2.043	2.093	ns
	GCLK PLL	t_{su}	0.941	0.905	-1.096	-1.482	-1.740	-1.651	-1.575	-1.472	-1.652	-1.565	-1.618	ns
		t_h	-0.827	-0.776	-1.285	1.938	2.257	2.138	2.063	1.937	2.177	2.059	2.109	ns
1.5-V HSTL CLASS I	GCLK	t_{su}	1.033	1.014	-1.182	-1.492	-1.756	-1.667	-1.591	-1.481	-1.668	-1.581	-1.634	ns
		t_h	0.941	0.905	1.585	-1.289	-1.396	-1.340	-1.633	-1.328	-1.434	-1.380	-1.671	ns
	GCLK PLL	t_{su}	-0.817	-0.847	1.368	1.494	1.624	1.555	1.845	1.542	1.670	1.605	1.882	ns
		t_h	0.931	0.973	-1.182	1.938	2.257	2.138	2.063	1.937	2.177	2.059	2.109	ns
1.5-V HSTL CLASS II	GCLK	t_{su}	0.931	0.934	1.585	-1.492	-1.756	-1.667	-1.591	-1.481	-1.668	-1.581	-1.634	ns
		t_h	-0.682	-0.673	1.368	-1.289	-1.396	-1.340	-1.633	-1.328	-1.434	-1.380	-1.671	ns
	GCLK PLL	t_{su}	-0.817	-0.847	1.368	1.494	1.624	1.555	1.845	1.542	1.670	1.605	1.882	ns
		t_h	0.931	0.973	1.368	1.938	2.257	2.138	2.063	1.937	2.177	2.059	2.109	ns
1.2-V HSTL CLASS I	GCLK	t_{su}	0.931	0.934	1.368	-1.492	-1.756	-1.667	-1.591	-1.481	-1.668	-1.581	-1.634	ns
		t_h	-0.682	-0.673	1.368	-1.289	-1.396	-1.340	-1.633	-1.328	-1.434	-1.380	-1.671	ns
	GCLK PLL	t_{su}	-0.811	-0.836	-1.185	-1.296	-1.513	-1.460	-1.732	-1.306	-1.513	-1.464	-1.763	ns
		t_h	0.925	0.962	1.582	1.801	1.915	1.799	1.814	1.796	1.923	1.804	1.865	ns
1.2-V HSTL CLASS II	GCLK	t_{su}	0.937	0.945	1.371	1.505	1.747	1.679	1.951	1.526	1.756	1.693	1.982	ns
		t_h	-0.688	-0.684	-1.185	-1.296	-1.513	-1.460	-1.732	-1.306	-1.513	-1.464	-1.763	ns
	GCLK PLL	t_{su}	-0.811	-0.836	-1.185	-1.296	-1.513	-1.460	-1.732	-1.306	-1.513	-1.464	-1.763	ns
		t_h	0.925	0.962	1.582	1.801	1.915	1.799	1.814	1.796	1.923	1.804	1.865	ns
3.0-V PCI	GCLK	t_{su}	0.937	0.945	1.371	1.505	1.747	1.679	1.951	1.526	1.756	1.693	1.982	ns
		t_h	-0.688	-0.684	-1.182	-1.297	-1.516	-1.463	-1.735	-1.305	-1.518	-1.469	-1.768	ns
	GCLK PLL	t_{su}	-0.817	-0.847	1.368	1.506	1.750	1.682	1.954	1.525	1.761	1.698	1.987	ns
		t_h	0.931	0.973	-1.182	-1.297	-1.516	-1.463	-1.735	-1.305	-1.518	-1.469	-1.768	ns
3.0-V PCI-X	GCLK	t_{su}	0.931	0.934	1.585	1.800	1.912	1.796	1.811	1.797	1.918	1.799	1.860	ns
		t_h	-0.682	-0.673	1.368	1.506	1.750	1.682	1.954	1.525	1.761	1.698	1.987	ns
	GCLK PLL	t_{su}	-0.817	-0.847	1.377	1.519	1.765	1.697	1.969	1.534	1.771	1.708	1.997	ns
		t_h	0.931	0.973	-1.191	-1.310	-1.531	-1.478	-1.750	-1.314	-1.528	-1.479	-1.778	ns

Table 1–53. EP3SL70 Column Pins Output Timing Parameters (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
1.8 V	2mA	GCLK	t_{co}	3.378	3.378	4.810	5.219	5.742	5.621	5.829	5.219	5.742	5.621	5.829	ns
		GCLK PLL	t_{co}	3.705	3.705	5.294	5.748	6.339	6.196	6.478	5.748	6.339	6.196	6.478	ns
	4mA	GCLK	t_{co}	3.200	3.200	4.533	4.912	5.395	5.275	5.481	4.912	5.395	5.275	5.481	ns
		GCLK PLL	t_{co}	3.524	3.524	5.015	5.439	5.991	5.849	6.147	5.439	5.991	5.849	6.147	ns
	6mA	GCLK	t_{co}	3.115	3.115	4.424	4.796	5.284	5.163	5.371	4.796	5.284	5.163	5.371	ns
		GCLK PLL	t_{co}	3.442	3.442	4.908	5.324	5.881	5.738	6.035	5.324	5.881	5.738	6.035	ns
	8mA	GCLK	t_{co}	3.095	3.095	4.366	4.742	5.218	5.097	5.305	4.742	5.218	5.097	5.305	ns
		GCLK PLL	t_{co}	3.422	3.422	4.850	5.270	5.815	5.672	5.958	5.270	5.815	5.672	5.958	ns
	10mA	GCLK	t_{co}	3.032	3.032	4.306	4.668	5.137	5.016	5.224	4.668	5.137	5.016	5.224	ns
		GCLK PLL	t_{co}	3.359	3.359	4.789	5.195	5.734	5.591	5.889	5.195	5.734	5.591	5.889	ns
	12mA	GCLK	t_{co}	3.015	3.015	4.285	4.647	5.114	4.993	5.201	4.647	5.114	4.993	5.201	ns
		GCLK PLL	t_{co}	3.341	3.341	4.768	5.174	5.711	5.568	5.856	5.174	5.711	5.568	5.856	ns
1.5 V	2mA	GCLK	t_{co}	3.324	3.324	4.739	5.152	5.680	5.559	5.767	5.152	5.680	5.559	5.767	ns
		GCLK PLL	t_{co}	3.651	3.651	5.223	5.680	6.277	6.134	6.423	5.680	6.277	6.134	6.423	ns
	4mA	GCLK	t_{co}	3.112	3.112	4.420	4.795	5.288	5.167	5.375	4.795	5.288	5.167	5.375	ns
		GCLK PLL	t_{co}	3.439	3.439	4.904	5.324	5.885	5.742	6.037	5.324	5.885	5.742	6.037	ns
	6mA	GCLK	t_{co}	3.088	3.088	4.353	4.737	5.221	5.100	5.308	4.737	5.221	5.100	5.308	ns
		GCLK PLL	t_{co}	3.414	3.414	4.837	5.264	5.818	5.675	5.960	5.264	5.818	5.675	5.960	ns
	8mA	GCLK	t_{co}	3.076	3.076	4.337	4.712	5.201	5.080	5.288	4.712	5.201	5.080	5.288	ns
		GCLK PLL	t_{co}	3.403	3.403	4.820	5.239	5.798	5.655	5.943	5.239	5.798	5.655	5.943	ns
	10mA	GCLK	t_{co}	3.021	3.021	4.298	4.661	5.131	5.010	5.218	4.661	5.131	5.010	5.218	ns
		GCLK PLL	t_{co}	3.348	3.348	4.782	5.188	5.728	5.585	5.880	5.188	5.728	5.585	5.880	ns
	12mA	GCLK	t_{co}	3.015	3.015	4.281	4.648	5.120	4.999	5.207	4.648	5.120	4.999	5.207	ns
		GCLK PLL	t_{co}	3.343	3.343	4.765	5.177	5.717	5.574	5.859	5.177	5.717	5.574	5.859	ns

Table 1–55. EP3SL70 Column Pins Input Timing Parameters (Part 2 of 2)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{su}	-0.717	-0.740	-1.091	-1.204	-1.329	-1.272	-1.559	-1.205	-1.329	-1.275	-1.595	ns
		t_h	0.834	0.872	1.277	1.411	1.557	1.489	1.775	1.420	1.565	1.502	1.810	ns
	GCLK PLL	t_{su}	1.123	1.136	1.802	2.031	2.244	2.131	2.137	2.041	2.255	2.140	2.186	ns
		t_h	-0.872	-0.870	-1.404	-1.584	-1.746	-1.661	-1.661	-1.586	-1.749	-1.661	-1.709	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{su}	-0.717	-0.740	-1.091	-1.204	-1.329	-1.272	-1.559	-1.205	-1.329	-1.275	-1.595	ns
		t_h	0.834	0.872	1.277	1.411	1.557	1.489	1.775	1.420	1.565	1.502	1.810	ns
	GCLK PLL	t_{su}	1.123	1.136	1.802	2.031	2.244	2.131	2.137	2.041	2.255	2.140	2.186	ns
		t_h	-0.872	-0.870	-1.404	-1.584	-1.746	-1.661	-1.661	-1.586	-1.749	-1.661	-1.709	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{su}	-0.724	-0.746	-1.103	-1.209	-1.329	-1.274	-1.558	-1.209	-1.324	-1.273	-1.591	ns
		t_h	0.841	0.878	1.290	1.419	1.560	1.492	1.779	1.427	1.565	1.501	1.811	ns
	GCLK PLL	t_{su}	1.116	1.130	1.790	2.026	2.244	2.129	2.138	2.037	2.260	2.142	2.190	ns
		t_h	-0.865	-0.864	-1.391	-1.576	-1.743	-1.658	-1.657	-1.579	-1.749	-1.662	-1.708	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{su}	-0.724	-0.746	-1.103	-1.209	-1.329	-1.274	-1.558	-1.209	-1.324	-1.273	-1.591	ns
		t_h	0.841	0.878	1.290	1.419	1.560	1.492	1.779	1.427	1.565	1.501	1.811	ns
	GCLK PLL	t_{su}	1.116	1.130	1.790	2.026	2.244	2.129	2.138	2.037	2.260	2.142	2.190	ns
		t_h	-0.865	-0.864	-1.391	-1.576	-1.743	-1.658	-1.657	-1.579	-1.749	-1.662	-1.708	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{su}	-0.697	-0.717	-1.072	-1.182	-1.294	-1.237	-1.524	-1.183	-1.296	-1.242	-1.562	ns
		t_h	0.814	0.849	1.257	1.389	1.522	1.454	1.740	1.398	1.532	1.469	1.777	ns
	GCLK PLL	t_{su}	1.143	1.159	1.821	2.053	2.279	2.166	2.172	2.063	2.288	2.173	2.219	ns
		t_h	-0.892	-0.893	-1.424	-1.606	-1.781	-1.696	-1.696	-1.608	-1.782	-1.694	-1.742	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{su}	-0.697	-0.717	-1.072	-1.182	-1.294	-1.237	-1.524	-1.183	-1.296	-1.242	-1.562	ns
		t_h	0.814	0.849	1.257	1.389	1.522	1.454	1.740	1.398	1.532	1.469	1.777	ns
	GCLK PLL	t_{su}	1.143	1.159	1.821	2.053	2.279	2.166	2.172	2.063	2.288	2.173	2.219	ns
		t_h	-0.892	-0.893	-1.424	-1.606	-1.781	-1.696	-1.696	-1.608	-1.782	-1.694	-1.742	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{su}	-0.705	-0.729	-1.082	-1.193	-1.310	-1.253	-1.540	-1.194	-1.311	-1.257	-1.577	ns
		t_h	0.822	0.861	1.267	1.400	1.538	1.470	1.756	1.409	1.547	1.484	1.792	ns
	GCLK PLL	t_{su}	1.135	1.147	1.811	2.042	2.263	2.150	2.156	2.052	2.273	2.158	2.204	ns
		t_h	-0.884	-0.881	-1.414	-1.595	-1.765	-1.680	-1.680	-1.597	-1.767	-1.679	-1.727	ns

Table 1–60 lists the EP3SL70 row pin delay adders when using the regional clock.

Table 1–60. EP3SL70 Row Pin Delay Adders for Regional Clock

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
RCLK input adder	0.111	0.123	0.177	0.192	0.207	0.198	0.263	0.194	0.212	0.201	0.266	ns
RCLK PLL input adder	0.099	0.105	0.156	0.175	0.195	0.185	0.263	0.177	0.195	0.188	0.263	ns
RCLK output adder	-0.113	-0.127	-0.183	-0.198	-0.213	-0.205	-0.272	-0.202	-0.216	-0.21	-0.273	ns
RCLK PLL output adder	-0.107	-0.112	-0.164	-0.185	-0.202	-0.193	-0.258	-0.184	-0.204	-0.197	-0.257	ns

EP3SL110 I/O Timing Parameters

Table 1–61 through Table 1–65 list the maximum I/O timing parameters for EP3SL110 devices for single-ended I/O standards.

Table 1–61 lists the EP3SL110 column pins input timing parameters for single-ended I/O standards.

Table 1–61. EP3SL110 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
3.3-V LVTTL	GCLK	t_{su}	-0.917	-0.917	-1.333	-1.452	-1.682	-1.627	-1.980	-1.452	-1.682	-1.627	-1.980	ns
		t_h	1.053	1.053	1.524	1.667	1.918	1.850	2.205	1.667	1.918	1.850	2.205	ns
	GCLK PLL	t_{su}	-1.234	-1.176	-1.704	-1.940	-2.210	-2.135	-2.470	-1.940	-2.210	-2.135	-2.470	ns
		t_h	1.512	1.460	2.116	2.394	2.710	2.610	2.971	2.394	2.710	2.610	2.971	ns
3.3-V LVCMOS	GCLK	t_{su}	-0.917	-0.917	-1.333	-1.452	-1.682	-1.627	-1.980	-1.452	-1.682	-1.627	-1.980	ns
		t_h	1.053	1.053	1.524	1.667	1.918	1.850	2.205	1.667	1.918	1.850	2.205	ns
	GCLK PLL	t_{su}	-1.234	-1.176	-1.704	-1.940	-2.210	-2.135	-2.470	-1.940	-2.210	-2.135	-2.470	ns
		t_h	1.512	1.460	2.116	2.394	2.710	2.610	2.971	2.394	2.710	2.610	2.971	ns
3.0-V LVTTL	GCLK	t_{su}	-0.928	-0.928	-1.332	-1.454	-1.681	-1.626	-1.979	-1.454	-1.681	-1.626	-1.979	ns
		t_h	1.064	1.064	1.523	1.669	1.917	1.849	2.204	1.669	1.917	1.849	2.204	ns
	GCLK PLL	t_{su}	-1.245	-1.187	-1.703	-1.942	-2.209	-2.134	-2.469	-1.942	-2.209	-2.134	-2.469	ns
		t_h	1.523	1.471	2.115	2.396	2.709	2.609	2.970	2.396	2.709	2.609	2.970	ns
3.0-V LVCMOS	GCLK	t_{su}	-0.928	-0.928	-1.332	-1.454	-1.681	-1.626	-1.979	-1.454	-1.681	-1.626	-1.979	ns
		t_h	1.064	1.064	1.523	1.669	1.917	1.849	2.204	1.669	1.917	1.849	2.204	ns
	GCLK PLL	t_{su}	-1.245	-1.187	-1.703	-1.942	-2.209	-2.134	-2.469	-1.942	-2.209	-2.134	-2.469	ns
		t_h	1.523	1.471	2.115	2.396	2.709	2.609	2.970	2.396	2.709	2.609	2.970	ns
2.5 V	GCLK	t_{su}	-0.923	-0.923	-1.341	-1.466	-1.700	-1.645	-1.998	-1.466	-1.700	-1.645	-1.998	ns
		t_h	1.059	1.059	1.532	1.681	1.936	1.868	2.223	1.681	1.936	1.868	2.223	ns
	GCLK PLL	t_{su}	-1.240	-1.182	-1.712	-1.954	-2.228	-2.153	-2.488	-1.954	-2.228	-2.153	-2.488	ns
		t_h	1.518	1.466	2.124	2.408	2.728	2.628	2.989	2.408	2.728	2.628	2.989	ns

Table 1–63. EP3SL110 Column Pins Output Timing Parameters (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
1.5-V HSTL CLASS II	16mA	GCLK	t_{co}	3.267	3.267	4.605	4.987	5.483	5.352	5.646	4.987	5.483	5.352	5.646	ns
		GCLK PLL	t_{co}	3.657	3.657	5.181	5.620	6.171	6.013	6.395	5.620	6.171	6.013	6.395	ns
1.2-V HSTL CLASS I	4mA	GCLK	t_{co}	3.286	3.286	4.642	5.028	5.529	5.398	5.692	5.028	5.529	5.398	5.692	ns
		GCLK PLL	t_{co}	3.676	3.676	5.217	5.661	6.217	6.059	6.441	5.661	6.217	6.059	6.441	ns
	6mA	GCLK	t_{co}	3.278	3.278	4.633	5.019	5.520	5.389	5.683	5.019	5.520	5.389	5.683	ns
		GCLK PLL	t_{co}	3.668	3.668	5.208	5.652	6.208	6.050	6.432	5.652	6.208	6.050	6.432	ns
	8mA	GCLK	t_{co}	3.279	3.279	4.640	5.028	5.529	5.398	5.692	5.028	5.529	5.398	5.692	ns
		GCLK PLL	t_{co}	3.669	3.669	5.216	5.660	6.217	6.059	6.441	5.660	6.217	6.059	6.441	ns
	10mA	GCLK	t_{co}	3.268	3.268	4.627	5.014	5.515	5.384	5.678	5.014	5.515	5.384	5.678	ns
		GCLK PLL	t_{co}	3.658	3.658	5.203	5.647	6.203	6.045	6.427	5.647	6.203	6.045	6.427	ns
	12mA	GCLK	t_{co}	3.268	3.268	4.627	5.014	5.516	5.385	5.679	5.014	5.516	5.385	5.679	ns
		GCLK PLL	t_{co}	3.658	3.658	5.203	5.647	6.204	6.046	6.428	5.647	6.204	6.046	6.428	ns
1.2-V HSTL CLASS II	16mA	GCLK	t_{co}	3.289	3.289	4.643	5.029	5.529	5.398	5.692	5.029	5.529	5.398	5.692	ns
		GCLK PLL	t_{co}	3.679	3.679	5.219	5.662	6.217	6.059	6.441	5.662	6.217	6.059	6.441	ns
3.0-V PCI	—	GCLK	t_{co}	3.392	3.392	4.688	5.063	5.554	5.423	5.717	5.063	5.554	5.423	5.717	ns
		GCLK PLL	t_{co}	3.782	3.782	5.264	5.696	6.242	6.084	6.466	5.696	6.242	6.084	6.466	ns
3.0-V PCI-X	—	GCLK	t_{co}	3.392	3.392	4.688	5.063	5.554	5.423	5.717	5.063	5.554	5.423	5.717	ns
		GCLK PLL	t_{co}	3.782	3.782	5.264	5.696	6.242	6.084	6.466	5.696	6.242	6.084	6.466	ns

Table 1–73. EP3SL150 Column Pins Output Timing Parameters (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
SSTL-15 CLASS II	8mA	GCLK	t_{co}	3.251	3.268	4.617	4.983	5.486	5.334	5.669	4.983	5.486	5.334	5.669	ns
		GCLK PLL	t_{co}	3.674	3.670	5.204	5.648	6.202	6.022	6.404	5.648	6.202	6.022	6.404	ns
	16mA	GCLK	t_{co}	3.254	3.271	4.624	4.992	5.497	5.345	5.680	4.992	5.497	5.345	5.680	ns
		GCLK PLL	t_{co}	3.677	3.673	5.211	5.657	6.213	6.033	6.415	5.657	6.213	6.033	6.415	ns
1.8-V HSTL CLASS I	4mA	GCLK	t_{co}	3.261	3.278	4.619	4.983	5.484	5.332	5.667	4.983	5.484	5.332	5.667	ns
		GCLK PLL	t_{co}	3.684	3.680	5.206	5.648	6.200	6.020	6.402	5.648	6.200	6.020	6.402	ns
	6mA	GCLK	t_{co}	3.254	3.271	4.617	4.982	5.483	5.331	5.666	4.982	5.483	5.331	5.666	ns
		GCLK PLL	t_{co}	3.677	3.673	5.204	5.647	6.199	6.019	6.401	5.647	6.199	6.019	6.401	ns
	8mA	GCLK	t_{co}	3.246	3.263	4.609	4.974	5.476	5.324	5.659	4.974	5.476	5.324	5.659	ns
		GCLK PLL	t_{co}	3.669	3.665	5.196	5.639	6.192	6.012	6.394	5.639	6.192	6.012	6.394	ns
	10mA	GCLK	t_{co}	3.249	3.266	4.612	4.978	5.480	5.328	5.663	4.978	5.480	5.328	5.663	ns
		GCLK PLL	t_{co}	3.672	3.668	5.199	5.643	6.196	6.016	6.398	5.643	6.196	6.016	6.398	ns
	12mA	GCLK	t_{co}	3.246	3.263	4.615	4.981	5.484	5.332	5.667	4.981	5.484	5.332	5.667	ns
		GCLK PLL	t_{co}	3.669	3.665	5.202	5.646	6.200	6.020	6.402	5.646	6.200	6.020	6.402	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{co}	3.254	3.271	4.614	4.979	5.480	5.328	5.663	4.979	5.480	5.328	5.663	ns
		GCLK PLL	t_{co}	3.677	3.673	5.201	5.644	6.196	6.016	6.398	5.644	6.196	6.016	6.398	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{co}	3.266	3.283	4.627	4.993	5.495	5.343	5.678	4.993	5.495	5.343	5.678	ns
		GCLK PLL	t_{co}	3.689	3.685	5.214	5.658	6.211	6.031	6.413	5.658	6.211	6.031	6.413	ns
	6mA	GCLK	t_{co}	3.262	3.279	4.628	4.995	5.498	5.346	5.681	4.995	5.498	5.346	5.681	ns
		GCLK PLL	t_{co}	3.685	3.681	5.215	5.660	6.214	6.034	6.416	5.660	6.214	6.034	6.416	ns
	8mA	GCLK	t_{co}	3.258	3.275	4.624	4.990	5.493	5.341	5.676	4.990	5.493	5.341	5.676	ns
		GCLK PLL	t_{co}	3.681	3.677	5.211	5.655	6.209	6.029	6.411	5.655	6.209	6.029	6.411	ns
	10mA	GCLK	t_{co}	3.251	3.268	4.617	4.983	5.486	5.334	5.669	4.983	5.486	5.334	5.669	ns
		GCLK PLL	t_{co}	3.674	3.670	5.204	5.648	6.202	6.022	6.404	5.648	6.202	6.022	6.404	ns
	12mA	GCLK	t_{co}	3.252	3.269	4.624	4.991	5.496	5.344	5.679	4.991	5.496	5.344	5.679	ns
		GCLK PLL	t_{co}	3.675	3.671	5.211	5.656	6.212	6.032	6.414	5.656	6.212	6.032	6.414	ns

Table 1–78. EP3SL150 Row Pins Output Timing Parameters (Part 3 of 3)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{co}	3.151	3.396	4.805	5.209	5.720	5.584	5.839	5.335	5.849	5.712	5.915	ns
		GCLK PLL	t_{co}	1.371	1.557	2.015	2.118	2.331	2.344	2.347	2.226	2.443	2.453	2.335	ns
	6mA	GCLK	t_{co}	3.136	3.381	4.791	5.194	5.705	5.569	5.824	5.320	5.834	5.697	5.900	ns
		GCLK PLL	t_{co}	1.356	1.542	2.001	2.103	2.316	2.329	2.332	2.211	2.428	2.438	2.320	ns
	8mA	GCLK	t_{co}	3.125	3.370	4.786	5.191	5.702	5.566	5.821	5.317	5.832	5.695	5.898	ns
		GCLK PLL	t_{co}	1.345	1.531	1.996	2.100	2.313	2.326	2.329	2.208	2.426	2.436	2.318	ns
	10mA	GCLK	t_{co}	3.105	3.350	4.763	5.167	5.679	5.543	5.798	5.294	5.808	5.671	5.874	ns
		GCLK PLL	t_{co}	1.325	1.511	1.973	2.076	2.290	2.303	2.306	2.185	2.402	2.412	2.294	ns
	12mA	GCLK	t_{co}	3.102	3.346	4.759	5.164	5.675	5.539	5.794	5.290	5.805	5.668	5.871	ns
		GCLK PLL	t_{co}	1.322	1.507	1.969	2.073	2.286	2.299	2.302	2.181	2.399	2.409	2.291	ns
	8mA	GCLK	t_{co}	3.107	3.350	4.750	5.152	5.661	5.525	5.780	5.277	5.789	5.652	5.855	ns
		GCLK PLL	t_{co}	1.327	1.511	1.960	2.061	2.272	2.285	2.288	2.168	2.383	2.393	2.275	ns
	16mA	GCLK	t_{co}	3.100	3.343	4.749	5.153	5.664	5.528	5.783	5.280	5.794	5.657	5.860	ns
		GCLK PLL	t_{co}	1.320	1.504	1.959	2.062	2.275	2.288	2.291	2.171	2.388	2.398	2.280	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	t_{co}	3.138	3.382	4.787	5.190	5.700	5.564	5.819	5.316	5.829	5.692	5.895	ns
		GCLK PLL	t_{co}	1.358	1.543	1.997	2.099	2.311	2.324	2.327	2.207	2.423	2.433	2.315	ns
	12mA	GCLK	t_{co}	3.120	3.365	4.772	5.175	5.685	5.549	5.804	5.301	5.814	5.677	5.880	ns
		GCLK PLL	t_{co}	1.340	1.526	1.982	2.084	2.296	2.309	2.312	2.192	2.408	2.418	2.300	ns
	16mA	GCLK	t_{co}	3.106	3.349	4.749	5.151	5.660	5.524	5.779	5.277	5.789	5.652	5.855	ns
		GCLK PLL	t_{co}	1.326	1.510	1.959	2.060	2.271	2.284	2.287	2.168	2.383	2.393	2.275	ns

Table 1–83. EP3SL200 Column Pins Output Timing Parameters (Part 6 of 7)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
1.8-V HSTL CLASS I	4mA	GCLK	t_{co}	3.516	3.516	5.153	5.348	5.856	5.713	6.118	5.348	5.856	5.713	6.118	ns
		GCLK PLL	t_{co}	3.915	3.915	5.788	5.988	6.560	6.388	6.875	5.988	6.560	6.388	6.875	ns
	6mA	GCLK	t_{co}	3.509	3.509	5.151	5.346	5.855	5.712	6.117	5.346	5.855	5.712	6.117	ns
		GCLK PLL	t_{co}	3.908	3.908	5.786	5.986	6.559	6.387	6.874	5.986	6.559	6.387	6.874	ns
	8mA	GCLK	t_{co}	3.501	3.501	5.143	5.339	5.848	5.705	6.110	5.339	5.848	5.705	6.110	ns
		GCLK PLL	t_{co}	3.900	3.900	5.778	5.979	6.552	6.380	6.867	5.979	6.552	6.380	6.867	ns
	10mA	GCLK	t_{co}	3.504	3.504	5.146	5.342	5.852	5.709	6.114	5.342	5.852	5.709	6.114	ns
		GCLK PLL	t_{co}	3.903	3.903	5.781	5.982	6.556	6.384	6.871	5.982	6.556	6.384	6.871	ns
	12mA	GCLK	t_{co}	3.501	3.501	5.149	5.346	5.856	5.713	6.118	5.346	5.856	5.713	6.118	ns
		GCLK PLL	t_{co}	3.900	3.900	5.784	5.986	6.560	6.388	6.875	5.986	6.560	6.388	6.875	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{co}	3.509	3.509	5.148	5.343	5.852	5.709	6.114	5.343	5.852	5.709	6.114	ns
		GCLK PLL	t_{co}	3.908	3.908	5.783	5.983	6.556	6.384	6.871	5.983	6.556	6.384	6.871	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{co}	3.521	3.521	5.161	5.358	5.867	5.724	6.129	5.358	5.867	5.724	6.129	ns
		GCLK PLL	t_{co}	3.920	3.920	5.796	5.998	6.571	6.399	6.886	5.998	6.571	6.399	6.886	ns
	6mA	GCLK	t_{co}	3.517	3.517	5.162	5.359	5.870	5.727	6.132	5.359	5.870	5.727	6.132	ns
		GCLK PLL	t_{co}	3.916	3.916	5.797	5.999	6.574	6.402	6.889	5.999	6.574	6.402	6.889	ns
	8mA	GCLK	t_{co}	3.513	3.513	5.158	5.355	5.865	5.722	6.127	5.355	5.865	5.722	6.127	ns
		GCLK PLL	t_{co}	3.912	3.912	5.793	5.995	6.569	6.397	6.884	5.995	6.569	6.397	6.884	ns
	10mA	GCLK	t_{co}	3.506	3.506	5.151	5.348	5.858	5.715	6.120	5.348	5.858	5.715	6.120	ns
		GCLK PLL	t_{co}	3.905	3.905	5.786	5.988	6.562	6.390	6.877	5.988	6.562	6.390	6.877	ns
	12mA	GCLK	t_{co}	3.507	3.507	5.158	5.356	5.868	5.725	6.130	5.356	5.868	5.725	6.130	ns
		GCLK PLL	t_{co}	3.906	3.906	5.793	5.996	6.572	6.400	6.887	5.996	6.572	6.400	6.887	ns
1.5-V HSTL CLASS II	16mA	GCLK	t_{co}	3.505	3.505	5.139	5.334	5.842	5.699	6.104	5.334	5.842	5.699	6.104	ns
		GCLK PLL	t_{co}	3.904	3.904	5.774	5.974	6.546	6.374	6.861	5.974	6.546	6.374	6.861	ns

Table 1–88. EP3SL200 Row Pins Output Timing Parameters (Part 2 of 3)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	t_{co}	3.581	3.866	5.700	5.916	6.490	6.323	6.702	6.068	6.644	6.323	6.702	ns
		GCLK PLL	t_{co}	3.566	3.851	5.686	5.901	6.475	6.308	6.687	6.053	6.629	6.308	6.687	ns
	6mA	GCLK	t_{co}	3.555	3.840	5.681	5.898	6.472	6.305	6.684	6.050	6.627	6.305	6.684	ns
		GCLK PLL	t_{co}	3.535	3.820	5.658	5.874	6.449	6.282	6.661	6.027	6.603	6.282	6.661	ns
	8mA	GCLK	t_{co}	3.532	3.816	5.654	5.871	6.445	6.278	6.657	6.023	6.600	6.278	6.657	ns
		GCLK PLL	t_{co}	3.537	3.820	5.645	5.859	6.431	6.264	6.643	6.010	6.584	6.264	6.643	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{co}	3.530	3.813	5.644	5.860	6.434	6.267	6.646	6.013	6.589	6.267	6.646	ns
		GCLK PLL	t_{co}	3.568	3.852	5.682	5.897	6.470	6.303	6.682	6.049	6.624	6.303	6.682	ns
	6mA	GCLK	t_{co}	3.550	3.835	5.667	5.882	6.455	6.288	6.667	6.034	6.609	6.288	6.667	ns
		GCLK PLL	t_{co}	3.536	3.819	5.644	5.858	6.430	6.263	6.642	6.010	6.584	6.263	6.642	ns
	8mA	GCLK	t_{co}	3.152	3.376	4.936	5.115	5.637	5.478	5.865	5.239	5.762	5.478	5.865	ns
		GCLK PLL	t_{co}	3.536	3.812	5.604	5.814	6.381	6.214	6.593	5.962	6.531	6.214	6.593	ns
	10mA	GCLK	t_{co}	3.518	3.802	5.642	5.860	6.435	6.268	6.647	6.013	6.592	6.268	6.647	ns
		GCLK PLL	t_{co}	3.152	3.376	4.936	5.115	5.637	5.478	5.865	5.239	5.762	5.478	5.865	ns
	12mA	GCLK	t_{co}	3.536	3.812	5.604	5.814	6.381	6.214	6.593	5.962	6.531	6.214	6.593	ns
		GCLK PLL	t_{co}	3.518	3.802	5.642	5.860	6.435	6.268	6.647	6.013	6.592	6.268	6.647	ns
	16mA	GCLK	t_{co}	3.152	3.376	4.936	5.115	5.637	5.478	5.865	5.239	5.762	5.478	5.865	ns
		GCLK PLL	t_{co}	3.536	3.812	5.604	5.814	6.381	6.214	6.593	5.962	6.531	6.214	6.593	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{co}	3.518	3.802	5.642	5.860	6.435	6.268	6.647	6.013	6.592	6.268	6.647	ns
		GCLK PLL	t_{co}	3.562	3.845	5.678	5.894	6.468	6.301	6.680	6.046	6.621	6.301	6.680	ns
	6mA	GCLK	t_{co}	3.548	3.831	5.665	5.881	6.455	6.288	6.667	6.032	6.608	6.288	6.667	ns
		GCLK PLL	t_{co}	3.544	3.827	5.663	5.881	6.456	6.289	6.668	6.032	6.610	6.289	6.668	ns
	8mA	GCLK	t_{co}	3.560	3.842	5.664	5.878	6.450	6.283	6.662	6.029	6.603	6.283	6.662	ns
		GCLK PLL	t_{co}	3.549	3.832	5.660	5.874	6.447	6.280	6.659	6.026	6.600	6.280	6.659	ns

Table 1–95. EP3SL340 Column Pins Input Timing Parameters (Part 2 of 2)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{su}	-1.114	-1.181	-1.806	-1.828	-1.982	-1.910	-2.388	-1.837	-1.986	-1.920	-2.429	ns
		t_h	1.243	1.327	2.025	2.054	2.228	2.145	2.624	2.072	2.241	2.164	2.669	ns
	GCLK PLL	t_{su}	1.021	1.039	1.740	1.829	2.017	1.918	1.791	1.847	2.040	1.934	1.844	ns
		t_h	-0.753	-0.751	-1.283	-1.356	-1.492	-1.422	-1.284	-1.364	-1.504	-1.429	-1.332	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{su}	-1.102	-1.170	-1.797	-1.817	-1.963	-1.891	-2.369	-1.826	-1.968	-1.902	-2.411	ns
		t_h	1.231	1.316	2.016	2.043	2.209	2.126	2.605	2.061	2.223	2.146	2.651	ns
	GCLK PLL	t_{su}	1.033	1.050	1.749	1.840	2.036	1.937	1.810	1.858	2.058	1.952	1.862	ns
		t_h	-0.765	-0.762	-1.292	-1.367	-1.511	-1.441	-1.303	-1.375	-1.522	-1.447	-1.350	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{su}	-1.102	-1.170	-1.797	-1.817	-1.963	-1.891	-2.369	-1.826	-1.968	-1.902	-2.411	ns
		t_h	1.231	1.316	2.016	2.043	2.209	2.126	2.605	2.061	2.223	2.146	2.651	ns
	GCLK PLL	t_{su}	1.033	1.050	1.749	1.840	2.036	1.937	1.810	1.858	2.058	1.952	1.862	ns
		t_h	-0.765	-0.762	-1.292	-1.367	-1.511	-1.441	-1.303	-1.375	-1.522	-1.447	-1.350	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{su}	-1.114	-1.181	-1.806	-1.828	-1.982	-1.910	-2.388	-1.837	-1.986	-1.920	-2.429	ns
		t_h	1.243	1.327	2.025	2.054	2.228	2.145	2.624	2.072	2.241	2.164	2.669	ns
	GCLK PLL	t_{su}	1.021	1.039	1.740	1.829	2.017	1.918	1.791	1.847	2.040	1.934	1.844	ns
		t_h	-0.753	-0.751	-1.283	-1.356	-1.492	-1.422	-1.284	-1.364	-1.504	-1.429	-1.332	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{su}	-1.114	-1.181	-1.806	-1.828	-1.982	-1.910	-2.388	-1.837	-1.986	-1.920	-2.429	ns
		t_h	1.243	1.327	2.025	2.054	2.228	2.145	2.624	2.072	2.241	2.164	2.669	ns
	GCLK PLL	t_{su}	1.021	1.039	1.740	1.829	2.017	1.918	1.791	1.847	2.040	1.934	1.844	ns
		t_h	-0.753	-0.751	-1.283	-1.356	-1.492	-1.422	-1.284	-1.364	-1.504	-1.429	-1.332	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{su}	-1.121	-1.187	-1.818	-1.833	-1.982	-1.912	-2.387	-1.841	-1.981	-1.918	-2.425	ns
		t_h	1.250	1.333	2.038	2.062	2.231	2.148	2.628	2.079	2.241	2.163	2.670	ns
	GCLK PLL	t_{su}	1.014	1.033	1.728	1.824	2.017	1.916	1.792	1.843	2.045	1.936	1.848	ns
		t_h	-0.746	-0.745	-1.270	-1.348	-1.489	-1.419	-1.280	-1.357	-1.504	-1.430	-1.331	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{su}	-1.121	-1.187	-1.818	-1.833	-1.982	-1.912	-2.387	-1.841	-1.981	-1.918	-2.425	ns
		t_h	1.250	1.333	2.038	2.062	2.231	2.148	2.628	2.079	2.241	2.163	2.670	ns
	GCLK PLL	t_{su}	1.014	1.033	1.728	1.824	2.017	1.916	1.792	1.843	2.045	1.936	1.848	ns
		t_h	-0.746	-0.745	-1.270	-1.348	-1.489	-1.419	-1.280	-1.357	-1.504	-1.430	-1.331	ns

EP3SE80 I/O Timing Parameters

Table 1–111 through Table 1–114 list the maximum I/O timing parameters for EP3SE80 devices for single-ended I/O standards.

Table 1–111 lists the EP3SE80 column pins input timing parameters for single-ended I/O standards.

Table 1–111. EP3SE80 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
3.3-V LVTTL	GCLK	t_{su}	-1.054	-1.054	-1.505	-1.636	-1.872	-1.819	-2.173	-1.636	-1.872	-1.819	-2.173	ns
		t_h	1.195	1.195	1.704	1.861	2.117	2.050	2.409	1.861	2.117	2.050	2.409	ns
	GCLK PLL	t_{su}	-1.307	-1.307	-1.870	-2.028	-2.321	-2.214	-2.661	-2.028	-2.321	-2.214	-2.661	ns
		t_h	1.605	1.605	2.302	2.513	2.858	2.721	3.186	2.513	2.858	2.721	3.186	ns
3.3-V LVCMOS	GCLK	t_{su}	-1.054	-1.054	-1.505	-1.636	-1.872	-1.819	-2.173	-1.636	-1.872	-1.819	-2.173	ns
		t_h	1.195	1.195	1.704	1.861	2.117	2.050	2.409	1.861	2.117	2.050	2.409	ns
	GCLK PLL	t_{su}	-1.307	-1.307	-1.870	-2.028	-2.321	-2.214	-2.661	-2.028	-2.321	-2.214	-2.661	ns
		t_h	1.605	1.605	2.302	2.513	2.858	2.721	3.186	2.513	2.858	2.721	3.186	ns
3.0-V LVTTL	GCLK	t_{su}	-1.065	-1.065	-1.504	-1.638	-1.871	-1.818	-2.172	-1.638	-1.871	-1.818	-2.172	ns
		t_h	1.206	1.206	1.703	1.863	2.116	2.049	2.408	1.863	2.116	2.049	2.408	ns
	GCLK PLL	t_{su}	-1.318	-1.318	-1.869	-2.030	-2.320	-2.213	-2.660	-2.030	-2.320	-2.213	-2.660	ns
		t_h	1.616	1.616	2.301	2.515	2.857	2.720	3.185	2.515	2.857	2.720	3.185	ns
3.0-V LVCMOS	GCLK	t_{su}	-1.065	-1.065	-1.504	-1.638	-1.871	-1.818	-2.172	-1.638	-1.871	-1.818	-2.172	ns
		t_h	1.206	1.206	1.703	1.863	2.116	2.049	2.408	1.863	2.116	2.049	2.408	ns
	GCLK PLL	t_{su}	-1.318	-1.318	-1.869	-2.030	-2.320	-2.213	-2.660	-2.030	-2.320	-2.213	-2.660	ns
		t_h	1.616	1.616	2.301	2.515	2.857	2.720	3.185	2.515	2.857	2.720	3.185	ns
2.5 V	GCLK	t_{su}	-1.060	-1.060	-1.513	-1.650	-1.890	-1.837	-2.191	-1.650	-1.890	-1.837	-2.191	ns
		t_h	1.201	1.201	1.712	1.875	2.135	2.068	2.427	1.875	2.135	2.068	2.427	ns
	GCLK PLL	t_{su}	-1.313	-1.313	-1.878	-2.042	-2.339	-2.232	-2.679	-2.042	-2.339	-2.232	-2.679	ns
		t_h	1.611	1.611	2.310	2.527	2.876	2.739	3.204	2.527	2.876	2.739	3.204	ns
1.8 V	GCLK	t_{su}	-1.082	-1.082	-1.553	-1.686	-1.888	-1.835	-2.189	-1.686	-1.888	-1.835	-2.189	ns
		t_h	1.225	1.225	1.752	1.911	2.133	2.066	2.425	1.911	2.133	2.066	2.425	ns
	GCLK PLL	t_{su}	-1.335	-1.335	-1.918	-2.078	-2.337	-2.230	-2.677	-2.078	-2.337	-2.230	-2.677	ns
		t_h	1.635	1.635	2.350	2.563	2.874	2.737	3.202	2.563	2.874	2.737	3.202	ns
1.5 V	GCLK	t_{su}	-1.072	-1.072	-1.530	-1.654	-1.818	-1.765	-2.119	-1.654	-1.818	-1.765	-2.119	ns
		t_h	1.215	1.215	1.729	1.879	2.063	1.996	2.355	1.879	2.063	1.996	2.355	ns
	GCLK PLL	t_{su}	-1.325	-1.325	-1.895	-2.046	-2.267	-2.160	-2.607	-2.046	-2.267	-2.160	-2.607	ns
		t_h	1.625	1.625	2.327	2.531	2.804	2.667	3.132	2.531	2.804	2.667	3.132	ns
1.2 V	GCLK	t_{su}	-1.020	-1.020	-1.453	-1.555	-1.662	-1.609	-1.963	-1.555	-1.662	-1.609	-1.963	ns
		t_h	1.163	1.163	1.652	1.780	1.907	1.840	2.199	1.780	1.907	1.840	2.199	ns
	GCLK PLL	t_{su}	-1.273	-1.273	-1.818	-1.947	-2.111	-2.004	-2.451	-1.947	-2.111	-2.004	-2.451	ns
		t_h	1.573	1.573	2.250	2.432	2.648	2.511	2.976	2.432	2.648	2.511	2.976	ns

Table 1–124. EP3SE110 Row Pins Output Timing Parameters (Part 3 of 5)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
1.5 V	2mA	GCLK	t_{co}	3.369	3.648	5.244	5.703	6.278	6.148	6.428	5.838	6.417	6.289	6.524	ns
		GCLK PLL	t_{co}	1.574	1.792	2.430	2.582	2.857	2.877	2.882	2.699	2.980	2.999	2.891	ns
	4mA	GCLK	t_{co}	3.127	3.390	4.839	5.266	5.787	5.657	5.937	5.392	5.913	5.785	6.020	ns
		GCLK PLL	t_{co}	1.332	1.534	2.025	2.145	2.366	2.386	2.391	2.253	2.476	2.495	2.387	ns
	6mA	GCLK	t_{co}	3.100	3.343	4.766	5.170	5.691	5.551	5.834	5.294	5.816	5.685	5.916	ns
		GCLK PLL	t_{co}	1.305	1.487	1.952	2.049	2.260	2.280	2.285	2.155	2.371	2.390	2.282	ns
	8mA	GCLK	t_{co}	3.091	3.334	4.744	5.152	5.672	5.532	5.815	5.276	5.797	5.666	5.897	ns
		GCLK PLL	t_{co}	1.296	1.478	1.930	2.031	2.241	2.261	2.266	2.137	2.349	2.368	2.260	ns
1.2 V	2mA	GCLK	t_{co}	3.312	3.573	5.154	5.617	6.203	6.073	6.353	5.750	6.333	6.205	6.440	ns
		GCLK PLL	t_{co}	1.517	1.717	2.340	2.496	2.782	2.802	2.807	2.611	2.896	2.915	2.807	ns
	4mA	GCLK	t_{co}	3.132	3.384	4.861	5.294	5.828	5.698	5.978	5.417	5.955	5.827	6.062	ns
		GCLK PLL	t_{co}	1.337	1.528	2.047	2.173	2.407	2.427	2.432	2.278	2.518	2.537	2.429	ns
SSTL-2 CLASS I	8mA	GCLK	t_{co}	3.057	3.295	4.657	5.045	5.571	5.411	5.718	5.165	5.692	5.561	5.795	ns
		GCLK PLL	t_{co}	1.261	1.464	1.868	1.951	2.126	2.146	2.147	2.033	2.230	2.250	2.137	ns
	12mA	GCLK	t_{co}	3.052	3.291	4.654	5.043	5.569	5.409	5.716	5.164	5.691	5.560	5.794	ns
		GCLK PLL	t_{co}	1.249	1.460	1.865	1.949	2.118	2.138	2.139	2.025	2.223	2.243	2.130	ns
SSTL-2 CLASS II	16mA	GCLK	t_{co}	3.043	3.280	4.639	5.027	5.552	5.392	5.699	5.147	5.673	5.542	5.776	ns
		GCLK PLL	t_{co}	1.234	1.449	1.850	1.933	2.097	2.111	2.112	1.999	2.202	2.221	2.103	ns
SSTL-18 CLASS I	4mA	GCLK	t_{co}	3.069	3.308	4.672	5.065	5.586	5.433	5.729	5.184	5.707	5.576	5.807	ns
		GCLK PLL	t_{co}	1.274	1.452	1.858	1.944	2.142	2.162	2.167	2.045	2.246	2.265	2.157	ns
	6mA	GCLK	t_{co}	3.054	3.294	4.669	5.063	5.585	5.431	5.728	5.182	5.705	5.574	5.805	ns
		GCLK PLL	t_{co}	1.259	1.438	1.855	1.942	2.140	2.160	2.165	2.043	2.244	2.263	2.155	ns
	8mA	GCLK	t_{co}	3.043	3.282	4.652	5.046	5.575	5.414	5.718	5.165	5.696	5.565	5.796	ns
		GCLK PLL	t_{co}	1.248	1.426	1.838	1.925	2.123	2.143	2.148	2.026	2.228	2.247	2.139	ns
	10mA	GCLK	t_{co}	3.030	3.267	4.636	5.030	5.562	5.399	5.705	5.150	5.684	5.553	5.784	ns
		GCLK PLL	t_{co}	1.228	1.404	1.822	1.909	2.108	2.128	2.133	2.011	2.213	2.232	2.124	ns
	12mA	GCLK	t_{co}	3.030	3.266	4.635	5.029	5.562	5.398	5.705	5.149	5.684	5.553	5.784	ns
		GCLK PLL	t_{co}	1.228	1.403	1.821	1.908	2.107	2.127	2.132	2.010	2.213	2.232	2.123	ns

Table 1–126. EP3SE110 Row Pins Input Timing Parameters (Part 2 of 3)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{su}	-0.758	-0.806	-1.154	-1.254	-1.359	-1.307	-1.649	-1.255	-1.360	-1.309	-1.693	ns
		t_h	0.884	0.948	1.354	1.478	1.603	1.540	1.883	1.488	1.613	1.551	1.928	ns
	GCLK PLL	t_{su}	1.147	1.162	1.855	2.094	2.328	2.208	2.147	2.111	2.346	2.224	2.194	ns
		t_h	-0.884	-0.882	-1.438	-1.629	-1.812	-1.720	-1.650	-1.635	-1.818	-1.725	-1.693	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{su}	-0.758	-0.806	-1.154	-1.254	-1.359	-1.307	-1.649	-1.255	-1.360	-1.309	-1.693	ns
		t_h	0.884	0.948	1.354	1.478	1.603	1.540	1.883	1.488	1.613	1.551	1.928	ns
	GCLK PLL	t_{su}	1.147	1.162	1.855	2.094	2.328	2.208	2.147	2.111	2.346	2.224	2.194	ns
		t_h	-0.884	-0.882	-1.438	-1.629	-1.812	-1.720	-1.650	-1.635	-1.818	-1.725	-1.693	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{su}	-0.772	-0.818	-1.163	-1.264	-1.377	-1.325	-1.667	-1.266	-1.377	-1.326	-1.710	ns
		t_h	0.898	0.960	1.364	1.488	1.621	1.558	1.901	1.499	1.630	1.568	1.945	ns
	GCLK PLL	t_{su}	1.133	1.150	1.842	2.084	2.310	2.190	2.129	2.100	2.329	2.207	2.177	ns
		t_h	-0.870	-0.870	-1.426	-1.619	-1.794	-1.702	-1.632	-1.624	-1.801	-1.708	-1.676	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{su}	-0.772	-0.818	-1.163	-1.264	-1.377	-1.325	-1.667	-1.266	-1.377	-1.326	-1.710	ns
		t_h	0.898	0.960	1.364	1.488	1.621	1.558	1.901	1.499	1.630	1.568	1.945	ns
	GCLK PLL	t_{su}	1.133	1.150	1.842	2.084	2.310	2.190	2.129	2.100	2.329	2.207	2.177	ns
		t_h	-0.870	-0.870	-1.426	-1.619	-1.794	-1.702	-1.632	-1.624	-1.801	-1.708	-1.676	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{su}	-0.758	-0.806	-1.154	-1.254	-1.359	-1.307	-1.649	-1.255	-1.360	-1.309	-1.693	ns
		t_h	0.884	0.948	1.354	1.478	1.603	1.540	1.883	1.488	1.613	1.551	1.928	ns
	GCLK PLL	t_{su}	1.147	1.162	1.855	2.094	2.328	2.208	2.147	2.111	2.346	2.224	2.194	ns
		t_h	-0.884	-0.882	-1.438	-1.629	-1.812	-1.720	-1.650	-1.635	-1.818	-1.725	-1.693	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{su}	-0.758	-0.806	-1.154	-1.254	-1.359	-1.307	-1.649	-1.255	-1.360	-1.309	-1.693	ns
		t_h	0.884	0.948	1.354	1.478	1.603	1.540	1.883	1.488	1.613	1.551	1.928	ns
	GCLK PLL	t_{su}	1.147	1.162	1.855	2.094	2.328	2.208	2.147	2.111	2.346	2.224	2.194	ns
		t_h	-0.884	-0.882	-1.438	-1.629	-1.812	-1.720	-1.650	-1.635	-1.818	-1.725	-1.693	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{su}	-0.772	-0.818	-1.163	-1.264	-1.377	-1.325	-1.667	-1.266	-1.377	-1.326	-1.710	ns
		t_h	0.898	0.960	1.364	1.488	1.621	1.558	1.901	1.499	1.630	1.568	1.945	ns
	GCLK PLL	t_{su}	1.133	1.150	1.842	2.084	2.310	2.190	2.129	2.100	2.329	2.207	2.177	ns
		t_h	-0.870	-0.870	-1.426	-1.619	-1.794	-1.702	-1.632	-1.624	-1.801	-1.708	-1.676	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{su}	-0.772	-0.818	-1.163	-1.264	-1.377	-1.325	-1.667	-1.266	-1.377	-1.326	-1.710	ns
		t_h	0.898	0.960	1.364	1.488	1.621	1.558	1.901	1.499	1.630	1.568	1.945	ns
	GCLK PLL	t_{su}	1.133	1.150	1.842	2.084	2.310	2.190	2.129	2.100	2.329	2.207	2.177	ns
		t_h	-0.870	-0.870	-1.426	-1.619	-1.794	-1.702	-1.632	-1.624	-1.801	-1.708	-1.676	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{su}	-0.781	-0.827	-1.178	-1.275	-1.384	-1.333	-1.673	-1.273	-1.378	-1.329	-1.712	ns
		t_h	0.907	0.969	1.379	1.502	1.631	1.568	1.912	1.509	1.636	1.573	1.952	ns
	GCLK PLL	t_{su}	1.124	1.141	1.827	2.068	2.299	2.178	2.118	2.089	2.323	2.199	2.170	ns
		t_h	-0.861	-0.861	-1.411	-1.601	-1.780	-1.688	-1.617	-1.610	-1.792	-1.699	-1.665	ns

EP3SL70 Clock Timing Parameters

Table 1–148 and Table 1–149 list the global clock timing specifications for EP3SL70 devices.

Table 1–148. EP3SL70 Column Pin Global Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.749	1.735	2.434	2.702	3.056	2.950	3.403	2.702	3.056	2.950	3.403	ns
t_{COUT}	1.749	1.735	2.434	2.702	3.056	2.950	3.403	2.702	3.056	2.950	3.403	ns
t_{PLLCIN}	-0.012	-0.021	-0.255	-0.306	-0.251	-0.203	-0.044	-0.306	0.161	-0.203	-0.044	ns
$t_{PLLCOUT}$	-0.012	-0.021	-0.255	-0.306	-0.251	-0.203	-0.044	-0.306	0.161	-0.203	-0.044	ns

Table 1–149. EP3SL70 Row Pin Global Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.732	1.840	2.524	2.758	3.083	2.986	3.227	2.811	3.157	3.042	3.260	ns
t_{COUT}	1.650	1.749	2.382	2.595	2.902	2.815	3.068	2.641	2.968	2.863	3.101	ns
t_{PLLCIN}	0.051	0.115	-0.144	-0.219	-0.193	-0.144	-0.188	-0.170	0.275	-0.097	-0.234	ns
$t_{PLLCOUT}$	-0.031	0.024	-0.286	-0.382	-0.374	-0.315	-0.347	-0.340	0.086	-0.276	-0.393	ns

Table 1–150 and Table 1–151 list the regional clock timing parameters for EP3SL70 devices.

Table 1–150. EP3SL70 Column Pin Regional Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.689	1.689	2.388	2.649	3.004	2.723	3.132	2.649	3.014	2.723	3.132	ns
t_{COUT}	1.689	1.689	2.388	2.649	3.004	2.723	3.132	2.649	3.014	2.723	3.132	ns
t_{PLLCIN}	-0.011	-0.022	-0.261	-0.308	-0.256	-0.207	-0.054	-0.308	0.224	-0.207	-0.054	ns
$t_{PLLCOUT}$	-0.011	-0.022	-0.261	-0.308	-0.256	-0.207	-0.054	-0.308	0.224	-0.207	-0.054	ns

Table 1–151. EP3SL70 Row Pin Regional Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.637	1.726	2.353	2.566	2.885	2.786	2.964	2.625	2.948	2.839	3.001	ns
t_{COUT}	1.555	1.635	2.211	2.403	2.704	2.615	2.805	2.455	2.759	2.660	2.842	ns
t_{PLLCIN}	0.018	0.085	-0.176	-0.252	-0.230	-0.180	-0.226	-0.203	0.307	-0.139	-0.272	ns
$t_{PLLCOUT}$	-0.064	-0.006	-0.318	-0.415	-0.411	-0.351	-0.385	-0.373	0.118	-0.318	-0.431	ns

Table 1–176 and Table 1–177 list the periphery clock timing parameters for EP3SL340 devices.

Table 1–176. EP3SL340 Column Pin Periphery Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.778	1.760	2.687	2.847	3.240	3.099	3.718	2.847	3.240	3.099	3.718	ns
t_{COUT}	1.778	1.760	2.687	2.847	3.240	3.099	3.718	2.847	3.240	3.099	3.718	ns
t_{PLLCIN}	0.086	0.061	-0.164	-0.161	-0.140	-0.097	0.101	-0.161	-0.140	-0.097	0.101	ns
$t_{PLLCOUT}$	0.086	0.061	-0.164	-0.161	-0.140	-0.097	0.101	-0.161	-0.140	-0.097	0.101	ns

Table 1–177. EP3SL340 Row Pin Periphery Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.524	1.616	2.435	2.567	2.958	2.823	3.141	2.605	3.002	2.861	3.165	ns
t_{COUT}	1.442	1.525	2.280	2.404	2.777	2.652	2.982	2.435	2.813	2.682	3.006	ns
t_{PLLCIN}	0.116	0.211	-0.039	-0.116	-0.055	-0.030	-0.051	-0.040	-0.006	0.050	-0.098	ns
$t_{PLLCOUT}$	0.034	0.120	-0.191	-0.279	-0.236	-0.201	-0.210	-0.210	-0.195	-0.129	-0.257	ns

EP3SE50 Clock Timing Parameters

Table 1–178 and Table 1–179 list the global clock timing parameters for EP3SE50 devices.

Table 1–178. EP3SE50 Column Pin Global Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.786	1.789	2.495	2.748	3.111	2.993	3.489	2.748	3.105	2.993	3.489	ns
t_{COUT}	1.786	1.789	2.495	2.748	3.111	2.993	3.489	2.748	3.105	2.993	3.489	ns
t_{PLLCIN}	0.023	0.027	-0.204	-0.268	-0.226	-0.180	0.025	-0.268	0.249	-0.180	0.025	ns
$t_{PLLCOUT}$	0.083	0.103	-0.068	-0.131	-0.226	-0.010	0.025	-0.131	0.249	-0.010	0.025	ns

Table 1–179. EP3SE50 Row Pin Global Clock Timing Specifications

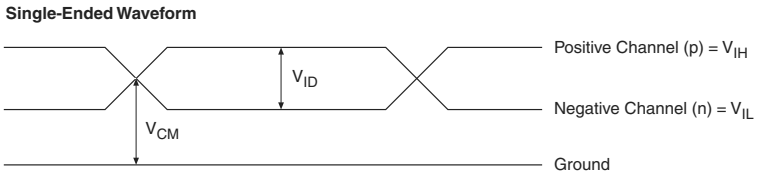
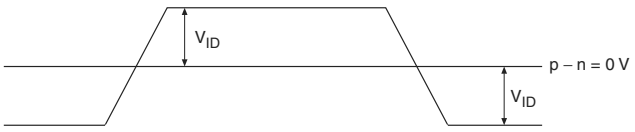
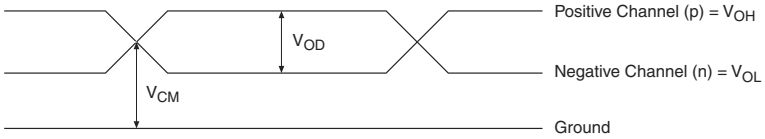
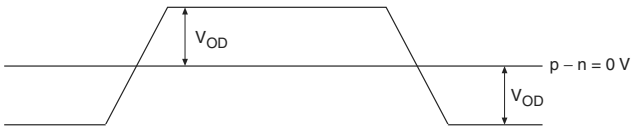
Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.739	1.849	2.536	2.769	3.112	3.010	3.250	2.830	3.171	3.069	3.276	ns
t_{COUT}	1.657	1.758	2.394	2.606	2.931	2.839	3.091	2.660	2.982	2.890	3.117	ns
t_{PLLCIN}	0.044	0.117	-0.143	-0.220	-0.183	-0.135	-0.189	-0.171	0.345	-0.088	-0.242	ns
$t_{PLLCOUT}$	-0.038	0.026	-0.285	-0.383	-0.364	-0.306	-0.348	-0.341	0.156	-0.267	-0.401	ns

Glossary

The following table lists the glossary for this chapter.

Table 1.

Glossary Table (Part 1 of 4)

Letter	Subject	Definitions
A	—	—
B	—	—
C	—	—
D	Differential I/O Standards	Receiver Input Waveforms **Single-Ended Waveform**  **Differential Waveform**  Transmitter Output Waveforms **Single-Ended Waveform**  **Differential Waveform** 
E	—	—
F	f_{HSCLK}	High-Speed I/O Block: High-speed receiver/transmitter input and output clock frequency.
	f_{HSDR}	High-Speed I/O Block: Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	High-Speed I/O Block: Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
G	—	—
H	—	—
I	—	—