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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3200
Number of Logic Elements/Cells	80000
Total RAM Bits	6843392
Number of I/O	744
Number of Gates	-
Voltage - Supply	0.86V ~ 1.15V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep3se80f1152c4n

Table 1–18. Differential I/O Standard Specifications (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{ID} (V) *(1)*			$V_{ICM(DC)}$ (V)			V_{OD} (V) *(2)*			V_{OCM} (V) *(2)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
2.5 V LVDS (Column I/O)	2.375	2.5	2.625	0.1	V_{CM} = 1.25	—	0.05 *(6)*	$D_{max} \leq 700$ Mbps	1.8 *(6)*	0.247	—	0.6	1.0	1.25	1.5
	2.375	2.5	2.625	0.1	V_{CM} = 1.25	—	1.05 *(6)*	$D_{max} > 700$ Mbps	1.55 *(6)*	0.247	—	0.6	1.0	1.25	1.5
RSDS (Row I/O)	2.375	2.5	2.625	0.1	V_{CM} = 1.25	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
RSDS (Column I/O)	2.375	2.5	2.625	0.1	V_{CM} = 1.25	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.5
Mini-LVDS (Row I/O)	2.375	2.5	2.625	0.2	—	0.6	0.4	—	1.325	0.25	—	0.6	0.5	1.2	1.4
Mini-LVDS (Column I/0)	2.375	2.5	2.625	0.2	—	0.6	0.4	—	1.325	0.25	—	0.6	0.5	1.2	1.5
LVPECL *(3)*	2.375 *(5)*	2.5 *(5)*	2.625 *(5)*	0.3	—	—	0.6	$D_{max} \leq 700$ Mbps	1.8 *(4)*	—	—	—	—	—	—
	2.375 *(5)*	2.5 *(5)*	2.625 *(5)*	0.3	—	—	1.0	$D_{max} > 700$ Mbps	1.6 *(4)*	—	—	—	—	—	—

Notes to Table 1–18:

(1) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(2) RL range: $90 \leq RL \leq 110\ \Omega$.

(3) Column and row I/O banks support LVPECL I/O standards for input operation only on dedicated clock input pins. Differential clock inputs in column I/O use V_{CC_CLKIN} that must be powered by 2.5 V. Differential clock inputs in row I/O banks are powered by V_{CCPD}.

(4) The receiver voltage input range for the data rate when $D_{max} > 700$ Mbps is $0.85\ V \leq V_{IN} \leq 1.75$ V.
The receiver voltage input range for the data rate when $D_{max} \leq 700$ Mbps is $0.45\ V \leq V_{IN} \leq 1.95$ V.

(5) Power supply for the column I/O LVPECL differential clock input buffer is V_{CC_CLKIN}.

(6) The receiver voltage input range for the data rate when $D_{max} > 700$ Mbps is $1.0\ V \leq V_{IN} \leq 1.6$ V.
The receiver voltage input range for the data rate when $D_{max} \leq 700$ Mbps is zero $V \leq V_{IN} \leq 1.85$ V.

Power Consumption

Altera offers two ways to estimate power for a design: the Excel-based Early Power Estimator (EPE) and the Quartus® II **PowerPlay Power Analyzer** feature.

The interactive Excel-based Early Power Estimator is typically used prior to designing the FPGA in order to get a magnitude estimate of the device power. The Quartus II **PowerPlay Power Analyzer** provides estimation based on the specifics of the design after place-and-route is complete. The **PowerPlay Power Analyzer** can apply a combination of user-entered, simulation-derived, and estimated signal activities which, when combined with detailed circuit models, can yield very accurate power estimation.

Refer to Table 1–4 on page 1–5 for supply current estimates for V_{CCPGM} and V_{CC_CLKIN}. Use the EPE and PowerPlay Power Analyzer for current estimates of remaining power supplies.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide For Stratix III FPGAs* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Table 1–22. TriMatrix Memory Block Performance Specifications for Stratix III Devices *(Note 1)* (Part 3 of 3)

Memory Block Type	Mode	ALUTs	TriMatrix Memory	C2 *(6)*	C3	C4	C4L		I3	I4	I4L	Unit
				V_{CCL} = 1.1 V	V_{CCL} = 1.1 V	V_{CCL} = 1.1 V	V_{CCL} = 1.1 V	V_{CCL} = 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
M144K *(3), (5)*	Simple dual-port 2K × 64 (with ECC)	0	1	255	210	180	180	130	195	180	120	MHz
	Min Pulse Width (Clock High Time)	—	—	800	1000	1100	1100	1800	1000	1100	1800	ps
	Min Pulse Width (Clock Low Time)	—	—	500	625	690	690	1100	625	690	1100	ps

Notes to Table 1–22:

(1) Use a memory block clock that comes through global clock routing from an on-chip PLL set to 50% output duty cycle to achieve the maximum memory block performance. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) The F_{max} shown for M9K degrades 2% when you use the Error Detection CRC feature on the device, except for the C4L speed grade with V_{CCL} = 0.9 V. For the C4L speed grade with V_{CCL} = 0.9V, there is no degradation in F_{max} when you use the Error Detection CRC feature.

(3) The F_{max} shown for M144K degrades 10 MHz when you use byte-enable support on M144K.

(4) F_{max} is applicable when the **COMPTABILITY** option is turned ON.

(5) F_{max} is applicable when the **COMPTABILITY** option is turned OFF. This option is turned ON by default in Quartus II software.

(6) The F_{max} for the EP3SL200, EP3SE260, and EP3SL340 devices at the C2 speed grade is 7% slower than the C2 values shown in the table.

Configuration and JTAG Specifications

Table 1–23 lists the Stratix III configuration mode specifications.

Table 1–23. Configuration Mode Specifications for Stratix III Devices *(Note 1)*

Programming Mode	DCLK F_{max}	Unit
Passive Serial	100	MHz
Fast Passive Parallel *(2)*	100	MHz
Fast Active Serial *(3)*	40	MHz

Notes to Table 1–23:

(1) DCLK F_{max} is restricted when you enable the Remote Update feature. For more information, refer to the *Remote Update Circuitry (ALTREMOTE_UPDATE) Megafunction User Guide*.

(2) The data rate must be 4× slower than the clock when you use decompression and/or encryption.

(3) For more information about the minimum and typical DCLK F_{max} value in Fast Active Serial configuration, refer to the *Configuring Stratix III Devices* chapter.

Table 1–24 lists the JTAG timing parameters and values for Stratix III devices. Refer to the figure for "HIGH-SPEED I/O Block" in the "Glossary" on page 1–326 for the JTAG timing requirements.

Table 1–24. JTAG Timing Parameters and Values for Stratix III Devices

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
t_{JPSU} (TDI)	JTAG port setup time for TDI	1	—	ns
t_{JPSU} (TMS)	JTAG port setup time for TMS	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

Figure 1–3 shows the LVDS Soft-CDR/ DPA sinusoidal jitter tolerance specifications for Stratix III devices.

Figure 1–3. LVDS Soft-CDR/DPA Sinusiodal Jitter Tolerance Specification for Stratix III Devices

Table 1–27 lists the LVDS Soft-CDR/ DPA sinusiodal jitter mask values for Stratix III devices.

Table 1–27. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for Stratix III Devices

Jitter Frequency (Hz)		Jitter Amplitude	Unit
F1	10,000	25.000	UI
F2	17,565	25.000	UI
F3	1,493,000	0.350	UI
F4	50,000,000	0.350	UI

External Memory Interface Specifications

The following sections describe the external memory I/O timing specifications and the DLL and DQS block specifications.

For more information about the maximum clock rate support for external memory interfaces with a half-rate or full-rate controller, refer to *Section III: System Performance Specifications* of the *External Memory Interfaces Handbook*.

External Memory I/O Timing Specifications

Table 1–28 and Table 1–29 list Stratix III device timing uncertainties on the read and write data paths. Use these specifications to determine timing margins for source synchronous paths between the Stratix III FPGA and the external memory device. For more information, refer to the figure for "SW (sampling window)" in the "Glossary" on page 1–326.

Table 1–31 lists the average DQS phase offset delay per setting for Stratix III devices.

Table 1–31. Average DQS Phase Offset Delay per Setting for Stratix III Devices *(Note 1)*, *(2)*, *(3)*

Speed Grade	Min	Typ	Max	Unit
C2	7	10	13	ps
C3, I3	7	11	15	ps
C4, I4	7	11.5	16	ps
C4L, I4L	7	11.5	16	ps

Notes to Table 1–31:

(1) The valid settings for phase offset are -64 to +63 for frequency modes 0 to 3 and -32 to +31 for frequency modes 4 to 6.

(2) The typical value equals the average of the minimum and maximum values.

(3) The delay settings are linear with a cumulative delay variation of ± 20 ps for all speed grades. For example, when using a C2 speed grade and applying 10° phase offset settings to a 90° phase shift at 400 MHz, the expected minimum cumulative delay is [625 ps + (10*7 ps) - 20 ps] = 675 ps.

Table 1–32 lists the DQS phase shift error specification for DLL-delayed clock (t_{DQS_PSERR}) for Stratix III devices.

Table 1–32. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Stratix III Devices *(Note 1)*

Number of DQS Delay Buffer	C2	C3, I3	C4, C4L, I4, I4L	Unit
1	±13	±14	±15	ps
2	±26	±28	±30	ps
3	±39	±42	±45	ps
4	±52	±56	±60	ps

Note to Table 1–32:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a C2 speed grade is ± 39 ps.

Table 1–33 lists the memory output jitter specification for Stratix III devices.

Table 1–33. Memory Output Clock Jitter Specification for Stratix III Devices *(Note 1)*, *(2)*

Parameter	Clock Network	Symbol	C2		C3, I3		C4, I4		C4L, I4L				Unit
			V_{CCL} = 1.1V		V_{CCL} = 1.1V		V_{CCL} = 1.1V		V_{CCL} = 1.1V		V_{CCL} = 0.9V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Clock period jitter	Regional	tJIT(per)	–75	75	–85	85	–100	100	–100	100	–120	120	ps
Cycle-to-cycle period jitter	Regional	tJIT(cc)	–150	150	–170	170	–190	190	–190	190	–230	230	ps
Duty cycle jitter	Regional	tJIT(duty)	–80	80	–90	90	–100	100	–100	100	–140	140	ps
Clock period jitter	Global	tJIT(per)	–113	113	–128	128	–150	150	–150	150	–180	180	ps
Cycle-to-cycle period jitter	Global	tJIT(cc)	–225	225	–255	255	–285	285	–285	285	–340	340	ps
Duty cycle jitter	Global	tJIT(duty)	–120	120	–135	135	–150	150	–150	150	–180	180	ps

Notes to Table 1–33:

(1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 standard.

(2) The clock jitter specification applies to memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a regional or global clock network as specified. Altera recommends using the regional clock networks whenever possible.

OCT Calibration Block Specifications

Table 1–34 lists the on-chip termination calibration block specifications for Stratix III devices.

Table 1–34. On-Chip Termination Calibration Block Specification

Symbol	Description	Min	Typical	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
t_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT Rs and Rt calibration	—	1000	—	cycles
$t_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out per OCT calibration block	—	28	—	cycles
t_{RS_RT}	Time required to dynamically switch from Rs to Rt	—	2.5	—	ns

DCD Specifications

Table 1–35 lists the worst case duty cycle distortion for Stratix III devices.

Table 1–35. Duty Cycle Distortion on Stratix III I/O Pins *(Note 1)*

Symbol	C2		C3		C4		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

Note to Table 1–35:

(1) The DCD specification applies to clock outputs from the PLLs, global clock tree, and IOE driving dedicated and general-purpose I/O pins.

I/O Timing

The following sections describe the timing models, preliminary and final timings, I/O timing measurement methodology, I/O default capacitive loading, programmable IOE delay, programmable output buffer delay, user I/O timing, and dedicated clock pin timing.

Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix III device densities and speed grades. This section describes the performance of the Stratix III device I/Os.

All specifications except the fast model are representative of worst-case supply voltage and junction temperature conditions. Fast model specifications are representative of best case process, supply voltage, and junction temperature conditions.

The timing numbers listed in this section are extracted from the Quartus II software version 8.1.

EP3SL70 I/O Timing Parameters

Table 1–51 through Table 1–54 list the maximum I/O timing parameters for EP3SL70 devices for single-ended I/O standards.

Table 1–51 lists the EP3SL70 column pins input timing parameters for single-ended I/O standards.

Table 1–51. EP3SL70 Column Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
3.3-V LVTTL	GCLK	t_{su}	-0.812	-0.811	-1.154	-1.261	-1.312	-1.266	-1.645	-1.261	-1.312	-1.266	-1.645	ns
		t_h	0.934	0.934	1.327	1.457	1.533	1.475	1.850	1.457	1.533	1.475	1.850	ns
	GCLK PLL	t_{su}	-0.965	-0.965	-1.395	-1.522	-1.763	-1.703	-2.094	-1.522	-1.763	-1.703	-2.094	ns
		t_h	1.216	1.216	1.764	1.937	2.222	2.138	2.540	1.937	2.222	2.138	2.540	ns
3.3-V LVCMOS	GCLK	t_{su}	-0.812	-0.811	-1.154	-1.261	-1.312	-1.266	-1.645	-1.261	-1.312	-1.266	-1.645	ns
		t_h	0.934	0.934	1.327	1.457	1.533	1.475	1.850	1.457	1.533	1.475	1.850	ns
	GCLK PLL	t_{su}	-0.965	-0.965	-1.395	-1.522	-1.763	-1.703	-2.094	-1.522	-1.763	-1.703	-2.094	ns
		t_h	1.216	1.216	1.764	1.937	2.222	2.138	2.540	1.937	2.222	2.138	2.540	ns
3.0-V LVTTL	GCLK	t_{su}	-0.823	-0.822	-1.153	-1.263	-1.311	-1.265	-1.644	-1.263	-1.311	-1.265	-1.644	ns
		t_h	0.945	0.945	1.326	1.459	1.532	1.474	1.849	1.459	1.532	1.474	1.849	ns
	GCLK PLL	t_{su}	-0.976	-0.976	-1.394	-1.524	-1.762	-1.702	-2.093	-1.524	-1.762	-1.702	-2.093	ns
		t_h	1.227	1.227	1.763	1.939	2.221	2.137	2.539	1.939	2.221	2.137	2.539	ns
3.0-V LVCMOS	GCLK	t_{su}	-0.823	-0.822	-1.153	-1.263	-1.311	-1.265	-1.644	-1.263	-1.311	-1.265	-1.644	ns
		t_h	0.945	0.945	1.326	1.459	1.532	1.474	1.849	1.459	1.532	1.474	1.849	ns
	GCLK PLL	t_{su}	-0.976	-0.976	-1.394	-1.524	-1.762	-1.702	-2.093	-1.524	-1.762	-1.702	-2.093	ns
		t_h	1.227	1.227	1.763	1.939	2.221	2.137	2.539	1.939	2.221	2.137	2.539	ns
2.5 V	GCLK	t_{su}	-0.818	-0.817	-1.162	-1.275	-1.330	-1.284	-1.663	-1.275	-1.330	-1.284	-1.663	ns
		t_h	0.940	0.940	1.335	1.471	1.551	1.493	1.868	1.471	1.551	1.493	1.868	ns
	GCLK PLL	t_{su}	-0.971	-0.971	-1.403	-1.536	-1.781	-1.721	-2.112	-1.536	-1.781	-1.721	-2.112	ns
		t_h	1.222	1.222	1.772	1.951	2.240	2.156	2.558	1.951	2.240	2.156	2.558	ns
1.8 V	GCLK	t_{su}	-0.840	-0.839	-1.202	-1.311	-1.328	-1.282	-1.661	-1.311	-1.328	-1.282	-1.661	ns
		t_h	0.964	0.964	1.375	1.507	1.549	1.491	1.866	1.507	1.549	1.491	1.866	ns
	GCLK PLL	t_{su}	-0.993	-0.993	-1.443	-1.572	-1.779	-1.719	-2.110	-1.572	-1.779	-1.719	-2.110	ns
		t_h	1.246	1.246	1.812	1.987	2.238	2.154	2.556	1.987	2.238	2.154	2.556	ns
1.5 V	GCLK	t_{su}	-0.830	-0.829	-1.179	-1.279	-1.258	-1.212	-1.591	-1.279	-1.258	-1.212	-1.591	ns
		t_h	0.954	0.954	1.352	1.475	1.479	1.421	1.796	1.475	1.479	1.421	1.796	ns
	GCLK PLL	t_{su}	-0.983	-0.983	-1.420	-1.540	-1.709	-1.649	-2.040	-1.540	-1.709	-1.649	-2.040	ns
		t_h	1.236	1.236	1.789	1.955	2.168	2.084	2.486	1.955	2.168	2.084	2.486	ns
1.2 V	GCLK	t_{su}	-0.778	-0.777	-1.102	-1.180	-1.102	-1.056	-1.435	-1.180	-1.102	-1.056	-1.435	ns
		t_h	0.902	0.902	1.275	1.376	1.323	1.265	1.640	1.376	1.323	1.265	1.640	ns
	GCLK PLL	t_{su}	-0.931	-0.931	-1.343	-1.441	-1.553	-1.493	-1.884	-1.441	-1.553	-1.493	-1.884	ns
		t_h	1.184	1.184	1.712	1.856	2.012	1.928	2.330	1.856	2.012	1.928	2.330	ns

Table 1–53. EP3SL70 Column Pins Output Timing Parameters (Part 3 of 7)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
1.8 V	2mA	GCLK	t_{co}	3.378	3.378	4.810	5.219	5.742	5.621	5.829	5.219	5.742	5.621	5.829	ns
		GCLK PLL	t_{co}	3.705	3.705	5.294	5.748	6.339	6.196	6.478	5.748	6.339	6.196	6.478	ns
	4mA	GCLK	t_{co}	3.200	3.200	4.533	4.912	5.395	5.275	5.481	4.912	5.395	5.275	5.481	ns
		GCLK PLL	t_{co}	3.524	3.524	5.015	5.439	5.991	5.849	6.147	5.439	5.991	5.849	6.147	ns
	6mA	GCLK	t_{co}	3.115	3.115	4.424	4.796	5.284	5.163	5.371	4.796	5.284	5.163	5.371	ns
		GCLK PLL	t_{co}	3.442	3.442	4.908	5.324	5.881	5.738	6.035	5.324	5.881	5.738	6.035	ns
	8mA	GCLK	t_{co}	3.095	3.095	4.366	4.742	5.218	5.097	5.305	4.742	5.218	5.097	5.305	ns
		GCLK PLL	t_{co}	3.422	3.422	4.850	5.270	5.815	5.672	5.958	5.270	5.815	5.672	5.958	ns
	10mA	GCLK	t_{co}	3.032	3.032	4.306	4.668	5.137	5.016	5.224	4.668	5.137	5.016	5.224	ns
		GCLK PLL	t_{co}	3.359	3.359	4.789	5.195	5.734	5.591	5.889	5.195	5.734	5.591	5.889	ns
	12mA	GCLK	t_{co}	3.015	3.015	4.285	4.647	5.114	4.993	5.201	4.647	5.114	4.993	5.201	ns
		GCLK PLL	t_{co}	3.341	3.341	4.768	5.174	5.711	5.568	5.856	5.174	5.711	5.568	5.856	ns
1.5 V	2mA	GCLK	t_{co}	3.324	3.324	4.739	5.152	5.680	5.559	5.767	5.152	5.680	5.559	5.767	ns
		GCLK PLL	t_{co}	3.651	3.651	5.223	5.680	6.277	6.134	6.423	5.680	6.277	6.134	6.423	ns
	4mA	GCLK	t_{co}	3.112	3.112	4.420	4.795	5.288	5.167	5.375	4.795	5.288	5.167	5.375	ns
		GCLK PLL	t_{co}	3.439	3.439	4.904	5.324	5.885	5.742	6.037	5.324	5.885	5.742	6.037	ns
	6mA	GCLK	t_{co}	3.088	3.088	4.353	4.737	5.221	5.100	5.308	4.737	5.221	5.100	5.308	ns
		GCLK PLL	t_{co}	3.414	3.414	4.837	5.264	5.818	5.675	5.960	5.264	5.818	5.675	5.960	ns
	8mA	GCLK	t_{co}	3.076	3.076	4.337	4.712	5.201	5.080	5.288	4.712	5.201	5.080	5.288	ns
		GCLK PLL	t_{co}	3.403	3.403	4.820	5.239	5.798	5.655	5.943	5.239	5.798	5.655	5.943	ns
	10mA	GCLK	t_{co}	3.021	3.021	4.298	4.661	5.131	5.010	5.218	4.661	5.131	5.010	5.218	ns
		GCLK PLL	t_{co}	3.348	3.348	4.782	5.188	5.728	5.585	5.880	5.188	5.728	5.585	5.880	ns
	12mA	GCLK	t_{co}	3.015	3.015	4.281	4.648	5.120	4.999	5.207	4.648	5.120	4.999	5.207	ns
		GCLK PLL	t_{co}	3.343	3.343	4.765	5.177	5.717	5.574	5.859	5.177	5.717	5.574	5.859	ns

Table 1–58 lists the EP3SL70 row pins output timing parameters for differential I/O standards.

Table 1–58. EP3SL70 Row Pins Output Timing Parameters (Part 1 of 3)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
LVDS	—	GCLK	t_{co}	2.668	2.842	3.979	4.346	4.821	4.685	4.892	4.453	4.930	4.795	4.940	ns
		GCLK PLL	t_{co}	3.062	3.288	4.646	5.055	5.575	5.431	5.630	5.186	5.709	5.565	5.694	ns
LVDS_E_1R	—	GCLK	t_{co}	3.044	3.278	4.684	5.101	5.629	5.485	5.684	5.237	5.770	5.626	5.755	ns
		GCLK PLL	t_{co}	2.668	2.842	3.979	4.346	4.821	4.685	4.892	4.453	4.930	4.795	4.940	ns
LVDS_E_3R	—	GCLK	t_{co}	3.062	3.288	4.646	5.055	5.575	5.431	5.630	5.186	5.709	5.565	5.694	ns
		GCLK PLL	t_{co}	3.044	3.278	4.684	5.101	5.629	5.485	5.684	5.237	5.770	5.626	5.755	ns
MINI-LVDS	—	GCLK	t_{co}	2.668	2.842	3.979	4.346	4.821	4.685	4.892	4.453	4.930	4.795	4.940	ns
		GCLK PLL	t_{co}	3.062	3.288	4.646	5.055	5.575	5.431	5.630	5.186	5.709	5.565	5.694	ns
MINI-LVDS_E_1R	—	GCLK	t_{co}	3.044	3.278	4.684	5.101	5.629	5.485	5.684	5.237	5.770	5.626	5.755	ns
		GCLK PLL	t_{co}	3.098	3.331	4.730	5.145	5.672	5.528	5.727	5.280	5.809	5.665	5.794	ns
MINI-LVDS_E_3R	—	GCLK	t_{co}	3.084	3.317	4.717	5.132	5.659	5.515	5.714	5.266	5.796	5.652	5.781	ns
		GCLK PLL	t_{co}	3.080	3.313	4.715	5.132	5.660	5.516	5.715	5.266	5.798	5.654	5.783	ns
RSDS	—	GCLK	t_{co}	3.096	3.328	4.716	5.129	5.654	5.510	5.709	5.263	5.791	5.647	5.776	ns
		GCLK PLL	t_{co}	3.085	3.318	4.712	5.125	5.651	5.507	5.706	5.260	5.788	5.644	5.773	ns
RSDS_E_1R	—	GCLK	t_{co}	3.082	3.315	4.710	5.123	5.649	5.505	5.704	5.258	5.787	5.643	5.772	ns
		GCLK PLL	t_{co}	3.093	3.325	4.711	5.124	5.648	5.504	5.703	5.257	5.785	5.641	5.770	ns
RSDS_E_3R	—	GCLK	t_{co}	3.083	3.316	4.709	5.122	5.647	5.503	5.702	5.257	5.785	5.641	5.770	ns
		GCLK PLL	t_{co}	3.069	3.302	4.694	5.107	5.633	5.489	5.688	5.242	5.770	5.626	5.755	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{co}	3.066	3.298	4.690	5.103	5.629	5.485	5.684	5.238	5.766	5.622	5.751	ns
		GCLK PLL	t_{co}	3.063	3.296	4.691	5.106	5.632	5.488	5.687	5.241	5.770	5.626	5.755	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	t_{co}	3.064	3.296	4.681	5.094	5.619	5.475	5.674	5.228	5.756	5.612	5.741	ns
		GCLK PLL	t_{co}	3.113	3.349	4.752	5.167	5.695	5.551	5.750	5.302	5.832	5.688	5.817	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	t_{co}	3.089	3.325	4.734	5.150	5.678	5.534	5.733	5.285	5.817	5.673	5.802	ns
		GCLK PLL	t_{co}	3.071	3.306	4.712	5.128	5.656	5.512	5.711	5.263	5.795	5.651	5.780	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	t_{co}	3.117	3.352	4.752	5.167	5.694	5.550	5.749	5.302	5.832	5.688	5.817	ns
		GCLK PLL	t_{co}	3.102	3.337	4.738	5.152	5.679	5.535	5.734	5.287	5.817	5.673	5.802	ns

Table 1–67. EP3SL110 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{co}	3.118	3.353	4.737	5.133	5.643	5.504	5.788	5.256	5.765	5.629	5.862	ns
		GCLK PLL	t_{co}	1.326	1.503	1.935	2.032	2.245	2.256	2.283	2.137	2.352	2.362	2.270	ns
	6mA	GCLK	t_{co}	3.114	3.350	4.738	5.135	5.647	5.508	5.792	5.258	5.769	5.633	5.866	ns
		GCLK PLL	t_{co}	1.322	1.500	1.936	2.034	2.249	2.260	2.287	2.139	2.356	2.366	2.274	ns
	8mA	GCLK	t_{co}	3.104	3.339	4.727	5.124	5.635	5.496	5.780	5.247	5.757	5.621	5.854	ns
		GCLK PLL	t_{co}	1.312	1.489	1.925	2.023	2.237	2.248	2.275	2.128	2.344	2.354	2.262	ns
	10mA	GCLK	t_{co}	3.102	3.337	4.725	5.121	5.633	5.494	5.778	5.245	5.755	5.619	5.852	ns
		GCLK PLL	t_{co}	1.310	1.487	1.923	2.020	2.235	2.246	2.273	2.126	2.342	2.352	2.260	ns
	12mA	GCLK	t_{co}	3.102	3.338	4.728	5.126	5.638	5.499	5.783	5.249	5.761	5.625	5.858	ns
		GCLK PLL	t_{co}	1.310	1.488	1.926	2.025	2.240	2.251	2.278	2.130	2.348	2.358	2.266	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{co}	3.106	3.341	4.725	5.121	5.632	5.493	5.777	5.244	5.754	5.618	5.851	ns
		GCLK PLL	t_{co}	1.314	1.491	1.923	2.020	2.234	2.245	2.272	2.125	2.341	2.351	2.259	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{co}	3.132	3.370	4.770	5.169	5.682	5.543	5.827	5.292	5.804	5.668	5.901	ns
		GCLK PLL	t_{co}	1.340	1.520	1.968	2.068	2.284	2.295	2.322	2.173	2.391	2.401	2.309	ns
	6mA	GCLK	t_{co}	3.118	3.356	4.758	5.158	5.672	5.533	5.817	5.282	5.795	5.659	5.892	ns
		GCLK PLL	t_{co}	1.326	1.506	1.956	2.057	2.274	2.285	2.312	2.163	2.382	2.392	2.300	ns
	8mA	GCLK	t_{co}	3.106	3.343	4.741	5.140	5.654	5.515	5.799	5.264	5.777	5.641	5.874	ns
		GCLK PLL	t_{co}	1.314	1.493	1.939	2.039	2.256	2.267	2.294	2.145	2.364	2.374	2.282	ns
	10mA	GCLK	t_{co}	3.106	3.343	4.744	5.144	5.658	5.519	5.803	5.268	5.782	5.646	5.879	ns
		GCLK PLL	t_{co}	1.314	1.493	1.942	2.043	2.260	2.271	2.298	2.149	2.369	2.379	2.287	ns
	12mA	GCLK	t_{co}	3.102	3.339	4.737	5.136	5.651	5.512	5.796	5.261	5.774	5.638	5.871	ns
		GCLK PLL	t_{co}	1.310	1.489	1.935	2.035	2.253	2.264	2.291	2.142	2.361	2.371	2.279	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	8mA	GCLK	t_{co}	3.106	3.341	4.730	5.127	5.639	5.500	5.784	5.250	5.761	5.625	5.858	ns
		GCLK PLL	t_{co}	1.314	1.491	1.928	2.026	2.241	2.252	2.279	2.131	2.348	2.358	2.266	ns
	16mA	GCLK	t_{co}	3.107	3.343	4.738	5.137	5.650	5.511	5.795	5.260	5.773	5.637	5.870	ns
		GCLK PLL	t_{co}	1.315	1.493	1.936	2.036	2.252	2.263	2.290	2.141	2.360	2.370	2.278	ns

Table 1–77 lists the EP3SL150 column pins output timing parameters for differential I/O standards.

Table 1–77. EP3SL150 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
LVDS_E_1R	—	GCLK	t_{co}	3.100	3.330	4.687	5.079	5.586	5.447	5.731	5.200	5.706	5.570	5.803	ns
		GCLK PLL	t_{co}	1.308	1.480	1.885	1.978	2.188	2.199	2.226	2.081	2.293	2.303	2.211	ns
LVDS_E_3R	—	GCLK	t_{co}	3.096	3.333	4.734	5.134	5.648	5.509	5.793	5.259	5.772	5.636	5.869	ns
		GCLK PLL	t_{co}	1.304	1.483	1.932	2.033	2.250	2.261	2.288	2.140	2.359	2.369	2.277	ns
MINI-LVDS_E_1R	—	GCLK	t_{co}	3.100	3.330	4.687	5.079	5.586	5.447	5.731	5.200	5.706	5.570	5.803	ns
		GCLK PLL	t_{co}	1.308	1.480	1.885	1.978	2.188	2.199	2.226	2.081	2.293	2.303	2.211	ns
MINI-LVDS_E_3R	—	GCLK	t_{co}	3.096	3.333	4.734	5.134	5.648	5.509	5.793	5.259	5.772	5.636	5.869	ns
		GCLK PLL	t_{co}	1.304	1.483	1.932	2.033	2.250	2.261	2.288	2.140	2.359	2.369	2.277	ns
RSDS_E_1R	—	GCLK	t_{co}	3.100	3.330	4.687	5.079	5.586	5.447	5.731	5.200	5.706	5.570	5.803	ns
		GCLK PLL	t_{co}	1.308	1.480	1.885	1.978	2.188	2.199	2.226	2.081	2.293	2.303	2.211	ns
RSDS_E_3R	—	GCLK	t_{co}	3.096	3.333	4.734	5.134	5.648	5.509	5.793	5.259	5.772	5.636	5.869	ns
		GCLK PLL	t_{co}	1.304	1.483	1.932	2.033	2.250	2.261	2.288	2.140	2.359	2.369	2.277	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{co}	3.127	3.363	4.758	5.157	5.670	5.531	5.815	5.280	5.792	5.656	5.889	ns
		GCLK PLL	t_{co}	1.335	1.513	1.956	2.056	2.272	2.283	2.310	2.161	2.379	2.389	2.297	ns
	6mA	GCLK	t_{co}	3.117	3.353	4.748	5.146	5.660	5.521	5.805	5.269	5.782	5.646	5.879	ns
		GCLK PLL	t_{co}	1.325	1.503	1.946	2.045	2.262	2.273	2.300	2.150	2.369	2.379	2.287	ns
	8mA	GCLK	t_{co}	3.117	3.353	4.751	5.150	5.664	5.525	5.809	5.274	5.787	5.651	5.884	ns
		GCLK PLL	t_{co}	1.325	1.503	1.949	2.049	2.266	2.277	2.304	2.155	2.374	2.384	2.292	ns
	10mA	GCLK	t_{co}	3.110	3.347	4.744	5.144	5.658	5.519	5.803	5.267	5.781	5.645	5.878	ns
		GCLK PLL	t_{co}	1.318	1.497	1.942	2.043	2.260	2.271	2.298	2.148	2.368	2.378	2.286	ns
	12mA	GCLK	t_{co}	3.109	3.345	4.741	5.141	5.655	5.516	5.800	5.264	5.777	5.641	5.874	ns
		GCLK PLL	t_{co}	1.317	1.495	1.939	2.040	2.257	2.268	2.295	2.145	2.364	2.374	2.282	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	16mA	GCLK	t_{co}	3.131	3.367	4.762	5.161	5.674	5.535	5.819	5.284	5.797	5.661	5.894	ns
		GCLK PLL	t_{co}	1.339	1.517	1.960	2.060	2.276	2.287	2.314	2.165	2.384	2.394	2.302	ns

Table 1–78. EP3SL150 Row Pins Output Timing Parameters (Part 3 of 3)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{co}	3.151	3.396	4.805	5.209	5.720	5.584	5.839	5.335	5.849	5.712	5.915	ns
		GCLK PLL	t_{co}	1.371	1.557	2.015	2.118	2.331	2.344	2.347	2.226	2.443	2.453	2.335	ns
	6mA	GCLK	t_{co}	3.136	3.381	4.791	5.194	5.705	5.569	5.824	5.320	5.834	5.697	5.900	ns
		GCLK PLL	t_{co}	1.356	1.542	2.001	2.103	2.316	2.329	2.332	2.211	2.428	2.438	2.320	ns
	8mA	GCLK	t_{co}	3.125	3.370	4.786	5.191	5.702	5.566	5.821	5.317	5.832	5.695	5.898	ns
		GCLK PLL	t_{co}	1.345	1.531	1.996	2.100	2.313	2.326	2.329	2.208	2.426	2.436	2.318	ns
	10mA	GCLK	t_{co}	3.105	3.350	4.763	5.167	5.679	5.543	5.798	5.294	5.808	5.671	5.874	ns
		GCLK PLL	t_{co}	1.325	1.511	1.973	2.076	2.290	2.303	2.306	2.185	2.402	2.412	2.294	ns
	12mA	GCLK	t_{co}	3.102	3.346	4.759	5.164	5.675	5.539	5.794	5.290	5.805	5.668	5.871	ns
		GCLK PLL	t_{co}	1.322	1.507	1.969	2.073	2.286	2.299	2.302	2.181	2.399	2.409	2.291	ns
	8mA	GCLK	t_{co}	3.107	3.350	4.750	5.152	5.661	5.525	5.780	5.277	5.789	5.652	5.855	ns
		GCLK PLL	t_{co}	1.327	1.511	1.960	2.061	2.272	2.285	2.288	2.168	2.383	2.393	2.275	ns
	16mA	GCLK	t_{co}	3.100	3.343	4.749	5.153	5.664	5.528	5.783	5.280	5.794	5.657	5.860	ns
		GCLK PLL	t_{co}	1.320	1.504	1.959	2.062	2.275	2.288	2.291	2.171	2.388	2.398	2.280	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	t_{co}	3.138	3.382	4.787	5.190	5.700	5.564	5.819	5.316	5.829	5.692	5.895	ns
		GCLK PLL	t_{co}	1.358	1.543	1.997	2.099	2.311	2.324	2.327	2.207	2.423	2.433	2.315	ns
	12mA	GCLK	t_{co}	3.120	3.365	4.772	5.175	5.685	5.549	5.804	5.301	5.814	5.677	5.880	ns
		GCLK PLL	t_{co}	1.340	1.526	1.982	2.084	2.296	2.309	2.312	2.192	2.408	2.418	2.300	ns
	16mA	GCLK	t_{co}	3.106	3.349	4.749	5.151	5.660	5.524	5.779	5.277	5.789	5.652	5.855	ns
		GCLK PLL	t_{co}	1.326	1.510	1.959	2.060	2.271	2.284	2.287	2.168	2.383	2.393	2.275	ns

Table 1–93. EP3SL340 Column Pins Output Timing Parameters (Part 7 of 7)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
1.2-V HSTL CLASS I	4mA	GCLK	t_{co}	3.552	3.552	5.246	5.442	5.974	5.826	6.255	5.442	5.974	5.826	6.255	ns
		GCLK PLL	t_{co}	4.117	4.117	6.087	6.291	6.929	6.749	7.292	6.291	6.929	6.749	7.292	ns
	6mA	GCLK	t_{co}	3.544	3.544	5.237	5.433	5.965	5.817	6.246	5.433	5.965	5.817	6.246	ns
		GCLK PLL	t_{co}	4.108	4.108	6.078	6.282	6.917	6.737	7.280	6.282	6.917	6.737	7.280	ns
	8mA	GCLK	t_{co}	3.545	3.545	5.244	5.442	5.974	5.826	6.255	5.442	5.974	5.826	6.255	ns
		GCLK PLL	t_{co}	4.108	4.108	6.085	6.290	6.920	6.740	7.283	6.290	6.920	6.740	7.283	ns
	10mA	GCLK	t_{co}	3.534	3.534	5.231	5.428	5.960	5.812	6.241	5.428	5.960	5.812	6.241	ns
		GCLK PLL	t_{co}	4.098	4.098	6.072	6.276	6.915	6.736	7.277	6.276	6.915	6.736	7.277	ns
	12mA	GCLK	t_{co}	3.534	3.534	5.231	5.428	5.961	5.813	6.242	5.428	5.961	5.813	6.242	ns
		GCLK PLL	t_{co}	4.098	4.098	6.073	6.277	6.906	6.727	7.269	6.277	6.906	6.727	7.269	ns
1.2-V HSTL CLASS II	16mA	GCLK	t_{co}	3.555	3.555	5.247	5.443	5.974	5.826	6.255	5.443	5.974	5.826	6.255	ns
		GCLK PLL	t_{co}	4.119	4.119	6.089	6.292	6.943	6.763	7.306	6.292	6.943	6.763	7.306	ns
3.0-V PCI	—	GCLK	t_{co}	3.658	3.658	5.292	5.477	5.999	5.851	6.280	5.477	5.999	5.851	6.280	ns
		GCLK PLL	t_{co}	4.222	4.222	6.134	6.328	6.974	6.794	7.337	6.328	6.974	6.794	7.337	ns
3.0-V PCI-X	—	GCLK	t_{co}	3.658	3.658	5.292	5.477	5.999	5.851	6.280	5.477	5.999	5.851	6.280	ns
		GCLK PLL	t_{co}	4.222	4.222	6.134	6.328	6.974	6.794	7.337	6.328	6.974	6.794	7.337	ns

Table 1–98 lists the EP3SL340 row pins output timing parameters for differential I/O standards.

Table 1–98. EP3SL340 Row Pins Output Timing Parameters (Part 1 of 3)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
LVDS	—	GCLK	t_{co}	3.022	3.234	4.714	4.872	5.362	5.217	5.602	4.981	5.467	5.326	5.662	ns
		GCLK PLL	t_{co}	1.063	1.193	1.445	1.501	1.678	1.690	1.735	1.583	1.761	1.772	1.704	ns
LVDS_E_1R	—	GCLK	t_{co}	3.414	3.678	5.396	5.588	6.125	5.972	6.349	5.722	6.255	6.105	6.425	ns
		GCLK PLL	t_{co}	1.455	1.637	2.127	2.217	2.441	2.445	2.482	2.324	2.549	2.551	2.467	ns
LVDS_E_3R	—	GCLK	t_{co}	3.396	3.668	5.434	5.634	6.179	6.026	6.403	5.773	6.316	6.166	6.486	ns
		GCLK PLL	t_{co}	1.437	1.627	2.165	2.263	2.495	2.499	2.536	2.375	2.610	2.612	2.528	ns
MINI-LVDS	—	GCLK	t_{co}	3.022	3.234	4.714	4.872	5.362	5.217	5.602	4.981	5.467	5.326	5.662	ns
		GCLK PLL	t_{co}	1.063	1.193	1.445	1.501	1.678	1.690	1.735	1.583	1.761	1.772	1.704	ns
MINI-LVDS_E_1R	—	GCLK	t_{co}	3.414	3.678	5.396	5.588	6.125	5.972	6.349	5.722	6.255	6.105	6.425	ns
		GCLK PLL	t_{co}	1.455	1.637	2.127	2.217	2.441	2.445	2.482	2.324	2.549	2.551	2.467	ns
MINI-LVDS_E_3R	—	GCLK	t_{co}	3.396	3.668	5.434	5.634	6.179	6.026	6.403	5.773	6.316	6.166	6.486	ns
		GCLK PLL	t_{co}	1.437	1.627	2.165	2.263	2.495	2.499	2.536	2.375	2.610	2.612	2.528	ns
RSDS	—	GCLK	t_{co}	3.022	3.234	4.714	4.872	5.362	5.217	5.602	4.981	5.467	5.326	5.662	ns
		GCLK PLL	t_{co}	1.063	1.193	1.445	1.501	1.678	1.690	1.735	1.583	1.761	1.772	1.704	ns
RSDS_E_1R	—	GCLK	t_{co}	3.414	3.678	5.396	5.588	6.125	5.972	6.349	5.722	6.255	6.105	6.425	ns
		GCLK PLL	t_{co}	1.455	1.637	2.127	2.217	2.441	2.445	2.482	2.324	2.549	2.551	2.467	ns
RSDS_E_3R	—	GCLK	t_{co}	3.396	3.668	5.434	5.634	6.179	6.026	6.403	5.773	6.316	6.166	6.486	ns
		GCLK PLL	t_{co}	1.437	1.627	2.165	2.263	2.495	2.499	2.536	2.375	2.610	2.612	2.528	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{co}	3.440	3.711	5.470	5.668	6.212	6.059	6.436	5.806	6.345	6.195	6.515	ns
		GCLK PLL	t_{co}	1.491	1.680	2.211	2.307	2.538	2.542	2.579	2.418	2.649	2.651	2.567	ns
	6mA	GCLK	t_{co}	3.426	3.697	5.457	5.655	6.199	6.046	6.423	5.792	6.332	6.182	6.502	ns
		GCLK PLL	t_{co}	1.477	1.666	2.198	2.294	2.525	2.529	2.566	2.404	2.636	2.638	2.554	ns
	8mA	GCLK	t_{co}	3.422	3.693	5.455	5.655	6.200	6.047	6.424	5.792	6.334	6.184	6.504	ns
		GCLK PLL	t_{co}	1.473	1.662	2.196	2.294	2.526	2.530	2.567	2.404	2.638	2.640	2.556	ns

Table 1–101. EP3SE50 Column Pins Input Timing Parameters (Part 4 of 4)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
3.0-V | PCI-X	GCLK	t_{su}	-0.754	-0.753	-1.062	-1.167	-1.373	-1.328	-1.604	-1.167	-1.373	-1.328	-1.604	ns
		t_h	0.881	0.880	1.240	1.368	1.594	1.537	1.814	1.368	1.594	1.537	1.814	ns
	GCLK PLL	t_{su}	-1.048	-1.048	-1.465	-1.595	-1.829	-1.771	-2.037	-1.595	-1.829	-1.771	-2.037	ns
		t_h	1.301	1.301	1.835	2.011	2.291	2.206	2.483	2.011	2.291	2.206	2.483	ns

Table 1–102 lists the EP3SE50 row pins input timing parameters for single-ended I/O standards.

Table 1–102. EP3SE50 Row Pins Input Timing Parameters (Part 1 of 3)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
3.3-V LVTTL	GCLK	t_{su}	-0.896	-0.926	-1.311	-1.433	-1.658	-1.605	-1.896	-1.451	-1.663	-1.612	-1.927	ns
		t_h	1.009	1.052	1.597	1.816	1.931	1.813	1.843	1.809	1.936	1.818	1.895	ns
	GCLK PLL	t_{su}	0.952	0.960	1.494	1.640	1.888	1.819	2.111	1.667	1.903	1.836	2.144	ns
		t_h	-0.703	-0.700	-1.311	-1.433	-1.658	-1.605	-1.896	-1.451	-1.663	-1.612	-1.927	ns
3.3-V LVCMOS	GCLK	t_{su}	-0.896	-0.926	-1.311	-1.433	-1.658	-1.605	-1.896	-1.451	-1.663	-1.612	-1.927	ns
		t_h	1.009	1.052	1.597	1.816	1.931	1.813	1.843	1.809	1.936	1.818	1.895	ns
	GCLK PLL	t_{su}	0.952	0.960	1.494	1.640	1.888	1.819	2.111	1.667	1.903	1.836	2.144	ns
		t_h	-0.703	-0.700	-1.308	-1.434	-1.661	-1.608	-1.899	-1.450	-1.668	-1.617	-1.932	ns
3.0-V LVTTL	GCLK	t_{su}	-0.902	-0.937	1.491	1.641	1.891	1.822	2.114	1.666	1.908	1.841	2.149	ns
		t_h	1.015	1.063	-1.308	-1.434	-1.661	-1.608	-1.899	-1.450	-1.668	-1.617	-1.932	ns
	GCLK PLL	t_{su}	0.946	0.949	1.600	1.815	1.928	1.810	1.840	1.810	1.931	1.813	1.890	ns
		t_h	-0.697	-0.689	1.491	1.641	1.891	1.822	2.114	1.666	1.908	1.841	2.149	ns
3.0-V LVCMOS	GCLK	t_{su}	-0.902	-0.937	1.500	1.654	1.906	1.837	2.129	1.675	1.918	1.851	2.159	ns
		t_h	1.015	1.063	-1.317	-1.447	-1.676	-1.623	-1.914	-1.459	-1.678	-1.627	-1.942	ns
	GCLK PLL	t_{su}	0.946	0.949	1.591	1.802	1.913	1.795	1.825	1.801	1.921	1.803	1.880	ns
		t_h	-0.697	-0.689	1.500	1.654	1.906	1.837	2.129	1.675	1.918	1.851	2.159	ns
2.5 V	GCLK	t_{su}	-0.890	-0.930	1.510	1.730	1.876	1.758	1.788	1.729	1.881	1.762	1.840	ns
		t_h	1.003	1.056	1.458	1.596	1.807	1.742	2.015	1.614	1.817	1.754	2.048	ns
	GCLK PLL	t_{su}	0.958	0.956	-1.272	-1.388	-1.573	-1.523	-1.797	-1.395	-1.573	-1.526	-1.829	ns
		t_h	-0.709	-0.696	1.510	1.730	1.876	1.758	1.788	1.729	1.881	1.762	1.840	ns
1.8 V	GCLK	t_{su}	-0.869	-0.907	1.534	1.762	1.944	1.826	1.856	1.760	1.946	1.827	1.905	ns
		t_h	0.890	0.886	1.434	1.564	1.739	1.674	1.947	1.583	1.752	1.689	1.983	ns
	GCLK PLL	t_{su}	0.986	1.035	-1.248	-1.356	-1.505	-1.455	-1.729	-1.364	-1.508	-1.461	-1.764	ns
		t_h	-0.859	-0.896	1.613	1.863	2.103	1.985	2.015	1.856	2.101	1.982	2.060	ns

Table 1–103 lists the EP3SE50 column pins output timing parameters for single-ended I/O standards.

Table 1–103. EP3SE50 Column Pins Output Timing Parameters (Part 1 of 6)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
3.3-V LVTTL	4mA	GCLK	t_{co}	3.293	3.293	4.559	4.925	5.402	5.282	5.365	4.925	5.402	5.282	5.365	ns
		GCLK PLL	t_{co}	3.550	3.524	4.903	5.329	5.819	5.674	5.973	5.329	5.819	5.674	5.973	ns
	8mA	GCLK	t_{co}	3.176	3.176	4.405	4.763	5.232	5.112	5.252	4.763	5.232	5.112	5.252	ns
		GCLK PLL	t_{co}	3.483	3.457	4.794	5.218	5.706	5.561	5.860	5.218	5.706	5.561	5.860	ns
	12mA	GCLK	t_{co}	3.081	3.081	4.268	4.620	5.080	4.960	5.162	4.620	5.080	4.960	5.162	ns
		GCLK PLL	t_{co}	3.397	3.371	4.691	5.120	5.614	5.469	5.768	5.120	5.614	5.469	5.768	ns
	16mA	GCLK	t_{co}	3.041	3.051	4.243	4.596	5.055	4.935	5.120	4.596	5.055	4.935	5.120	ns
		GCLK PLL	t_{co}	3.390	3.364	4.674	5.092	5.573	5.428	5.727	5.092	5.573	5.428	5.727	ns
3.3-V LVCMOS	4mA	GCLK	t_{co}	3.296	3.296	4.563	4.937	5.416	5.296	5.373	4.937	5.416	5.296	5.373	ns
		GCLK PLL	t_{co}	3.556	3.530	4.908	5.334	5.826	5.681	5.980	5.334	5.826	5.681	5.980	ns
	8mA	GCLK	t_{co}	3.096	3.096	4.273	4.625	5.086	4.966	5.172	4.625	5.086	4.966	5.172	ns
		GCLK PLL	t_{co}	3.401	3.375	4.701	5.137	5.625	5.480	5.779	5.137	5.625	5.480	5.779	ns
	12mA	GCLK	t_{co}	3.059	3.069	4.236	4.594	5.055	4.935	5.148	4.594	5.055	4.935	5.148	ns
		GCLK PLL	t_{co}	3.408	3.382	4.695	5.116	5.599	5.454	5.753	5.116	5.599	5.454	5.753	ns
	16mA	GCLK	t_{co}	3.043	3.053	4.212	4.553	5.025	4.904	5.119	4.553	5.025	4.904	5.119	ns
		GCLK PLL	t_{co}	3.392	3.366	4.672	5.090	5.570	5.425	5.724	5.090	5.570	5.425	5.724	ns
3.0-V LVTTL	4mA	GCLK	t_{co}	3.238	3.238	4.508	4.876	5.367	5.247	5.356	4.876	5.367	5.247	5.356	ns
		GCLK PLL	t_{co}	3.514	3.488	4.870	5.298	5.786	5.641	5.940	5.298	5.786	5.641	5.940	ns
	8mA	GCLK	t_{co}	3.108	3.108	4.339	4.704	5.205	5.086	5.239	4.704	5.205	5.086	5.239	ns
		GCLK PLL	t_{co}	3.403	3.377	4.740	5.164	5.648	5.504	5.801	5.164	5.648	5.504	5.801	ns
	12mA	GCLK	t_{co}	3.033	3.033	4.250	4.605	5.103	4.984	5.175	4.605	5.103	4.984	5.175	ns
		GCLK PLL	t_{co}	3.367	3.341	4.677	5.095	5.574	5.430	5.728	5.095	5.574	5.430	5.728	ns
	16mA	GCLK	t_{co}	3.000	3.010	4.188	4.536	5.053	4.934	5.152	4.536	5.053	4.934	5.152	ns
		GCLK PLL	t_{co}	3.349	3.323	4.648	5.067	5.546	5.401	5.700	5.067	5.546	5.401	5.700	ns

Table 1–117. EP3SE80 Column Pins Output Timing Parameters (Part 3 of 4)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{co}	3.170	3.410	4.807	5.209	5.723	5.583	5.883	5.334	5.848	5.709	5.958	ns
		GCLK PLL	t_{co}	1.346	1.525	1.963	2.060	2.271	2.282	2.308	2.166	2.380	2.390	2.296	ns
	6mA	GCLK	t_{co}	3.166	3.407	4.808	5.211	5.727	5.587	5.887	5.336	5.852	5.713	5.962	ns
		GCLK PLL	t_{co}	1.342	1.522	1.964	2.062	2.275	2.286	2.312	2.168	2.384	2.394	2.300	ns
	8mA	GCLK	t_{co}	3.156	3.396	4.797	5.200	5.715	5.575	5.875	5.325	5.840	5.701	5.950	ns
		GCLK PLL	t_{co}	1.332	1.511	1.953	2.051	2.263	2.274	2.300	2.157	2.372	2.382	2.288	ns
	10mA	GCLK	t_{co}	3.154	3.394	4.795	5.197	5.713	5.573	5.873	5.323	5.838	5.699	5.948	ns
		GCLK PLL	t_{co}	1.330	1.509	1.951	2.048	2.261	2.272	2.298	2.155	2.370	2.380	2.286	ns
	12mA	GCLK	t_{co}	3.154	3.395	4.798	5.202	5.718	5.578	5.878	5.327	5.844	5.705	5.954	ns
		GCLK PLL	t_{co}	1.330	1.510	1.954	2.053	2.266	2.277	2.303	2.159	2.376	2.386	2.292	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{co}	3.158	3.398	4.795	5.197	5.712	5.572	5.872	5.322	5.837	5.698	5.947	ns
		GCLK PLL	t_{co}	1.334	1.513	1.951	2.048	2.260	2.271	2.297	2.154	2.369	2.379	2.285	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{co}	3.184	3.427	4.840	5.245	5.762	5.622	5.922	5.370	5.887	5.748	5.997	ns
		GCLK PLL	t_{co}	1.360	1.542	1.996	2.096	2.310	2.321	2.347	2.202	2.419	2.429	2.335	ns
	6mA	GCLK	t_{co}	3.170	3.413	4.828	5.234	5.752	5.612	5.912	5.360	5.878	5.739	5.988	ns
		GCLK PLL	t_{co}	1.346	1.528	1.984	2.085	2.300	2.311	2.337	2.192	2.410	2.420	2.326	ns
	8mA	GCLK	t_{co}	3.158	3.400	4.811	5.216	5.734	5.594	5.894	5.342	5.860	5.721	5.970	ns
		GCLK PLL	t_{co}	1.334	1.515	1.967	2.067	2.282	2.293	2.319	2.174	2.392	2.402	2.308	ns
	10mA	GCLK	t_{co}	3.158	3.400	4.814	5.220	5.738	5.598	5.898	5.346	5.865	5.726	5.975	ns
		GCLK PLL	t_{co}	1.334	1.515	1.970	2.071	2.286	2.297	2.323	2.178	2.397	2.407	2.313	ns
	12mA	GCLK	t_{co}	3.154	3.396	4.807	5.212	5.731	5.591	5.891	5.339	5.857	5.718	5.967	ns
		GCLK PLL	t_{co}	1.330	1.511	1.963	2.063	2.279	2.290	2.316	2.171	2.389	2.399	2.305	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	8mA	GCLK	t_{co}	3.158	3.398	4.800	5.203	5.719	5.579	5.879	5.328	5.844	5.705	5.954	ns
		GCLK PLL	t_{co}	1.334	1.513	1.956	2.054	2.267	2.278	2.304	2.160	2.376	2.386	2.292	ns
	16mA	GCLK	t_{co}	3.159	3.400	4.808	5.213	5.730	5.590	5.890	5.338	5.856	5.717	5.966	ns
		GCLK PLL	t_{co}	1.335	1.515	1.964	2.064	2.278	2.289	2.315	2.170	2.388	2.398	2.304	ns

Table 1–118 lists the EP3SE80 row pins output timing parameters for differential I/O standards.

Table 1–118. EP3SE80 Row Pins Output Timing Parameters (Part 1 of 3)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
LVDS	—	GCLK	t_{co}	2.744	2.932	4.083	4.440	4.901	4.771	5.049	4.540	5.002	4.873	5.107	ns
		GCLK PLL	t_{co}	0.931	1.057	1.249	1.300	1.458	1.480	1.486	1.382	1.545	1.563	1.456	ns
LVDS_E_1R	—	GCLK	t_{co}	3.136	3.376	4.754	5.156	5.664	5.526	5.797	5.281	5.790	5.652	5.871	ns
		GCLK PLL	t_{co}	1.333	1.511	1.930	2.026	2.231	2.245	2.243	2.133	2.343	2.352	2.229	ns
LVDS_E_3R	—	GCLK	t_{co}	3.118	3.366	4.792	5.202	5.718	5.580	5.851	5.332	5.851	5.713	5.932	ns
		GCLK PLL	t_{co}	1.315	1.501	1.968	2.072	2.285	2.299	2.297	2.184	2.404	2.413	2.290	ns
MINI-LVDS	—	GCLK	t_{co}	2.744	2.932	4.083	4.440	4.901	4.771	5.049	4.540	5.002	4.873	5.107	ns
		GCLK PLL	t_{co}	0.931	1.057	1.249	1.300	1.458	1.480	1.486	1.382	1.545	1.563	1.456	ns
MINI-LVDS_E_1R	—	GCLK	t_{co}	3.136	3.376	4.754	5.156	5.664	5.526	5.797	5.281	5.790	5.652	5.871	ns
		GCLK PLL	t_{co}	1.333	1.511	1.930	2.026	2.231	2.245	2.243	2.133	2.343	2.352	2.229	ns
MINI-LVDS_E_3R	—	GCLK	t_{co}	3.118	3.366	4.792	5.202	5.718	5.580	5.851	5.332	5.851	5.713	5.932	ns
		GCLK PLL	t_{co}	1.315	1.501	1.968	2.072	2.285	2.299	2.297	2.184	2.404	2.413	2.290	ns
RSDS	—	GCLK	t_{co}	2.744	2.932	4.083	4.440	4.901	4.771	5.049	4.540	5.002	4.873	5.107	ns
		GCLK PLL	t_{co}	0.931	1.057	1.249	1.300	1.458	1.480	1.486	1.382	1.545	1.563	1.456	ns
RSDS_E_1R	—	GCLK	t_{co}	3.136	3.376	4.754	5.156	5.664	5.526	5.797	5.281	5.790	5.652	5.871	ns
		GCLK PLL	t_{co}	1.333	1.511	1.930	2.026	2.231	2.245	2.243	2.133	2.343	2.352	2.229	ns
RSDS_E_3R	—	GCLK	t_{co}	3.118	3.366	4.792	5.202	5.718	5.580	5.851	5.332	5.851	5.713	5.932	ns
		GCLK PLL	t_{co}	1.315	1.501	1.968	2.072	2.285	2.299	2.297	2.184	2.404	2.413	2.290	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{co}	3.162	3.409	4.828	5.236	5.751	5.613	5.884	5.365	5.880	5.742	5.961	ns
		GCLK PLL	t_{co}	1.359	1.544	2.004	2.106	2.318	2.332	2.330	2.217	2.433	2.442	2.319	ns
	6mA	GCLK	t_{co}	3.148	3.395	4.815	5.223	5.738	5.600	5.871	5.351	5.867	5.729	5.948	ns
		GCLK PLL	t_{co}	1.345	1.530	1.991	2.093	2.305	2.319	2.317	2.203	2.420	2.429	2.306	ns
	8mA	GCLK	t_{co}	3.144	3.391	4.813	5.223	5.739	5.601	5.872	5.351	5.869	5.731	5.950	ns
		GCLK PLL	t_{co}	1.341	1.526	1.989	2.093	2.306	2.320	2.318	2.203	2.422	2.431	2.308	ns

Table 1–126. EP3SE110 Row Pins Input Timing Parameters (Part 3 of 3)

I/O Standard	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
			Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{su}	-0.781	-0.827	-1.178	-1.275	-1.384	-1.333	-1.673	-1.273	-1.378	-1.329	-1.712	ns
		t_h	0.907	0.969	1.379	1.502	1.631	1.568	1.912	1.509	1.636	1.573	1.952	ns
	GCLK PLL	t_{su}	1.124	1.141	1.827	2.068	2.299	2.178	2.118	2.089	2.323	2.199	2.170	ns
		t_h	-0.861	-0.861	-1.411	-1.601	-1.780	-1.688	-1.617	-1.610	-1.792	-1.699	-1.665	ns

Table 1–127 lists the EP3SE110 column pins output timing parameters for differential I/O standards.

Table 1–127. EP3SE110 Column Pins Output Timing Parameters (Part 1 of 4)

I/O Standard	Current Strength	Clock	Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS_E_1R	—	GCLK	t_{co}	3.152	3.387	4.757	5.155	5.666	5.526	5.826	5.278	5.789	5.650	5.899	ns
		GCLK PLL	t_{co}	1.328	1.502	1.913	2.006	2.214	2.225	2.251	2.110	2.321	2.331	2.237	ns
LVDS_E_3R	—	GCLK	t_{co}	3.148	3.390	4.804	5.210	5.728	5.588	5.888	5.337	5.855	5.716	5.965	ns
		GCLK PLL	t_{co}	1.324	1.505	1.960	2.061	2.276	2.287	2.313	2.169	2.387	2.397	2.303	ns
MINI-LVDS_E_1R	—	GCLK	t_{co}	3.152	3.387	4.757	5.155	5.666	5.526	5.826	5.278	5.789	5.650	5.899	ns
		GCLK PLL	t_{co}	1.328	1.502	1.913	2.006	2.214	2.225	2.251	2.110	2.321	2.331	2.237	ns
MINI-LVDS_E_3R	—	GCLK	t_{co}	3.148	3.390	4.804	5.210	5.728	5.588	5.888	5.337	5.855	5.716	5.965	ns
		GCLK PLL	t_{co}	1.324	1.505	1.960	2.061	2.276	2.287	2.313	2.169	2.387	2.397	2.303	ns
RSDS_E_1R	—	GCLK	t_{co}	3.152	3.387	4.757	5.155	5.666	5.526	5.826	5.278	5.789	5.650	5.899	ns
		GCLK PLL	t_{co}	1.328	1.502	1.913	2.006	2.214	2.225	2.251	2.110	2.321	2.331	2.237	ns
RSDS_E_3R	—	GCLK	t_{co}	3.148	3.390	4.804	5.210	5.728	5.588	5.888	5.337	5.855	5.716	5.965	ns
		GCLK PLL	t_{co}	1.324	1.505	1.960	2.061	2.276	2.287	2.313	2.169	2.387	2.397	2.303	ns

Table 1–152 and Table 1–153 list the periphery clock timing parameters for EP3SL70 devices.

Table 1–152. EP3SL70 Column Pin Periphery Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.465	1.468	2.142	2.410	2.792	2.673	3.220	2.410	2.802	2.673	3.220	ns
t_{COUT}	1.465	1.468	2.142	2.410	2.792	2.673	3.220	2.410	2.802	2.673	3.220	ns
t_{PLLCIN}	-0.068	-0.083	-0.330	-0.370	-0.334	-0.288	-0.133	-0.370	0.273	-0.288	-0.133	ns
$t_{PLLCOUT}$	-0.068	-0.083	-0.330	-0.370	-0.334	-0.288	-0.133	-0.370	0.273	-0.288	-0.133	ns

Table 1–153. EP3SL70 Row Pin Periphery Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.482	1.558	2.227	2.488	2.851	2.727	3.031	2.539	2.905	2.777	3.056	ns
t_{COUT}	1.400	1.467	2.082	2.325	2.670	2.556	2.872	2.369	2.716	2.598	2.897	ns
t_{PLLCIN}	-0.019	0.039	-0.225	-0.302	-0.291	-0.235	-0.295	-0.261	0.376	-0.188	-0.257	ns
$t_{PLLCOUT}$	-0.101	-0.052	-0.367	-0.465	-0.472	-0.406	-0.454	-0.431	0.187	-0.367	-0.416	ns

EP3SL110 Clock Timing Parameters

Table 1–154 and Table 1–155 list the global clock timing parameters for EP3SL110 devices.

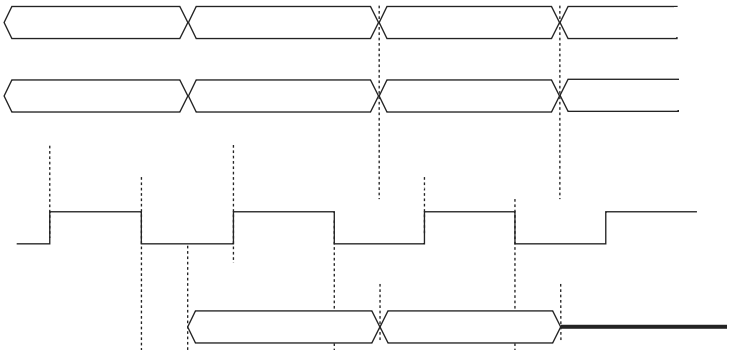
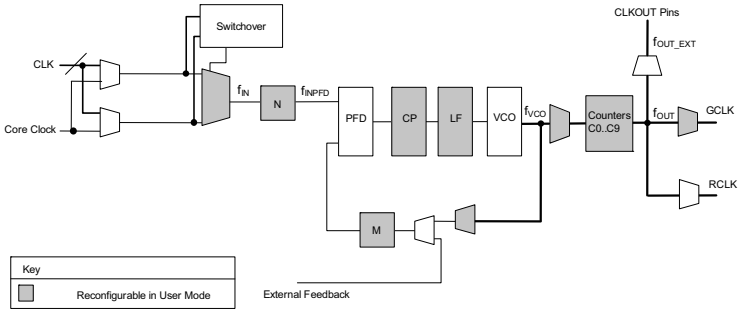
Table 1–154. EP3SL110 Column Pin Global Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Units
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.909	1.907	2.674	2.936	3.285	3.182	3.700	2.936	3.285	3.182	3.700	ns
t_{COUT}	1.909	1.907	2.674	2.936	3.285	3.182	3.700	2.936	3.285	3.182	3.700	ns
t_{PLLCIN}	-0.048	-0.050	-0.274	-0.330	-0.290	-0.251	-0.032	-0.330	-0.290	-0.251	-0.032	ns
$t_{PLLCOUT}$	-0.048	-0.050	-0.274	-0.330	-0.290	-0.251	-0.032	-0.330	-0.290	-0.251	-0.032	ns

Table 1–155. EP3SL110 Row Pin Global Clock Timing Specifications

Parameter	Fast Model		C2	C3	C4	C4L		I3	I4	I4L		Unit
	Industrial	Commercial	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 1.1 V	V_{CCL}= 0.9 V	
t_{CIN}	1.882	2.014	2.754	2.975	3.344	3.221	3.511	3.062	3.413	3.287	3.551	ns
t_{COUT}	1.800	1.923	2.612	2.812	3.163	3.050	3.352	2.892	3.224	3.108	3.392	ns
t_{PLLCIN}	-0.002	0.059	-0.202	-0.271	-0.231	-0.184	-0.212	-0.219	-0.184	-0.138	-0.260	ns
$t_{PLLCOUT}$	-0.084	-0.032	-0.347	-0.434	-0.412	-0.355	-0.371	-0.389	-0.373	-0.317	-0.419	ns

Table 1.

Glossary Table (Part 2 of 4)		
Letter	**Subject**	**Definitions**
J	J	High-Speed I/O Block: Deserialization factor (width of parallel data bus).
	JTAG Timing Specifications	JTAG Timing Specifications are in the following figure: 
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	PLL Specifications	The block diagram shown in the following figure highlights the PLL Specification parameters: Diagram of PLL Specifications (1)  **Note:** (1) CoreClock can only be fed by dedicated clock input pins or PLL outputs.
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to Stratix III device).