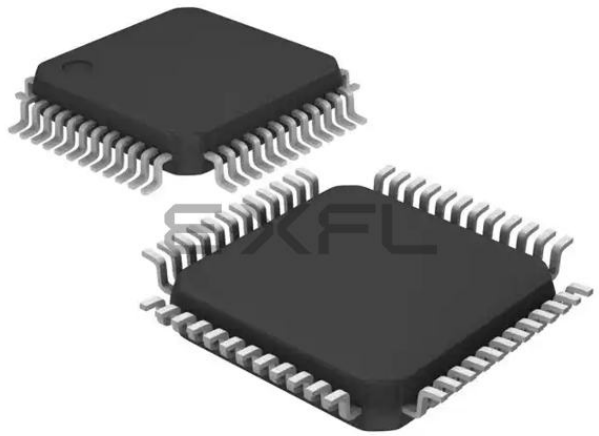

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT
Number of I/O	36
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc123lc2an1

1 GENERAL DESCRIPTION

The NuMicro® NUC123 series is a new 32-bit Cortex®-M0 microcontroller with USB 2.0 Full-speed devices and a 10-bit ADC. The NUC123 series provides the high 72 MHz operating speed, large 20 Kbytes SRAM, 8 USB endpoints and three sets of SPI controllers, which make it powerful in USB communication and data processing. The NUC123 series is ideal for industrial control, consumer electronics, and communication system applications such as printers, touch panel, gaming keyboard, gaming joystick, USB audio, PC peripherals, and alarm systems.

The NUC123 series runs up to 72 MHz and supports 32-bit multiplier, structure NVIC (Nested Vector Interrupt Control), dual-channel APB and PDMA (Peripheral Direct Memory Access) with CRC function. Besides, the NUC123 series is equipped with 36/68 Kbytes Flash memory, 12/20 Kbytes SRAM, and 4 Kbytes loader ROM for the ISP. It operates at a wide voltage range of 2.5V ~ 5.5V and temperature range of -40℃ ~ +105℃ and -40℃ ~ +85℃. It is also equipped with plenty of peripheral devices, such as 8-channel 10-bit ADC, UART, SPI, I^2C, I^2S, USB 2.0 FS devices, and offers low-voltage reset and Brown-out detection, PWM (Pulse-width Modulation), capture and compare features, four sets of 32-bit timers, Watchdog Timer, and internal RC oscillator. All these peripherals have been incorporated into the NUC123 series to reduce component count, board space and system cost.

Additionally, the NUC123 series is equipped with ISP (In-System Programming), IAP (In-Application-Programming) and ICP (In-Circuit Programming) functions, which allows the user to update the program under software control through the on-chip connectivity interface, such as SWD, UART and USB.

Product Line	UART	SPI	I^2C	USB	PS/2	I^2S	PWM	ADC
NUC123	2	3	2	1	1	1	4	8

Table 1-1 Key Features Support Table

  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two DMA requests, one for transmitting and the other for receiving
- PS/2 Device Controller
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - S/W override bus
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12 Mbps
  - On-chip USB transceiver
  - Provides 1 interrupt source with 4 interrupt events
  - Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provides 8 programmable endpoints
  - Includes 512 bytes internal SRAM as USB buffer
  - Provides remote wake-up capability
- ADC
  - 10-bit SAR ADC with 150K SPS (for NUC123xxxANx)
  - 10-bit SAR ADC with 200K SPS (for NUC123xxxAEx)
  - Up to 8-ch single-end input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion start by software programming or external input
  - Supports PDMA mode
- Brown-out detector
  - With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 2.0 V
- One built-in LDO
- Operating Temperature: -40℃~85℃ (for NUC123xxxANx)
- Operating Temperature: -40℃~105℃ (for NUC123xxxAEx)
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin
  - LQFP 48-pin
  - QFN 33-pin

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~20 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface

4.3.2.2 NuMicro® NUC123LxxAEx LQFP 48 pin

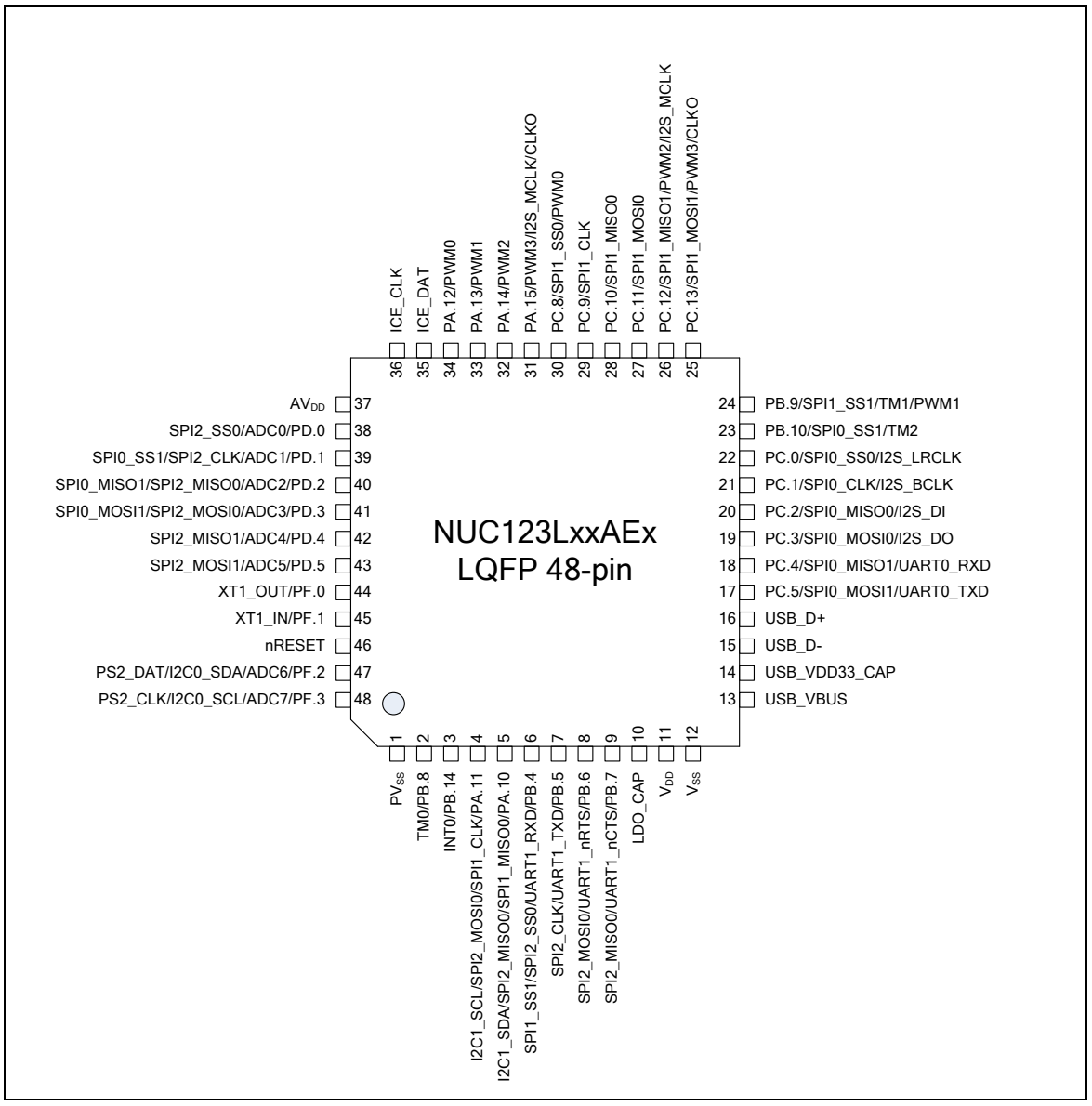

Figure 4-6 NuMicro® NUC123LxxAEx LQFP 48-pin Diagram

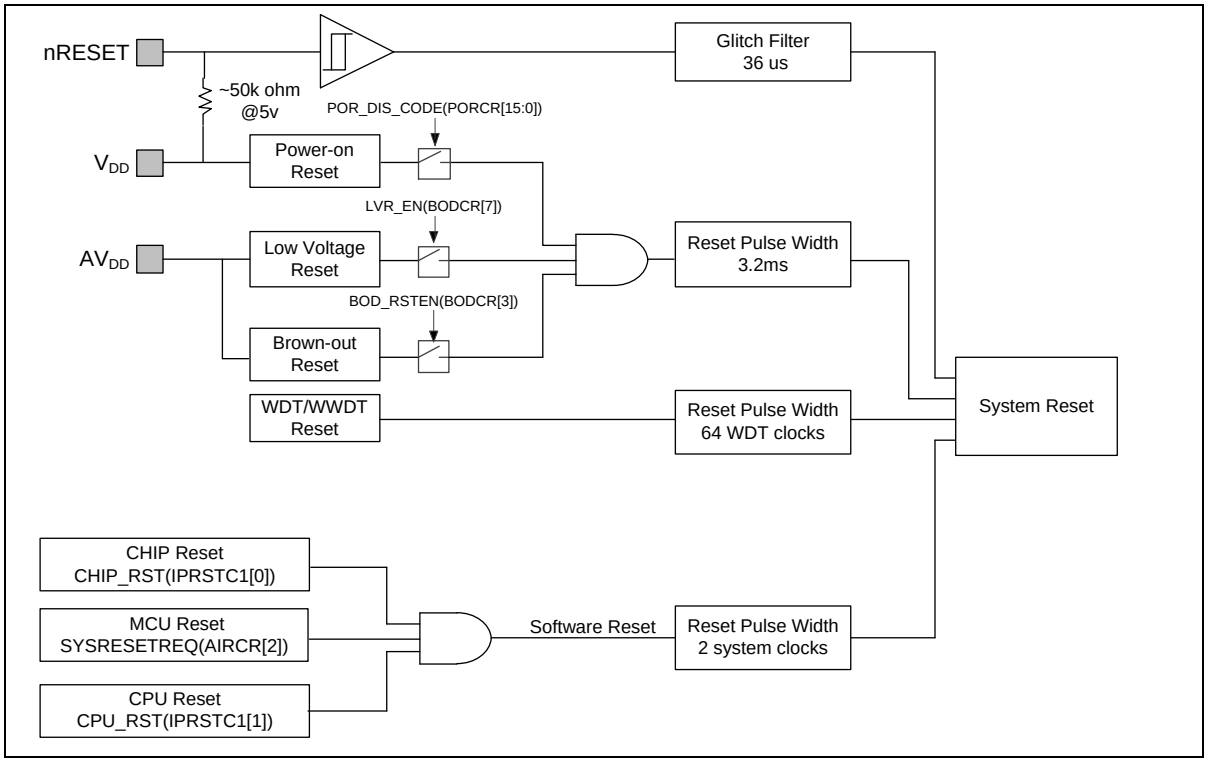

Figure 6-2 System Reset Resources

There are a total of 8 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M0 only; the other reset sources will reset Cortex®-M0 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6-1.

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	CHIP	MCU	CPU
RSTSRC	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIP_RST (IPRSTC1[0])	0x0	-	-	-	-	-	-	-
BOD_EN (BODCR[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	-
BOD_VL (BODCR[2:1])								
BOD_RSTEN (BODCR[3])								
XTL12M_EN (PWRCON [0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
WDT_EN (APBCLK[0])	0x1	-	0x1	-	-	0x1	-	-
HCLK_S (CLKSEL0[2:0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-

WDT_S (CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-
XTL12M_STB (CLKSTATUS[0])	0x0	-	-	-	-	-	-	-
PLL_STB (CLKSTATUS[2])	0x0	-	-	-	-	-	-	-
OSC10K_STB (CLKSTATUS[3])	0x0	-	-	-	-	-	-	-
OSC22M_STB (CLKSTATUS[4])	0x0	-	-	-	-	-	-	-
CLK_SW_FAIL (CLKSTATUS[7])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
WTE (WTCR[7])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0		
WTCR	0x0700	0x0700	0x0700	0x0700	0x0700	0x0700	-	-
WTCRALT	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDTRLD	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDTCR	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	-
WWDTSR	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDTCVR	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	-	-
BS (ISPCON[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
DFBADR	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	-
CBS (ISPSTA[2:1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
VECMAP (ISPSTA[20:9]) (NUC123xxxAEx Only)	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value							-
FMC Registers	Reset Value							
Note: '-' means that the value of register keeps original setting.								

Table 6-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 36 us (glitch filter), chip will be

6.2.4 System Power Distribution

In this chip, power distribution is divided into three segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.

The outputs of internal voltage regulators, LDO and USB_VDD33_CAP, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 6-8 shows the power distribution of the NuMicro® NUC123 series.

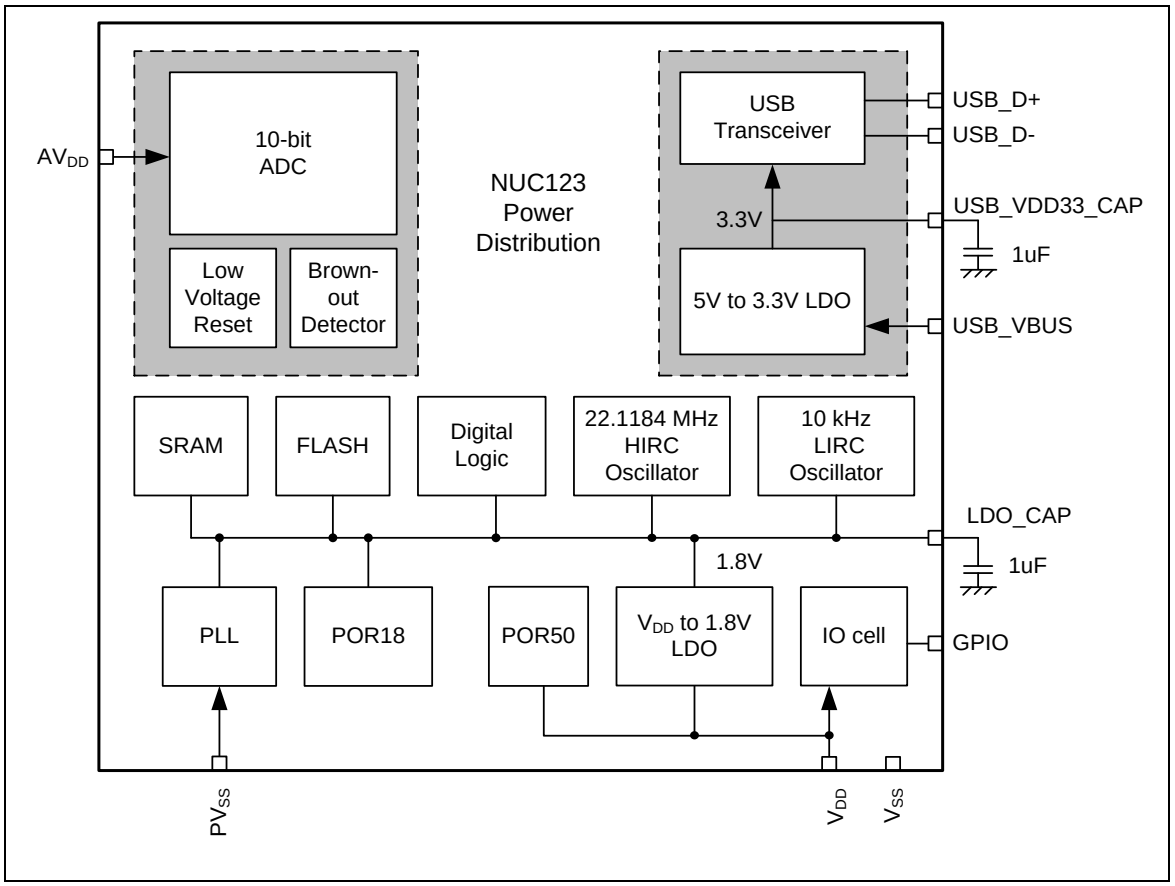

Figure 6-8 NuMicro® NUC123 Power Distribution Diagram

6.2.5 System Memory Map

The NuMicro® NUC123 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the Table 6-5. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripherals. The NuMicro® NUC123 Series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_FFFF	FLASH_BA	FLASH Memory Space (64KB)
0x2000_0000 – 0x2000_4FFF	SRAM_BA	SRAM Memory Space (20KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog/Window Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4010_0000 – 0x4010_3FFF	PS2_BA	PS/2 Interface Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4013_0000 – 0x4013_3FFF	SPI2_BA	SPI2 with master/slave function Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x401A_0000 – 0x401A_3FFF	I2S_BA	I^2S Interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers

6.3.2 System Clock and SysTick Clock

The system clock has 5 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown in Figure 6-11.

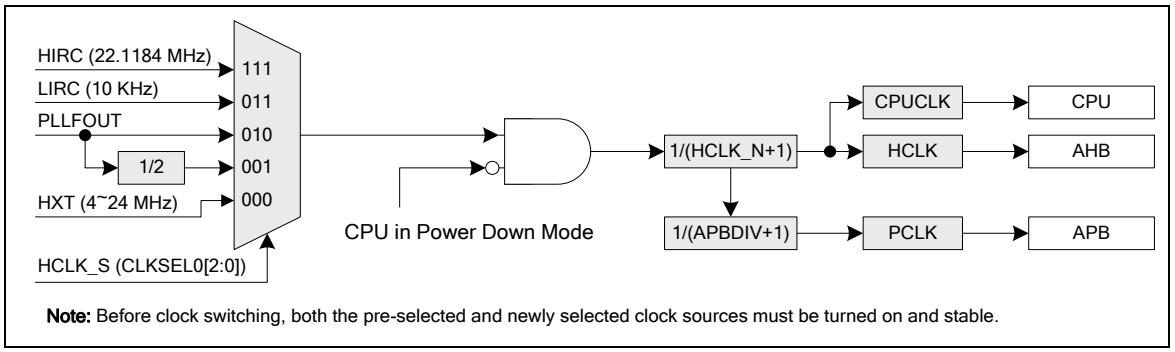

Figure 6-11 System Clock Block Diagram

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in Figure 6-12.

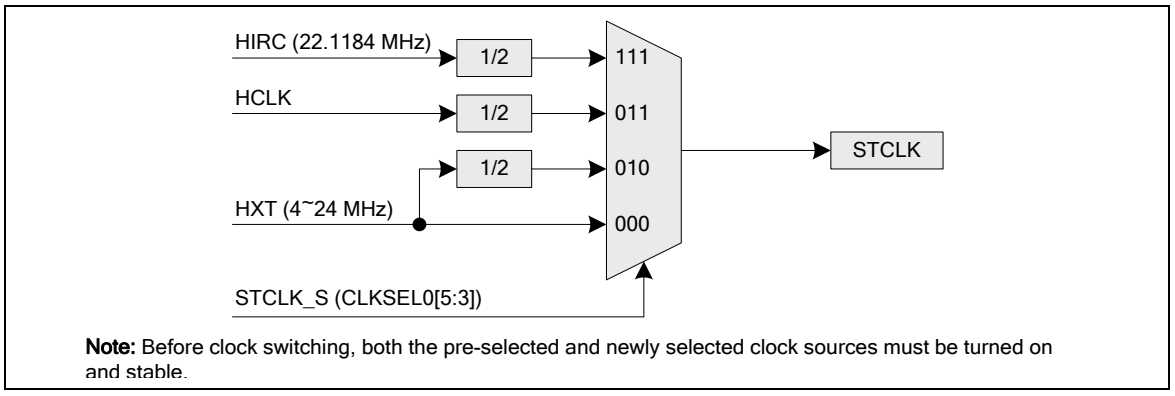

Figure 6-12 SysTick Clock Control Block Diagram

6.3.3 Peripherals Clock

The peripherals clock had different clock source switch setting depending on different peripherals. Please refer to the CLKSEL1 and CLKSEL2 register description in **錯誤! 找不到參照來源。**.

6.3.4 Power-down Mode Clock

When chip enters into Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clock are still active in Power-down mode.

The clocks kept active are listed below:

- Clock Generator
  - Internal 10 kHz low speed oscillator clock

6.14 Serial Peripheral Interface (SPI)

6.14.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. This NuMicro® NUC123 series contains up to three sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be configured as a Master or a Slave device.

This controller supports variable serial clock function for special application and it also supports 2-bit Transfer mode. The controller also supports PDMA function to access the data buffer and also supports Dual I/O transfer mode.

6.14.2 Features

- Up to three sets of SPI controllers
- Supports Master or Slave mode operation
- Supports 2-bit Transfer mode
- Supports Dual I/O transfer mode
- Configurable bit length of a transfer word from 8 to 32-bit
- Provide separate 8-layer depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Up to two slave select lines in Master mode
- Supports Byte Reorder function
- Supports configurable suspend interval in Master mode
- Variable output serial clock frequency in Master mode
- Supports PDMA transfer
- Supports 3-Wire, no slave select signal, bi-direction interface

7 ELECTRICAL CHARACTERISTICS (NUC123XXXANX)

7.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{DD} - V_{SS}$	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+85	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}		120	mA
I_{IO}	Maximum Current sunk by a I/O pin		35	mA
	Maximum Current sourced by a I/O pin		35	mA
	Maximum Current sunk by total I/O pins		100	mA
	Maximum Current sourced by total I/O pins		100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affect the lift and reliability of the device.

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
at 4 MHz	I_{DD10}		3		mA	V_{DD} = 5V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
	I_{DD11}		4		mA	V_{DD} = 3V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{DD12}		2		mA	V_{DD} = 3V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
Operating current Idle mode at 72 MHz	I_{IDLE1}		29		mA	V_{DD} = 5.5V at 72 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{IDLE2}		14		mA	V_{DD} = 5.5V at 72 MHz, All IP Disabled and PLL Enabled, XTAL = 12 MHz
	I_{IDLE3}		28		mA	V_{DD} = 3V at 72 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{IDLE4}		13		mA	V_{DD} = 3V at 72 MHz, All IP Disabled and PLL Enabled, XTAL=12 MHz
Operating current Idle mode at 12 MHz	I_{IDLE5}		6		mA	V_{DD} = 5.5V at 12 MHz, All IP Enabled and PLL Disabled, XTAL = 12 MHz
	I_{IDLE6}		3		mA	V_{DD} = 5.5V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
	I_{IDLE7}		5		mA	V_{DD} = 3V at 12 MHz, All IP Enabled and PLL Disabled, XTAL = 12 MHz
	I_{IDLE8}		2		mA	V_{DD} = 3 V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
Operating current Idle mode at 4 MHz	I_{IDLE9}		3		mA	V_{DD} = 5V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{IDLE10}		2		mA	V_{DD} = 5V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
	I_{IDLE11}		2		mA	V_{DD} = 3V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{IDLE12}		1		mA	V_{DD} = 3V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Source Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V
Brown-out voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brown-out voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brown-out voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.7	3.8	3.9	V	
Brown-out voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.4	4.5	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5V - 5.5V

Notes:

1. nRESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, 5he transition current reaches its maximum value when V_{IN} approximates to 2V.

8 ELECTRICAL CHARACTERISTICS (NUC123XXXAEX)

8.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{DD} - V_{SS}$	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+105	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}		120	mA
I_{IO}	Maximum Current sunk by a I/O pin		35	mA
	Maximum Current sourced by a I/O pin		35	mA
	Maximum Current sunk by total I/O pins		100	mA
	Maximum Current sourced by total I/O pins		100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affect the lift and reliability of the device.

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Source Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SR21}	-24	-28	-32	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V
Brown-out voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brown-out voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brown-out voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.5	3.7	3.9	V	
Brown-out voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.2	4.4	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5V - 5.5V

Notes:

1. nRESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, 5he transition current reaches its maximum value when V_{IN} approximates to 2V.

8.3.3 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25℃; V_{DD} =5 V	-1	-	+1	%
	-40℃~+105℃; V_{DD}=2.5 V~5.5 V	-3	-	+3	%
Operation Current	V_{DD} =5 V	-	500	-	uA

8.3.4 Internal 10 kHz Low Speed Oscillator

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25℃; V_{DD} =5 V	-30	-	+30	%
	-40℃~+105℃; V_{DD}=2.5 V~5.5 V	-50	-	+50	%

Note: Internal operation voltage comes from LDO.

C_{bp}	External Bypass Capacitor			1.0	-	uF

8.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage		1.62	1.8	1.98	V[1]
N_{ENDUR}	Endurance		20000			cycles[2]
T_{RET}	Data Retention	At 25℃	100			year
T_{ERASE}	Page Erase Time			20		ms
T_{MER}	Mass Erase Time			40		ms
T_{PROG}	Program Time			35		μs
I_{DD1}	Read Current		-	TBD		mA/MHz
I_{DD2}	Program/Erase Current				7	mA
I_{PD}	Power Down Current		-	1	20	μA

Note1: V_{DD} is source from chip LDO output voltage.

Note2: Number of program/erase cycles.

Note3: This table is guaranteed by design, not test in production.

8.6 SPI Dynamic Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
SPI Master mode (V_{DD} = 4.5V ~ 5.5V, 30pF loading Capacitor)					
t_{DS}	Data setup time	4	2	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	7	11	ns
SPI Master mode (V_{DD} = 3.0V ~ 3.6V, 30pF loading Capacitor)					
t_{DS}	Data setup time	5	3	-	ns
t_{DH}	Data hold time	0	-	-	ns
t_V	Data output valid time	-	13	18	ns
SPI Slave mode (V_{DD} = 4.5V ~ 5.5V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+4	-	-	ns
t_V	Data output valid time	-	2*PCLK+11	2*PCLK+19	ns
SPI Slave mode (V_{DD} = 3.0V ~ 3.6V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2*PCLK+6	-	-	ns
t_V	Data output valid time	-	2*PCLK+19	2*PCLK+25	ns

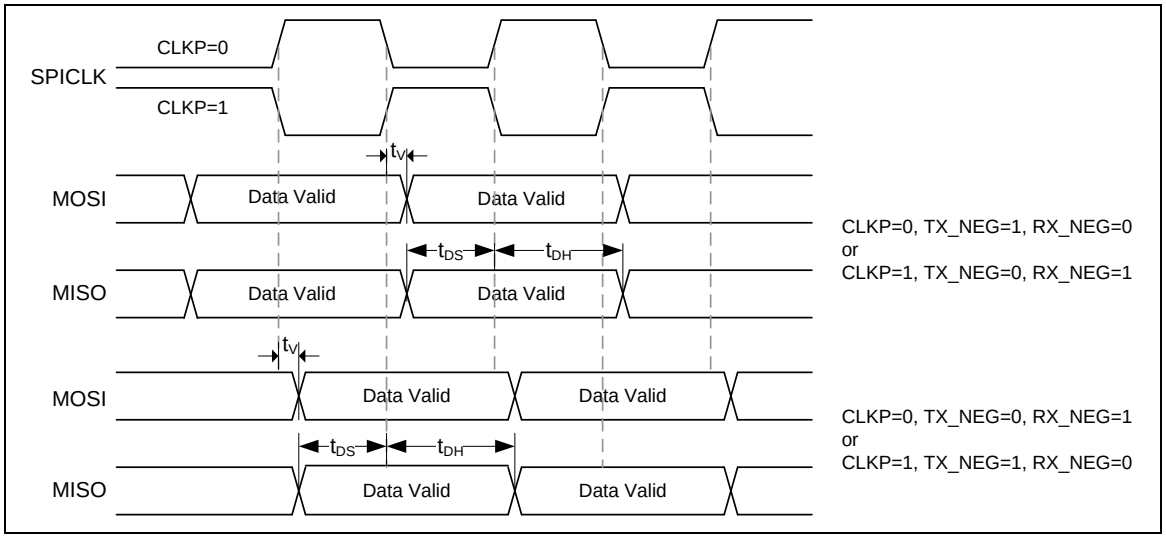

Figure 8-2 SPI Master Dynamic Characteristics timing