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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PS2, PWM, WDT
Number of I/O	47
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nuc123sc2an1

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SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4.3 NuMicro® NUC123 Series Pin Configuration

4.3.1 NuMicro® NUC123xxxANx Pin Diagram

4.3.1.1 NuMicro® NUC123SxxANx LQFP 64 pin

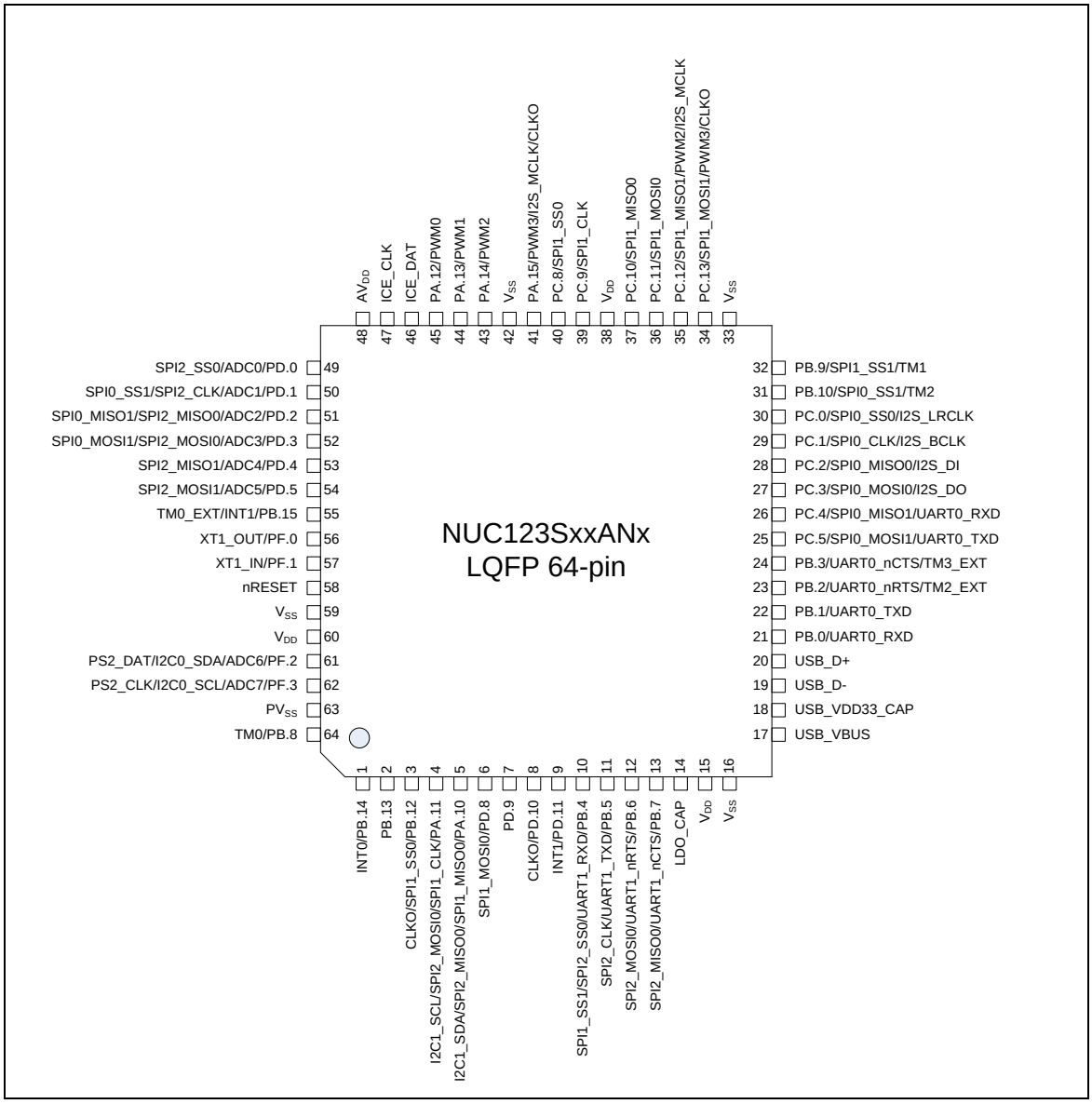


Figure 4-2 NuMicro® NUC123SxxANx LQFP 64-pin Diagram

4.3.1.3 NuMicro® NUC123ZxxANx QFN 33 pin

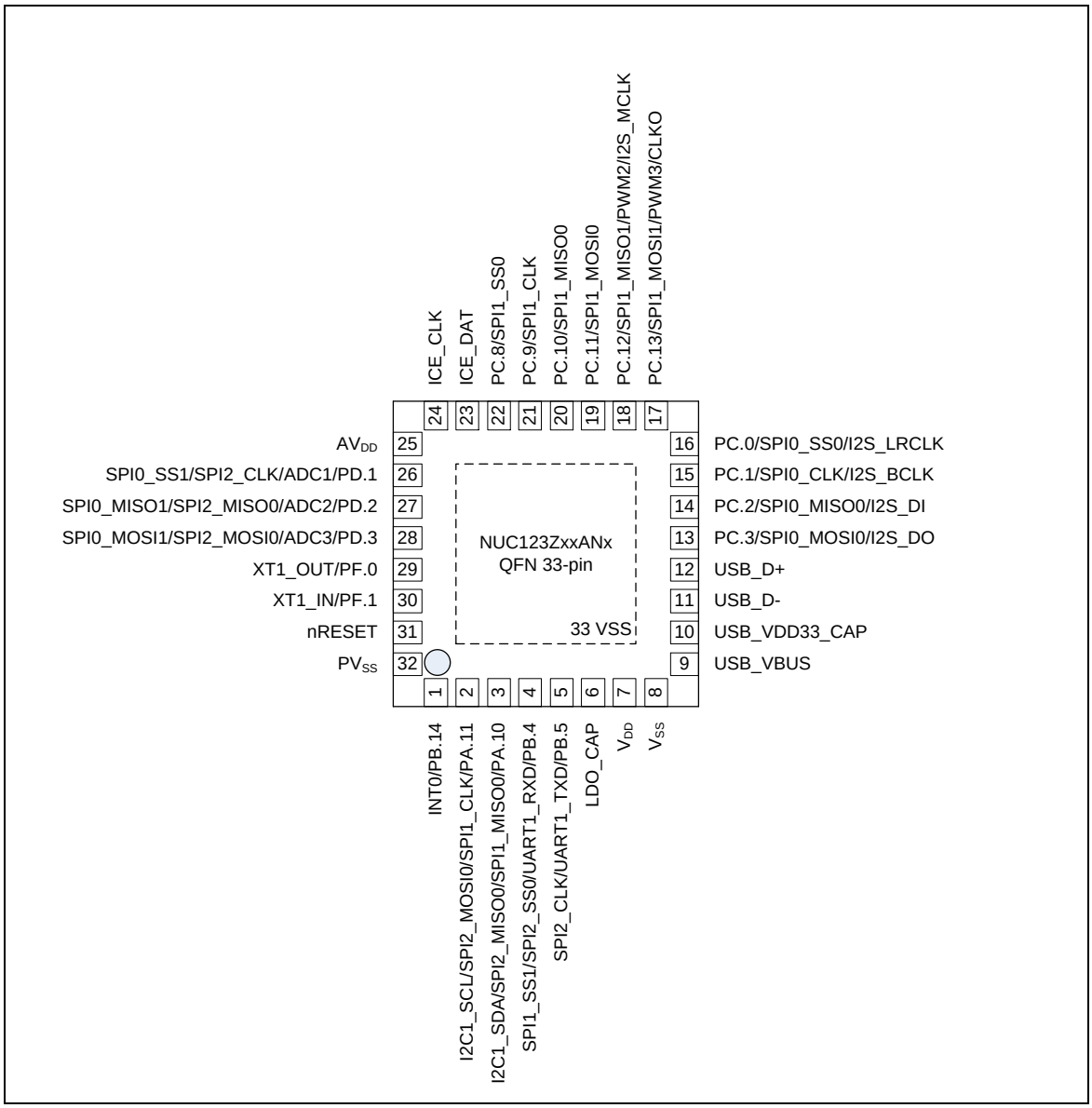


Figure 4-4 NuMicro® NUC123ZxxANx QFN 33-pin Diagram

4.3.2.3 NuMicro® NUC123ZxxAEx QFN 33 pin

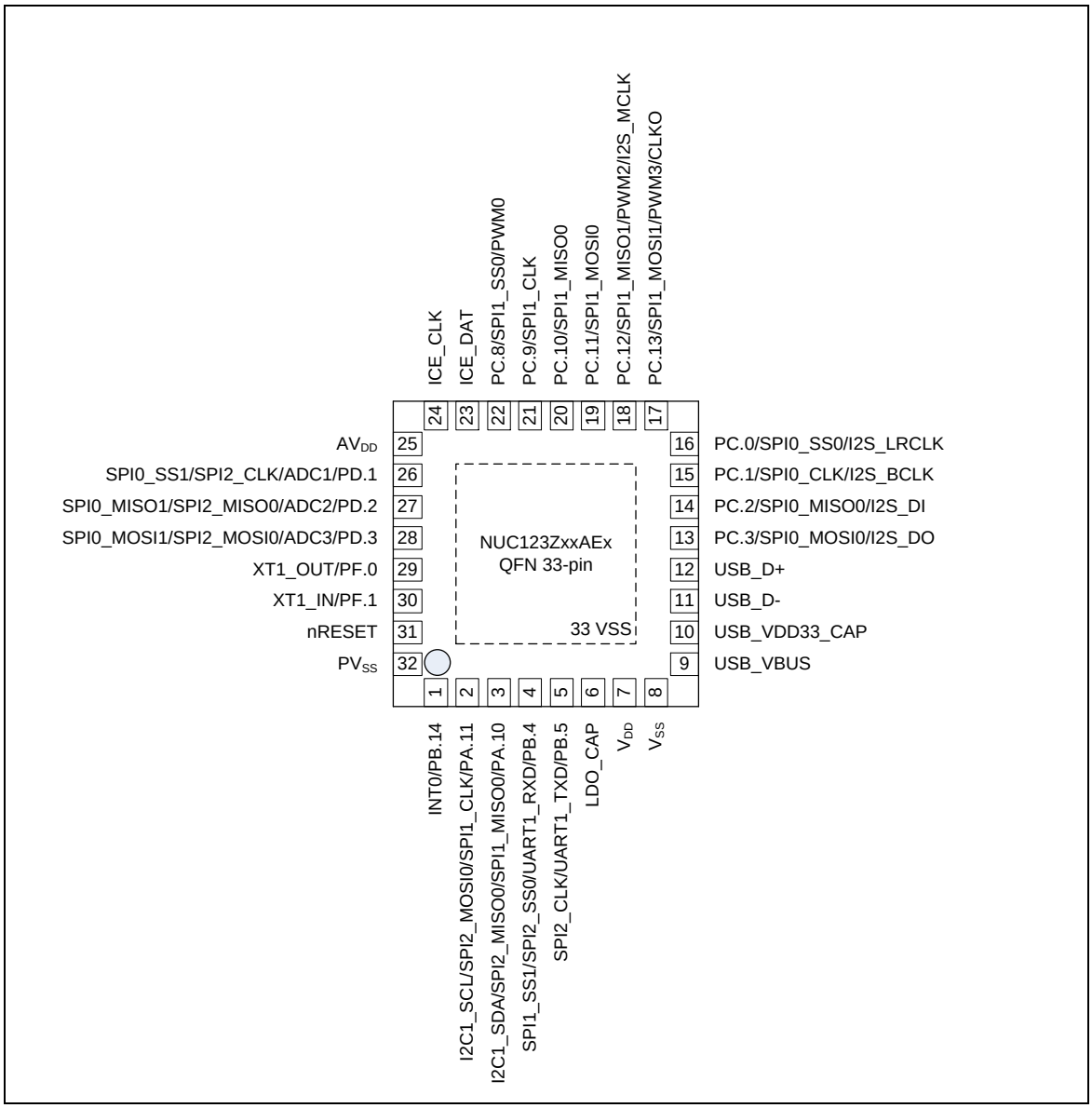


Figure 4-7 NuMicro® NUC123ZxxAEx QFN 33-pin Diagram

5 BLOCK DIAGRAM

5.1 NuMicro® NUC123 Block Diagram

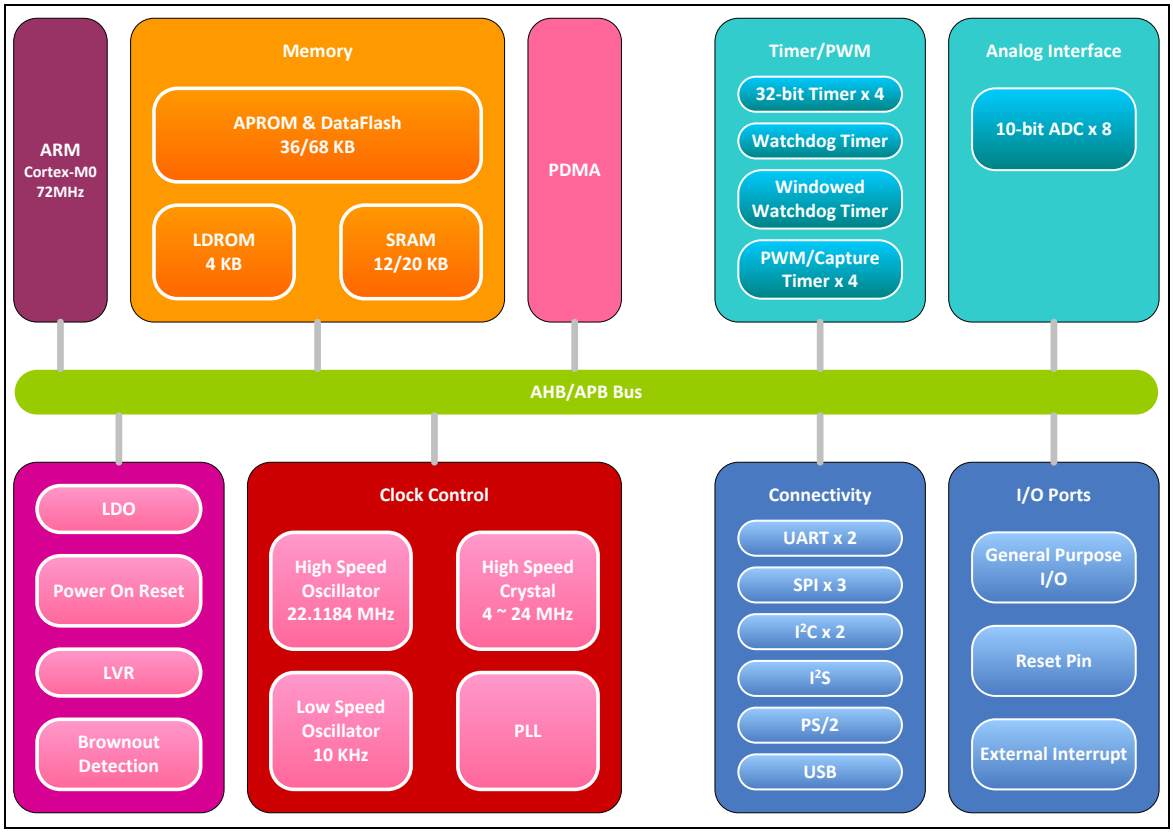


Figure 5-1 NuMicro® NUC123 Block Diagram

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-Maskable Interrupt (NMI) input
- Supports both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) with ultra-low power sleep mode

- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface providing simple integration to all system peripherals and memory
  - Single 32-bit slave port supporting the DAP (Debug Access Port)

Figure 6-4 Power-on Reset (POR) Waveform

6.2.2.3 *Low Voltage Reset (LVR)*

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVR_EN (BODCR[7]) to 1, after 100us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time (16*HCLK cycles), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time. The RSTS_RESET (RSTSRC[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6-5 shows the Low Voltage Reset waveform.

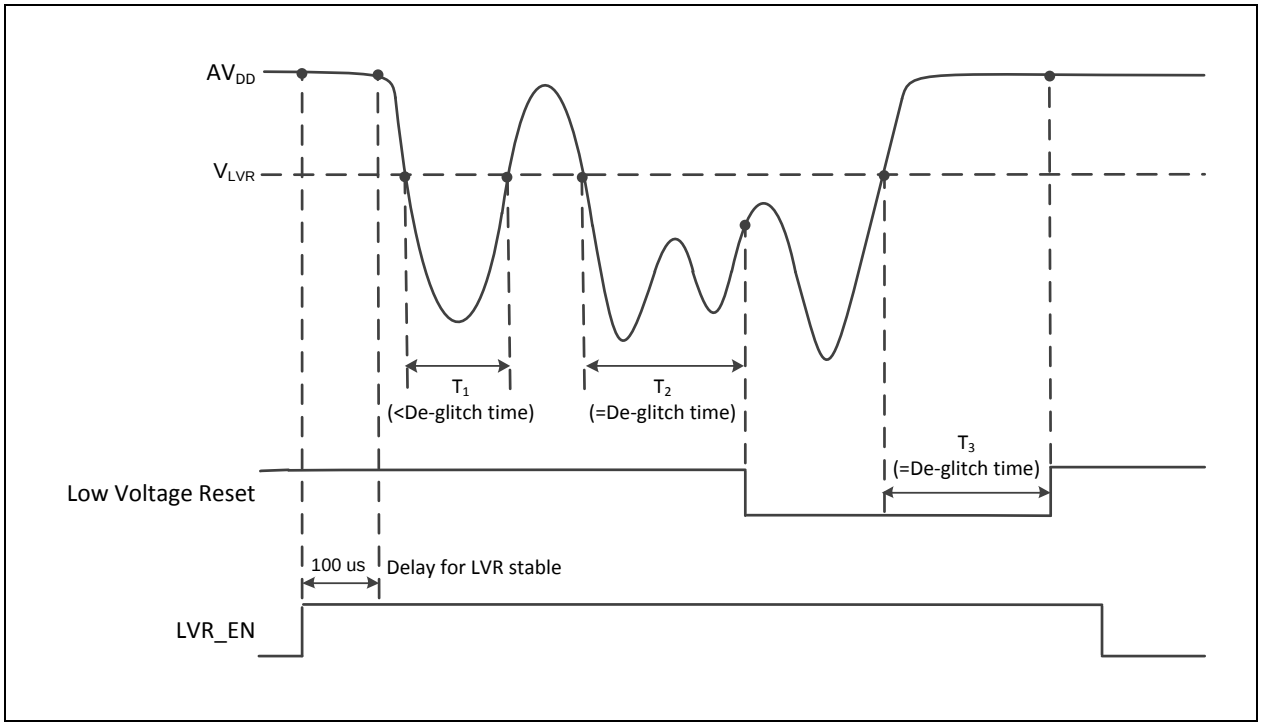


Figure 6-5 Low Voltage Reset Waveform

6.2.2.4 *Brown-out Detector Reset (BOD Reset)*

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BOD_EN (BODCR[0]), Brown-Out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BOD_EN (BODCR[0]) and BOD_VL (BODCR[2:1]) and the state keeps longer than De-glitch time (Max(20*HCLK cycles, 1*LIRC cycle)), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time. The default value of BOD_EN, BOD_VL and BOD_RSTEN is set by flash controller user configuration register CBODEN (CONFIG0[23]), CBOV1-0 (CONFIG0[22:21]) and CBORST (CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6-6 shows the Brown-Out Detector waveform.

6.2.3 Power modes and Wake-up sources

There are several wake-up sources in Idle mode and Power-down mode. Table 6-2 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	WDT, I²C, Timer, UART, BOD and GPIO
Available Clocks	All	All except CPU clock	LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6-2 Power Mode Difference Table

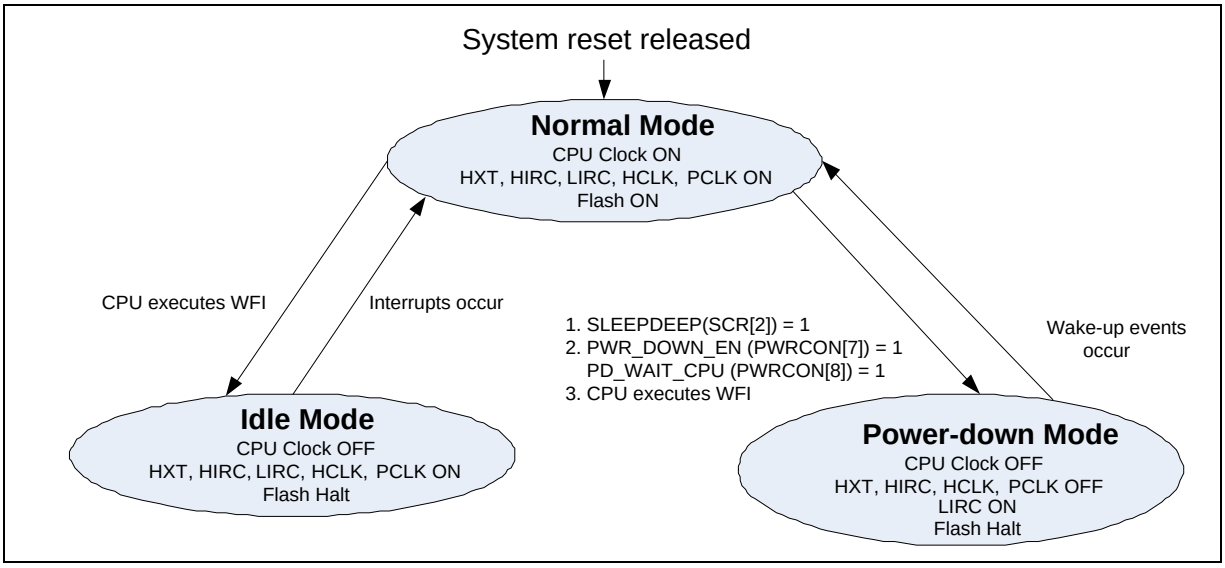


Figure 6-7 Power Mode State Machine

6.2.5 System Memory Map

The NuMicro® NUC123 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the Table 6-5. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripherals. The NuMicro® NUC123 Series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_FFFF	FLASH_BA	FLASH Memory Space (64KB)
0x2000_0000 – 0x2000_4FFF	SRAM_BA	SRAM Memory Space (20KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog/Window Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4010_0000 – 0x4010_3FFF	PS2_BA	PS/2 Interface Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4013_0000 – 0x4013_3FFF	SPI2_BA	SPI2 with master/slave function Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x401A_0000 – 0x401A_3FFF	I2S_BA	I^2S Interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers

6.2.7.2 Vector Table

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6-8 Vector Table Format

6.2.7.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending; however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In the Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal oscillator and 22.1184 MHz internal high speed RC oscillator to reduce the overall system power consumption. The Figure 6-9 and Figure 6-10 show the clock generator and the overview of the clock source control.

The clock generator consists of 4 clock sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency(PLL FOUT), PLL source can be from 4~24 MHz external high speed crystal oscillator (HXT) or 22.1184 MHz internal high speed RC oscillator (HIRC))
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter start counting and correlated clock stable index (OSC22M_STB(CLKSTATUS[4]), OSC10K_STB(CLKSTATUS[3]), PLL_STB(CLKSTATUS[2]) and XTL12M_STB(CLKSTATUS[0])) are set to 1 after stable counter value reach a define value asshown in Table 6-9. System and peripheral can use the clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index will auto clear when user disables the clock source (OSC10K_EN(PWRCON[3]), OSC22M_EN(PWRCON[2]), XTL12M_EN(PWRCON[0]) and PD(PLLCON[16])). Besides, the clock stable index of HXT, HIRC and PLL will auto clear when chip enter power-down and clock stable counter will re-counting after chip wake-up if correlate clock is enabled.

Clock Source	Clock Stable Count Value
HXT	4096 HXT clock
PLL	6144 PLL source (PLL source is HXT if PLL_SRC(PLLCON[19]) = 0, or HIRC if PLL_SRC(PLLCON[19]) = 1)
HIRC	256 HIRC clock
LIRC	1 LIRC

Table 6-9 Clock Stable Count Value Table

6.14 Serial Peripheral Interface (SPI)

6.14.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. This NuMicro® NUC123 series contains up to three sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be configured as a Master or a Slave device.

This controller supports variable serial clock function for special application and it also supports 2-bit Transfer mode. The controller also supports PDMA function to access the data buffer and also supports Dual I/O transfer mode.

6.14.2 Features

- Up to three sets of SPI controllers
- Supports Master or Slave mode operation
- Supports 2-bit Transfer mode
- Supports Dual I/O transfer mode
- Configurable bit length of a transfer word from 8 to 32-bit
- Provide separate 8-layer depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Up to two slave select lines in Master mode
- Supports Byte Reorder function
- Supports configurable suspend interval in Master mode
- Variable output serial clock frequency in Master mode
- Supports PDMA transfer
- Supports 3-Wire, no slave select signal, bi-direction interface

6.15 I^{2}S Controller (I^{2}S)

6.15.1 Overview

The I^{2}S controller consists of IIS protocol to interface with external audio CODEC. Two 8 word depth FIFO buffers for read path and write path respectively and is capable of handling 8/16/24/32 bits word sizes. PDMA controller handles the data movement between FIFO and memory.

6.15.2 Features

- Operated as either Master or Slave
- Capable of handling 8, 16, 24 and 32 bits word
- Supports monaural and stereo audio data
- Supports four data format:
  - I^{2}S data format
  - MSB justified data format
  - PCM mode A
  - PCM mode B
- Provides two 8 word depth FIFO buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports PDMA transfer

7.4.2 LDO and Power Management Specifications

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.5	5	5.5	V	V_{DD} input voltage
Output Voltage	1.62	1.8	1.98	V	V_{DD} > 2.5V
Temperature	-40	25	85	℃	
Cbp	-	1	-	uF	Resr = 1Ω

Notes:

1. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between V_{DD} and the closest V_{SS} pin of the device.

2. To ensure power stability, a 1uF (Cbp) or higher capacitor must be connected between LDO pin and the closest VSS pin of the device.

7.4.3 Low Voltage Reset Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	V_{DD} = 5.5 V	-	-	5	uA
Temperature	-	-40	25	85	℃
Threshold voltage	Temperature = 25℃	1.7	2.0	2.3	V
	Temperature = -40℃	-	2.4	-	V
	Temperature = 85℃	-	1.6	-	V
Hysteresis	-	0	0	0	V

C_{bp}	External Bypass Capacitor			1.0	-	uF

7.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage		1.62	1.8	1.98	V[1]
T_{RET}	Data Retention	Temp=85 ℃	10			year
T_{ERASE}	Page Erase Time			20		ms
T_{MER}	Mass Erase Time			40		ms
T_{PROG}	Program Time			40		us
I_{DD1}	Read Current				0.25	mA
I_{DD2}	Program/Erase Current				7	mA
I_{PD}	Power Down Current			1	20	uA

Note: V_{DD} is source from chip LDO output voltage.

8.4.4 Brown-out Detector Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV_{DD} = 5.5 V	-	-	125	μA
Temperature	-	-40	25	105	℃
Brown-out voltage	BOV_VL[1:0] = 11	4.2	4.4	4.6	V
	BOV_VL [1:0] = 10	3.5	3.7	3.9	V
	BOV_VL [1:0] = 01	2.6	2.7	2.8	V
	BOV_VL [1:0] = 00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

8.4.5 Power-On Reset (5V) Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Temperature	-	-40	25	105	℃
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

8.4.6 USB PHY Specifications

8.4.6.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high (driven)		2.0			V
V_{IL}	Input low				0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V_{OL}	Output low (driven)		0		0.3	V
V_{OH}	Output high (driven)		2.8		3.6	V
V_{CRS}	Output signal cross voltage		1.3		2.0	V
R_{PU}	Pull-up resistor		1.425		1.575	kΩ
R_{PD}	Pull-down resistor		14.25		15.75	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z_{DRV}	Driver output resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver capacitance	Pin to GND			20	pF

Note: Driver output resistance doesn't include series resistor resistance.

8.4.6.2 USB Full-Speed Driver Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{FR}	Rising time	C_L = 50p	4		20	ns
T_{FF}	Falling time	C_L = 50p	4		20	ns
T_{FRFF}	Rising and falling time matching	$T_{FRFF} = T_{FR}/T_{FF}$	90		111.11	%

8.4.6.3 USB Power Dissipation

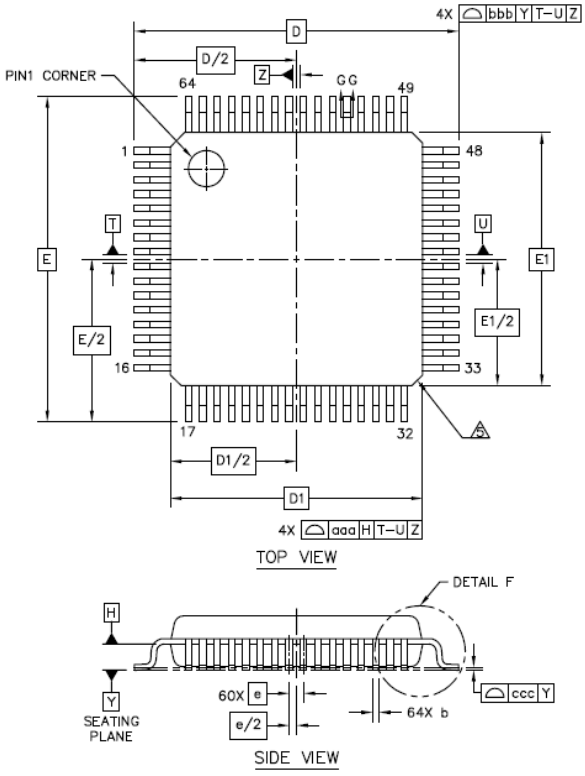
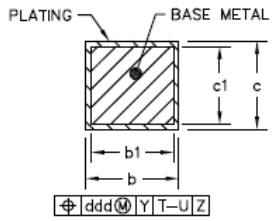
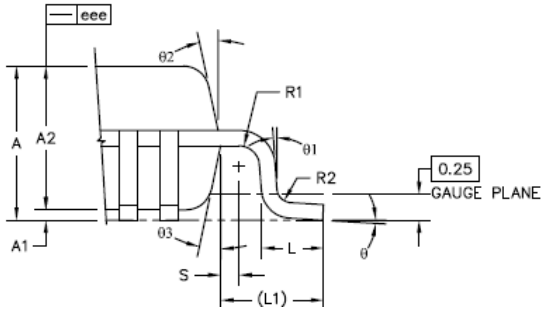
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{VBUS}	VBUS current (steady state)	Standby		50		uA

8.4.6.4 USB LDO Specification

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{BUS}	VBUS Pin Input Voltage		4.0	5.0	5.5	V
V_{DD33}	LDO Output Voltage		3.0	3.3	3.6	V

9 PACKAGE DIMENSIONS

9.1 64L LQFP (7x7x1.4 mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05