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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 11 |
| Program Memory Size | 14KB (8K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 14-SOIC (0.154", 3.90mm Width) |
| Supplier Device Package | 14-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16f1825t-i-sl |

### Peripheral Highlights (Continued)

- Data Signal Modulator Module:
  - Selectable modulator and carrier sources
- SR Latch:
  - Multiple Set/Reset input options
  - Emulates 555 Timer applications

### PIC12(L)F1822/1840/PIC16(L)F182x/1847 Family Types

| Device | Data Sheet Index | Program Memory Flash (words) | Data EEPROM (bytes) | Data SRAM (bytes) | I/O's(2) | 10-bit ADC (ch) | CapSense (ch) | Comparators | Timers (8/16-bit) | EUSART | MSSP ($I^2C$™/SPI) | ECCP (Full-Bridge) ECCP (Half-Bridge) CCP | SR Latch | Debug(1) | XLP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PIC12(L)F1822 | (1) | 2K | 256 | 128 | 6 | 4 | 4 | 1 | 2/1 | 1 | 1 | 0/1/0 | Y | I/H | Y |
| PIC12(L)F1840 | (2) | 4K | 256 | 256 | 6 | 4 | 4 | 1 | 2/1 | 1 | 1 | 0/1/0 | Y | I/H | Y |
| PIC16(L)F1823 | (1) | 2K | 256 | 128 | 12 | 8 | 8 | 2 | 2/1 | 1 | 1 | 1/0/0 | Y | I/H | Y |
| PIC16(L)F1824 | (3) | 4K | 256 | 256 | 12 | 8 | 8 | 2 | 4/1 | 1 | 1 | 1/1/2 | Y | I/H | Y |
| PIC16(L)F1825 | (4) | 8K | 256 | 1024 | 12 | 8 | 8 | 2 | 4/1 | 1 | 1 | 1/1/2 | Y | I/H | Y |
| PIC16(L)F1826 | (5) | 2K | 256 | 256 | 16 | 12 | 12 | 2 | 2/1 | 1 | 1 | 1/0/0 | Y | I/H | Y |
| PIC16(L)F1827 | (5) | 4K | 256 | 384 | 16 | 12 | 12 | 2 | 4/1 | 1 | 2 | 1/1/2 | Y | I/H | Y |
| PIC16(L)F1828 | (3) | 4K | 256 | 256 | 18 | 12 | 12 | 2 | 4/1 | 1 | 1 | 1/1/2 | Y | I/H | Y |
| PIC16(L)F1829 | (4) | 8K | 256 | 1024 | 18 | 12 | 12 | 2 | 4/1 | 1 | 2 | 1/1/2 | Y | I/H | Y |
| PIC16(L)F1847 | (6) | 8K | 256 | 1024 | 16 | 12 | 12 | 2 | 4/1 | 1 | 2 | 1/1/2 | Y | I/H | Y |

**Note 1:** I - Debugging, Integrated on Chip; H - Debugging, available using Debug Header.

**2:** One pin is input-only.

**Data Sheet Index:** (Unshaded devices are described in this document.)

**1:** DS41413 PIC12(L)F1822/PIC16(L)F1823 Data Sheet, 8/14-Pin Flash Microcontrollers.

**2:** DS41441 PIC12(L)F1840 Data Sheet, 8-Pin Flash Microcontrollers.

**3:** DS41419 PIC16(L)F1824/1828 Data Sheet, 28/40/44-Pin Flash Microcontrollers.

**4:** DS41440 PIC16(L)F1825/1829 Data Sheet, 14/20-Pin Flash Microcontrollers.

**5:** DS41391 PIC16(L)F1826/1827 Data Sheet, 18/20/28-Pin Flash Microcontrollers.

**6:** DS41453 PIC16(L)F1847 Data Sheet, 18/20/28-Pin Flash Microcontrollers.

**Note:** For other small form-factor package availability and marking information, please visit www.microchip.com/packaging or contact your local sales office.

**FIGURE 1: 14-PIN DIAGRAM FOR PIC16(L)F1825**

**PDIP, SOIC, TSSOP**

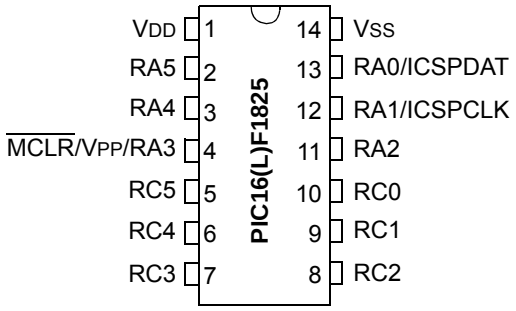
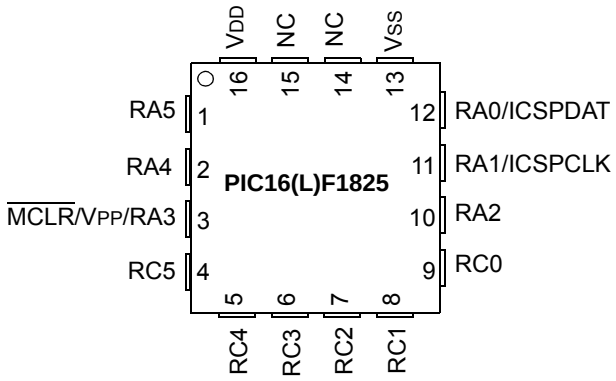



**FIGURE 2: 16-PIN DIAGRAM FOR PIC16(L)F1825**

**QFN, UQFN**



## 2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative Addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

### 2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 8.5 "Automatic Context Saving"**, for more information.

### 2.2 16-level Stack with Overflow and Underflow

These devices have an external stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled will cause a software Reset. See section **Section 3.4 "Stack"** for more details.

### 2.3 File Select Registers

There are two 16-bit File Select Registers (FSR). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSR points to program memory, there is one additional instruction cycle in instructions using INDF to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.5 "Indirect Addressing"** for more details.

### 2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 29.0 "Instruction Set Summary"** for more details.

**TABLE 3-3: PIC16(L)F1825/9 MEMORY MAP, BANKS 0-7**

| | BANK 0 | | BANK 1 | | BANK 2 | | BANK 3 | | BANK 4 | | BANK 5 | | BANK 6 | | BANK 7 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000h | INDF0 | 080h | INDF0 | 100h | INDF0 | 180h | INDF0 | 200h | INDF0 | 280h | INDF0 | 300h | INDF0 | 380h | INDF0 |
| 001h | INDF1 | 081h | INDF1 | 101h | INDF1 | 181h | INDF1 | 201h | INDF1 | 281h | INDF1 | 301h | INDF1 | 381h | INDF1 |
| 002h | PCL | 082h | PCL | 102h | PCL | 182h | PCL | 202h | PCL | 282h | PCL | 302h | PCL | 382h | PCL |
| 003h | STATUS | 083h | STATUS | 103h | STATUS | 183h | STATUS | 203h | STATUS | 283h | STATUS | 303h | STATUS | 383h | STATUS |
| 004h | FSR0L | 084h | FSR0L | 104h | FSR0L | 184h | FSR0L | 204h | FSR0L | 284h | FSR0L | 304h | FSR0L | 384h | FSR0L |
| 005h | FSR0H | 085h | FSR0H | 105h | FSR0H | 185h | FSR0H | 205h | FSR0H | 285h | FSR0H | 305h | FSR0H | 385h | FSR0H |
| 006h | FSR1L | 086h | FSR1L | 106h | FSR1L | 186h | FSR1L | 206h | FSR1L | 286h | FSR1L | 306h | FSR1L | 386h | FSR1L |
| 007h | FSR1H | 087h | FSR1H | 107h | FSR1H | 187h | FSR1H | 207h | FSR1H | 287h | FSR1H | 307h | FSR1H | 387h | FSR1H |
| 008h | BSR | 088h | BSR | 108h | BSR | 188h | BSR | 208h | BSR | 288h | BSR | 308h | BSR | 388h | BSR |
| 009h | WREG | 089h | WREG | 109h | WREG | 189h | WREG | 209h | WREG | 289h | WREG | 309h | WREG | 389h | WREG |
| 00Ah | PCLATH | 08Ah | PCLATH | 10Ah | PCLATH | 18Ah | PCLATH | 20Ah | PCLATH | 28Ah | PCLATH | 30Ah | PCLATH | 38Ah | PCLATH |
| 00Bh | INTCON | 08Bh | INTCON | 10Bh | INTCON | 18Bh | INTCON | 20Bh | INTCON | 28Bh | INTCON | 30Bh | INTCON | 38Bh | INTCON |
| 00Ch | PORTA | 08Ch | TRISA | 10Ch | LATA | 18Ch | ANSELA | 20Ch | WPUA | 28Ch | — | 30Ch | — | 38Ch | INLVLA |
| 00Dh | PORTB(1) | 08Dh | TRISB(1) | 10Dh | LATB(1) | 18Dh | ANSELB(1) | 20Dh | WPUB(1) | 28Dh | — | 30Dh | — | 38Dh | INLVLB(1) |
| 00Eh | PORTC | 08Eh | TRISC | 10Eh | LATC | 18Eh | ANSELC | 20Eh | WPUC | 28Eh | — | 30Eh | — | 38Eh | INLVLC |
| 00Fh | — | 08Fh | — | 10Fh | — | 18Fh | — | 20Fh | — | 28Fh | — | 30Fh | — | 38Fh | — |
| 010h | — | 090h | — | 110h | — | 190h | — | 210h | — | 290h | — | 310h | — | 390h | — |
| 011h | PIR1 | 091h | PIE1 | 111h | CM1CON0 | 191h | EEADRL | 211h | SSP1BUF | 291h | CCPR1L | 311h | CCPR3L | 391h | IOCAP |
| 012h | PIR2 | 092h | PIE2 | 112h | CM1CON1 | 192h | EEADRH | 212h | SSP1ADD | 292h | CCPR1H | 312h | CCPR3H | 392h | IOCAN |
| 013h | PIR3 | 093h | PIE3 | 113h | CM2CON0 | 193h | EEDATL | 213h | SSP1MSK | 293h | CCP1CON | 313h | CCP3CON | 393h | IOCAF |
| 014h | PIR4(1) | 094h | PIE4(1) | 114h | CM2CON1 | 194h | EEDATH | 214h | SSP1STAT | 294h | PWM1CON | 314h | — | 394h | IOCBP(1) |
| 015h | TMR0 | 095h | OPTION_REG | 115h | CMOUT | 195h | EECON1 | 215h | SSP1CON1 | 295h | CCP1AS | 315h | — | 395h | IOCBN(1) |
| 016h | TMR1L | 096h | PCON | 116h | BORCON | 196h | EECON2 | 216h | SSP1CON2 | 296h | PSTR1CON | 316h | — | 396h | IOCBF(1) |
| 017h | TMR1H | 097h | WDTCON | 117h | FVRCON | 197h | — | 217h | SSP1CON3 | 297h | — | 317h | — | 397h | — |
| 018h | T1CON | 098h | OSCTUNE | 118h | DACCON0 | 198h | — | 218h | — | 298h | CCPR2L | 318h | CCPR4L | 398h | — |
| 019h | T1GCON | 099h | OSCCON | 119h | DACCON1 | 199h | RCREG | 219h | SSP2BUF(1) | 299h | CCPR2H | 319h | CCPR4H | 399h | — |
| 01Ah | TMR2 | 09Ah | OSCSTAT | 11Ah | SRCON0 | 19Ah | TXREG | 21Ah | SSP2ADD(1) | 29Ah | CCP2CON | 31Ah | CCP4CON | 39Ah | CLKRCON |
| 01Bh | PR2 | 09Bh | ADRESL | 11Bh | SRCON1 | 19Bh | SPBRGL | 21Bh | SSP2MSK(1) | 29Bh | PWM2CON | 31Bh | — | 39Bh | — |
| 01Ch | T2CON | 09Ch | ADRESH | 11Ch | — | 19Ch | SPBRGH | 21Ch | SSP2STAT(1) | 29Ch | CCP2AS | 31Ch | — | 39Ch | MDCON |
| 01Dh | — | 09Dh | ADCON0 | 11Dh | APFCON0 | 19Dh | RCSTA | 21Dh | SSP2CON1(1) | 29Dh | PSTR2CON | 31Dh | — | 39Dh | MDSRC |
| 01Eh | CPSCON0 | 09Eh | ADCON1 | 11Eh | APFCON1 | 19Eh | TXSTA | 21Eh | SSP2CON2(1) | 29Eh | CCPTMRS | 31Eh | — | 39Eh | MDCARL |
| 01Fh | CPSCON1 | 09Fh | — | 11Fh | — | 19Fh | BAUDCON | 21Fh | SSP2CON3(1) | 29Fh | — | 31Fh | — | 39Fh | MDCARH |
| 020h | General Purpose Register 96 Bytes | 0A0h | General Purpose Register 80 Bytes | 120h | General Purpose Register 80 Bytes | 1A0h | General Purpose Register 80 Bytes | 220h | General Purpose Register 80 Bytes | 2A0h | General Purpose Register 80 Bytes | 320h | General Purpose Register 80 Bytes | 3A0h | General Purpose Register 80 Bytes |
| 06Fh | | 0EFh | | 16Fh | | 1EFh | | 26Fh | | 2EFh | | 36Fh | | 3EFh | |
| 070h | Common RAM | 0F0h | Accesses 70h – 7Fh | 170h | Accesses 70h – 7Fh | 1F0h | Accesses 70h – 7Fh | 270h | Accesses 70h – 7Fh | 2F0h | Accesses 70h – 7Fh | 370h | Accesses 70h – 7Fh | 3F0h | Accesses 70h – 7Fh |
| 07Fh | | 0FFh | | 17Fh | | 1FFh | | 27Fh | | 2FFh | | 37Fh | | 3FFh | |

**Legend:** = Unimplemented data memory locations, read as '0'

**Note 1:** Available only on PIC16(L)F1829.

**TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH REFERENCE CLOCK SOURCES**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| CLKRCON | CLKREN | CLKROE | CLKRSLR | CLKRDC<1:0> | | CLKRDIV<2:0> | | | 72 |

**Legend:** — Unimplemented locations read as '0'. Shaded cells are not used by reference clock sources.

**TABLE 6-2: SUMMARY OF CONFIGURATION WORD WITH REFERENCE CLOCK SOURCES**

| Name | Bits | Bit -/7 | Bit -/6 | Bit 13/5 | Bit 12/4 | Bit 11/3 | Bit 10/2 | Bit 9/1 | Bit 8/0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|---|
| CONFIG1 | 13:8 | — | — | FCMEN | IESO | $\overline{\text{CLKOUTEN}}$ | BOREN<1:0> | | $\overline{\text{CPD}}$ | 48 |
| | 7:0 | $\overline{\text{CP}}$ | MCLRE | $\overline{\text{PWRTE}}$ | WDTE<1:0> | | FOSC<2:0> | | | |

**Legend:** — Unimplemented locations read as '0'. Shaded cells are not used by reference clock sources.

**TABLE 10-3: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| OSCCON | SPLLEN | IRCF<3:0> | | | | — | SCS<1:0> | | 68 |
| STATUS | — | — | — | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 22 |
| WDTCON | — | — | WDTPS<4:0> | | | | | SWDTEN | 100 |

**Legend:** x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by Watchdog Timer.

**TABLE 10-4: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER**

| Name | Bits | Bit -/7 | Bit -/6 | Bit 13/5 | Bit 12/4 | Bit 11/3 | Bit 10/2 | Bit 9/1 | Bit 8/0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|---|
| CONFIG1 | 13:8 | — | — | FCMEN | IESO | $\overline{CLKOUTEN}$ | BOREN<1:0> | | $\overline{CPD}$ | 48 |
| | 7:0 | $\overline{CP}$ | MCLRE | $\overline{PWRTE}$ | WDTE<1:0> | | FOSC<2:0> | | | |

**Legend:** — Unimplemented location, read as '0'. Shaded cells are not used by Watchdog Timer.

### REGISTER 12-12: ANSELB: PORTB ANALOG SELECT REGISTER

| U-0 | U-0 | R/W-1/1 | R/W-1/1 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | ANSB5 | ANSB4 | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **ANSB<5:4>**: Analog Select between Analog or Digital Function on pins RB<5:4>, respectively
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.

bit 3-0 **Unimplemented:** Read as ‘0’

**Note 1:** When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

### REGISTER 12-13: WPUB: WEAK PULL-UP PORTB REGISTER

| R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| WPUB7 | WPUB6 | WPUB5 | WPUB4 | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-4 **WPUB<7:4>**: Weak Pull-up Register bits(1,2)
1 = Pull-up enabled
0 = Pull-up disabled

bit 3-0 **Unimplemented:** Read as ‘0’

**Note 1:** Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
**2:** The weak pull-up device is automatically disabled if the pin is in configured as an output.

### REGISTER 12-14: INLVLB: PORTB INPUT LEVEL CONTROL REGISTER

| R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| INLVLB7 | INLVLB6 | INLVLB5 | INLVLB4 | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-4 **INLVLB<7:4>:** PORTB Input Level Select bits
For RB<7:4> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

bit 7-6 **Unimplemented:** Read as ‘0’

**REGISTER 12-18: ANSELC: PORTC ANALOG SELECT REGISTER**

| R/W-1/1 | R/W-1/1 | U-0 | U-0 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| ANSC7(2) | ANSC6(2) | — | — | ANSC3 | ANSC2 | ANSC1 | ANSC0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-6 **ANSC<7:6>**: Analog Select between Analog or Digital Function on pins RC<7:6>, respectively(2)
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **ANSC<3:0>**: Analog Select between Analog or Digital Function on pins RC<3:0>, respectively
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.

**Note 1:** When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.
**2:** ANSELC<7:6> available on PIC16(L)F1829 only. Otherwise, they are unimplemented and read as '0'.

**REGISTER 12-19: WPUC: WEAK PULL-UP PORTC REGISTER**

| R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| WPUC7(3) | WPUC6(3) | WPUC5 | WPUC4 | WPUC3 | WPUC2 | WPUC1 | WPUC0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-0 **WPUC<7:0>**: Weak Pull-up Register bits(1, 2)
1 = Pull-up enabled
0 = Pull-up disabled

**Note 1:** Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
**2:** The weak pull-up device is automatically disabled if the pin is in configured as an output.
**3:** WPUC<7:6> available on PIC16(L)F1829 only. Otherwise, they are unimplemented and read as '0'.

**TABLE 16-3: SUMMARY OF REGISTERS ASSOCIATED WITH ADC**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| ADCON0 | — | CHS<4:0> | | | | | GO/$\overline{\text{DONE}}$ | ADON | 150 |
| ADCON1 | ADFM | ADCS<2:0> | | | — | ADNREF | ADPREF<1:0 | | 151 |
| ADRESH | A/D Result Register High | | | | | | | | 152, 153 |
| ADRESL | A/D Result Register Low | | | | | | | | 152, 153 |
| ANSELA | — | — | — | ANSA4 | — | ANSA2 | ANSA1 | ANSA0 | 123 |
| ANSELB(1) | — | — | ANSB5 | ANSB4 | — | — | — | — | 129 |
| ANSELC | ANSC7(1) | ANSC6(1) | — | — | ANSC3 | ANSC2 | ANSC1 | ANSC0 | 134 |
| CCP4CON | P4M<1:0> | | DC4B<1:0> | | CCP4M<3:0> | | | | 224 |
| INLVLA | — | — | INLVLA5 | INLVLA4 | INLVLA3 | INLVLA2 | INLVLA1 | INLVLA0 | 124 |
| INLVLB(1) | INLVLB7 | INLVLB6 | INLVLB5 | INLVLB4 | — | — | — | — | 129 |
| INLVLC | INLVLC7(1) | INLVLC6(1) | INLVLC5 | INLVLC4 | INLVLC3 | INLVLC2 | INLVLC1 | INLVLC0 | 135 |
| INTCON | GIE | PEIE | TMR0IE | INTE | IOCIE | TMR0IF | INTF | IOCIF | 87 |
| PIE1 | TMR1GIE | ADIE | RCIE | TXIE | SSP1IE | CCP1IE | TMR2IE | TMR1IE | 88 |
| PIR1 | TMR1GIF | ADIF | RCIF | TXIF | SSP1IF | CCP1IF | TMR2IF | TMR1IF | 92 |
| TRISA | — | — | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | 122 |
| TRISB(1) | TRISB7 | TRISB6 | TRISB5 | TRISB4 | — | — | — | — | 128 |
| TRISC | TRISC7(1) | TRISC6(1) | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 | 133 |
| FVRCON | FVREN | FVRRDY | TSEN | TSRNG | CDAFVR<1:0> | | ADFVR<1:0> | | 142 |
| DACCON0 | DACEN | DACLPS | DACOE | — | DACPSS<1:0> | | — | DACNSS | 160 |
| DACCON1 | — | — | — | DACR<4:0> | | | | | 160 |

**Legend:** x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends on condition. Shaded cells are not used for ADC module.

**Note 1:** PIC16(L)F1829 only.

## 19.2 Comparator Control

Each comparator has two control registers: CMxCON0 and CMxCON1.

The CMxCON0 registers (see Register 19-1) contain Control and Status bits for the following:

- Enable
- Output selection
- Output polarity
- Speed/Power selection
- Hysteresis enable
- Output synchronization

The CMxCON1 registers (see Register 19-2) contain Control bits for the following:

- Interrupt enable
- Interrupt edge polarity
- Positive input channel selection
- Negative input channel selection

### 19.2.1 COMPARATOR ENABLE

Setting the CxON bit of the CMxCON0 register enables the comparator for operation. Clearing the CxON bit disables the comparator resulting in minimum current consumption.

### 19.2.2 COMPARATOR OUTPUT SELECTION

The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the MCxOUT bit of the CMOUT register. In order to make the output available for an external connection, the following conditions must be true:

- CxOE bit of the CMxCON0 register must be set
- Corresponding TRIS bit must be cleared
- CxON bit of the CMxCON0 register must be set

| | |
|---|---|
| **Note 1:** | The CxOE bit of the CMxCON0 register overrides the PORT data latch. Setting the CxON bit of the CMxCON0 register has no impact on the port override. |
| **2:** | The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched. |

### 19.2.3 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

Table 19-1 shows the output state versus input conditions, including polarity control.

**TABLE 19-1: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS**

| Input Condition | CxPOL | CxOUT |
|---|---|---|
| CxVN > CxVP | 0 | 0 |
| CxVN < CxVP | 0 | 1 |
| CxVN > CxVP | 1 | 1 |
| CxVN < CxVP | 1 | 0 |

### 19.2.4 COMPARATOR SPEED/POWER SELECTION

The trade-off between speed or power can be optimized during program execution with the CxSP control bit. The default state for this bit is '1' which selects the Normal Speed mode. Device power consumption can be optimized at the cost of slower comparator propagation delay by clearing the CxSP bit to '0'.

## 19.3 Comparator Hysteresis

A selectable amount of separation voltage can be added to the input pins of each comparator to provide a hysteresis function to the overall operation. Hysteresis is enabled by setting the CxHYS bit of the CMxCON0 register.

See **Section 30.0 "Electrical Specifications"** for more information.

## 19.9 Interaction with ECCP Logic

In some devices, a comparator output signal can be used to trigger the auto-shutdown feature found within the ECCP module. When the ECCP auto-shutdown feature is enabled and a comparator output signal is selected as the source, the comparator can be used simultaneously as a general purpose comparator and as the ECCP auto-shutdown source. In addition, the comparator output signal can also be routed to the designated I/O pin. If the ECCP Auto-Restart mode is also enabled, the comparators can be used as a closed loop analog feedback circuit to the ECCP, thereby creating an analog controlled PWM.

Please see section

for more information.

| | |
|---|---|
| **Note:** | When the comparator module is first initialized the output state is unknown. Upon initialization, the user should verify the output state of the comparator prior to relying on the result, primarily when using the result in connection with other peripheral features, such as the ECCP Auto-Shutdown mode. |

## 19.10 Analog Input Connection Considerations

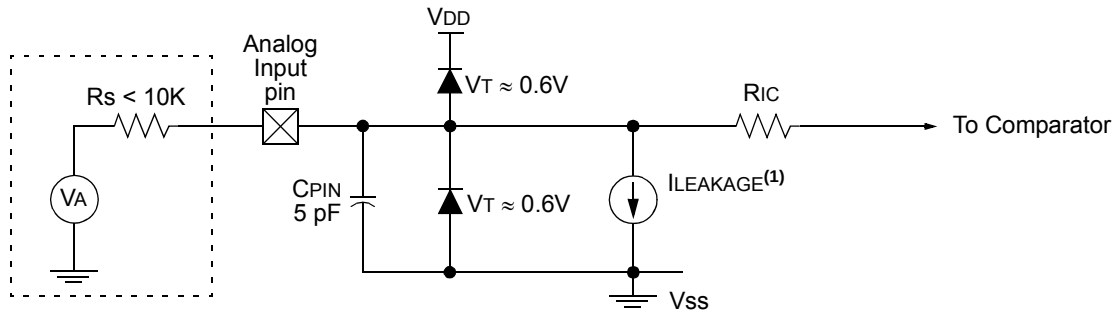
A simplified circuit for an analog input is shown in Figure 19-3. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to $V_{DD}$ and $V_{SS}$. The analog input, therefore, must be between $V_{SS}$ and $V_{DD}$.

If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of 10 kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

| | |
|---|---|
| **Note 1:** | When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification. |
| **2:** | Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified. |

**FIGURE 19-3: ANALOG INPUT MODEL**




**Legend:** $C_{PIN}$ = Input Capacitance
$I_{LEAKAGE}$ = Leakage Current at the pin due to various junctions
$R_{IC}$ = Interconnect Resistance
$R_S$ = Source Impedance
$V_A$ = Analog Voltage
$V_T$ = Threshold Voltage

**Note 1:** See **Section 30.0 "Electrical Specifications"**.

## 20.2 Option and Timer0 Control Register

**REGISTER 20-1: OPTION_REG: OPTION REGISTER**

| R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{WPUEN}}$ | INTEDG | TMR0CS | TMR0SE | PSA | PS<2:0> | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7 **$\overline{\text{WPUEN}}$:** Weak Pull-up Enable bit
1 = All weak pull-ups are disabled (except $\overline{\text{MCLR}}$, if it is enabled)
0 = Weak pull-ups are enabled by individual WPUx latch values

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

bit 5 **TMR0CS:** Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4 **TMR0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is not assigned to the Timer0 module
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

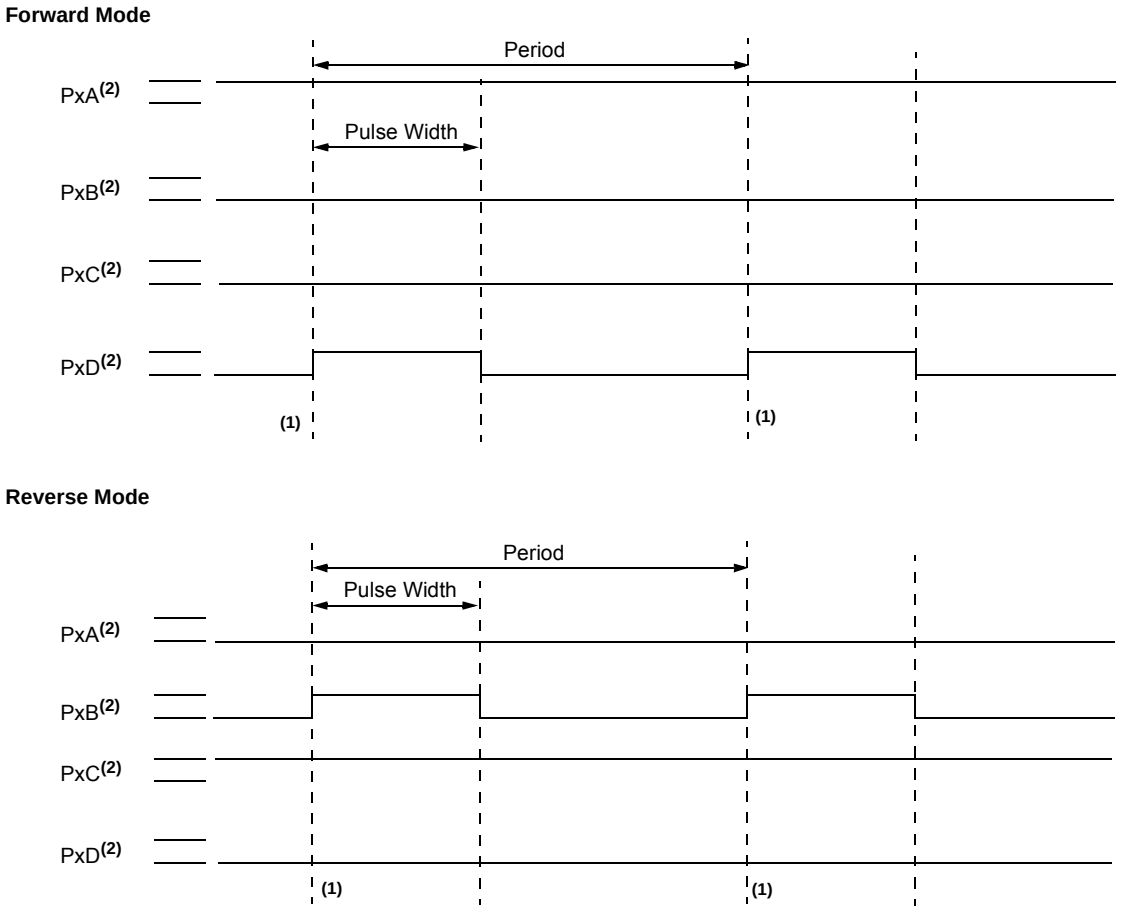
| Bit Value | Timer0 Rate |
|---|---|
| 000 | 1 : 2 |
| 001 | 1 : 4 |
| 010 | 1 : 8 |
| 011 | 1 : 16 |
| 100 | 1 : 32 |
| 101 | 1 : 64 |
| 110 | 1 : 128 |
| 111 | 1 : 256 |

**TABLE 20-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| CPSCON0 | CPSON | CPSRM | — | — | CPSRNG<1:0> | | CPSOUT | T0xCS | 315 |
| FVRCON | FVREN | FVRRDY | TSEN | TSRNG | CDAFVR<1:0> | | ADFVR<1:0> | | 142 |
| INLVLA | — | — | INLVLA5 | INLVLA4 | INLVLA3 | INLVLA2 | INLVLA1 | INLVLA0 | 124 |
| INTCON | GIE | PEIE | TMR0IE | INTE | IOCIE | TMR0IF | INTF | IOCIF | 87 |
| OPTION_REG | $\overline{\text{WPUEN}}$ | INTEDG | TMR0CS | TMR0SE | PSA | PS<2:0> | | | 176 |
| TMR0 | Timer0 Module Register | | | | | | | | 174* |
| TRISA | — | — | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | 122 |

**Legend:** — Unimplemented location, read as '0'. Shaded cells are not used by the Timer0 module.
* Page provides register information.

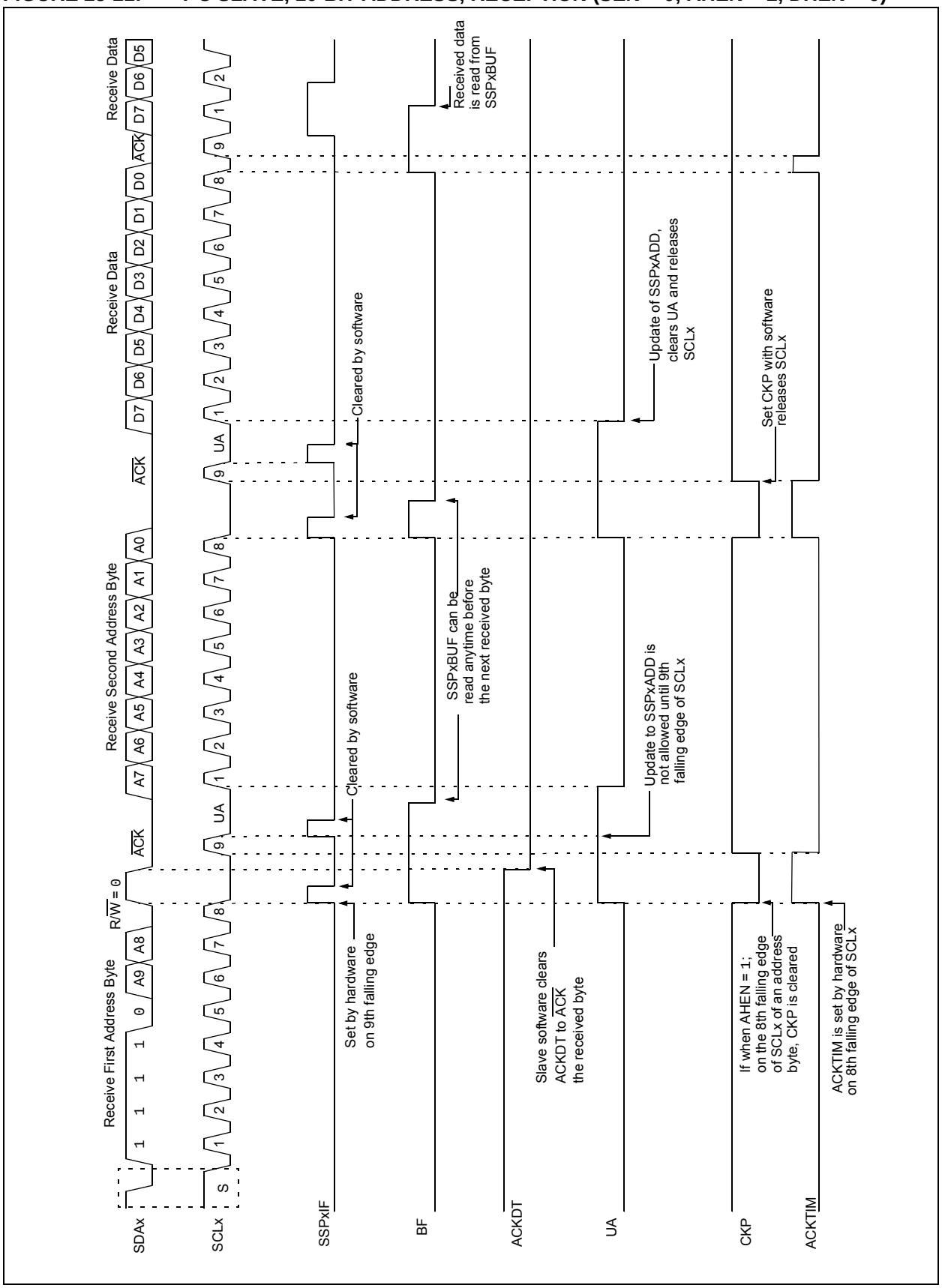
**FIGURE 24-11: EXAMPLE OF FULL-BRIDGE PWM OUTPUT**




**Note 1:** At this time, the TMRx register is equal to the PRx register.

**2:** Output signal is shown as active-high.

**FIGURE 25-21: I²C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 1, DHEN = 0)**



### 25.6.6 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address is accomplished by simply writing a value to the SSPxBUF register. This action will set the Buffer Full flag bit, BF and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDAx pin after the falling edge of SCLx is asserted. SCLx is held low for one Baud Rate Generator rollover count (TBRG). Data should be valid before SCLx is released high. When the SCLx pin is released high, it is held that way for TBRG. The data on the SDAx pin must remain stable for that duration and some hold time after the next falling edge of SCLx. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDAx. This allows the slave device being addressed to respond with an $\overline{ACK}$ bit during the ninth bit time if an address match occurred, or if data was received properly. The status of $\overline{ACK}$ is written into the ACKSTAT bit on the rising edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared. If not, the bit is set. After the ninth clock, the SSPxIF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSPxBUF, leaving SCLx low and SDAx unchanged (Figure 25-28).

After the write to the SSPxBUF, each bit of the address will be shifted out on the falling edge of SCLx until all seven address bits and the R/$\overline{W}$ bit are completed. On the falling edge of the eighth clock, the master will release the SDAx pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDAx pin to see if the address was recognized by a slave. The status of the $\overline{ACK}$ bit is loaded into the ACKSTAT Status bit of the SSPxCON2 register. Following the falling edge of the ninth clock transmission of the address, the SSPxIF is set, the BF flag is cleared and the Baud Rate Generator is turned off until another write to the SSPxBUF takes place, holding SCLx low and allowing SDAx to float.

#### 25.6.6.1 BF Status Flag

In Transmit mode, the BF bit of the SSPxSTAT register is set when the CPU writes to SSPxBUF and is cleared when all eight bits are shifted out.

#### 25.6.6.2 WCOL Status Flag

If the user writes the SSPxBUF when a transmit is already in progress (i.e., SSPxSR is still shifting out a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

WCOL must be cleared by software before the next transmission.

#### 25.6.6.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit of the SSPxCON2 register is cleared when the slave has sent an Acknowledge ($\overline{ACK}$ = 0) and is set when the slave does not Acknowledge ($\overline{ACK}$ = 1). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

#### 25.6.6.4 Typical Transmit Sequence:

1. The user generates a Start condition by setting the SEN bit of the SSPxCON2 register.
2. SSPxIF is set by hardware on completion of the Start.
3. SSPxIF is cleared by software.
4. The MSSPx module will wait the required start time before any other operation takes place.
5. The user loads the SSPxBUF with the slave address to transmit.
6. Address is shifted out the SDAx pin until all eight bits are transmitted. Transmission begins as soon as SSPxBUF is written to.
7. The MSSPx module shifts in the $\overline{ACK}$ bit from the slave device and writes its value into the ACKSTAT bit of the SSPxCON2 register.
8. The MSSPx module generates an interrupt at the end of the ninth clock cycle by setting the SSPxIF bit.
9. The user loads the SSPxBUF with eight bits of data.
10. Data is shifted out the SDAx pin until all eight bits are transmitted.
11. The MSSPx module shifts in the $\overline{ACK}$ bit from the slave device and writes its value into the ACKSTAT bit of the SSPxCON2 register.
12. Steps 8-11 are repeated for all transmitted data bytes.
13. The user generates a Stop or Restart condition by setting the PEN or RSEN bits of the SSPxCON2 register. Interrupt is generated once the Stop/Restart condition is complete.

## 26.5 EUSART Operation During Sleep

The EUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

### 26.5.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Reception (see **Section 26.4.2.4 "Synchronous Slave Reception Setup:"**).
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- The RCIF interrupt flag must be cleared by reading RCREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT and TX/CK pins, respectively. When the data word has been completely clocked in by the external device, the RCIF interrupt flag bit of the PIR1 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the GIE, Global Interrupt Enable, bit of the INTCON register is also set, then the Interrupt Service Routine at address 004h will be called.

### 26.5.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for synchronous slave transmission (see **Section 26.4.2.2 "Synchronous Slave Transmission Setup:"**).
- The TXIF interrupt flag must be cleared by writing the output data to the TXREG, thereby filling the TSR and transmit buffer.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the PEIE bit of the INTCON register.
- Interrupt enable bits TXIE of the PIE1 register and PEIE of the INTCON register must set.

Upon entering Sleep mode, the device will be ready to accept clocks on TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXREG will transfer to the TSR and the TXIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXREG is available to accept another character for transmission, which will clear the TXIF flag.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit is also set then the Interrupt Service Routine at address 0004h will be called.

### 26.5.3 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function registers, APFCON0 and APFCON1. To determine which pins can be moved and what their default locations are upon a Reset, see **Section 12.1 "Alternate Pin Function"** for more information.

## 30.1 DC Characteristics: PIC16(L)F1825/9-I/E (Industrial, Extended)

| PIC16LF1825/9 | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial<br>-40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **PIC16F1825/9** | | | **Standard Operating Conditions (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial<br>-40°C ≤ TA ≤ +125°C for extended | | | | |
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage (VDDMIN, VDDMAX)** | | | | | |
| | | PIC16LF1825/9 | 1.8<br>2.5 | —<br>— | 3.6<br>3.6 | V<br>V | FOSC ≤ 16 MHz:<br>FOSC ≤ 32 MHz (**Note 2**) |
| D001 | | PIC16F1825/9 | 1.8<br>2.5 | —<br>— | 5.5<br>5.5 | V<br>V | FOSC ≤ 16 MHz:<br>FOSC ≤ 32 MHz (**Note 2**) |
| D002* | VDR | **RAM Data Retention Voltage(1)** | | | | | |
| | | PIC16LF1825/9 | 1.5 | — | — | V | Device in Sleep mode |
| D002* | | PIC16F1825/9 | 1.7 | — | — | V | Device in Sleep mode |
| | VPOR* | **Power-on Reset Release Voltage** | — | 1.6 | — | V | |
| D002B* | VPORR* | **Power-on Reset Rearm Voltage** | | | | | |
| | | PIC16LF1825/9 | — | 0.8 | — | V | Device in Sleep mode |
| | | PIC16F1825/9 | — | 1.5 | — | V | Device in Sleep mode |
| D003 | VADFVR | **Fixed Voltage Reference Voltage for ADC** | -8 | — | 6 | % | 1.024V, VDD ≥ 2.5V<br>2.048V, VDD ≥ 2.5V<br>4.096V, VDD ≥ 4.75V |
| D003A | VCDAFVR | **Fixed Voltage Reference Voltage for Comparator and DAC** | -11 | — | 7 | % | 1.024V, VDD ≥ 2.5V<br>2.048V, VDD ≥ 2.5V<br>4.096V, VDD ≥ 4.75V |
| D003C* | TCVFVR | **Temperature Coefficient, Fixed Voltage Reference** | — | -130 | — | ppm/°C | |
| D003D* | ΔVFVR/ ΔVIN | **Line Regulation, Fixed Voltage Reference** | — | 0.270 | — | %/V | |
| D004* | SVDD | **VDD Rise Rate** to ensure internal Power-on Reset signal | 0.05 | — | — | V/ms | See **Section 7.1 "Power-on Reset (POR)"** for details. |

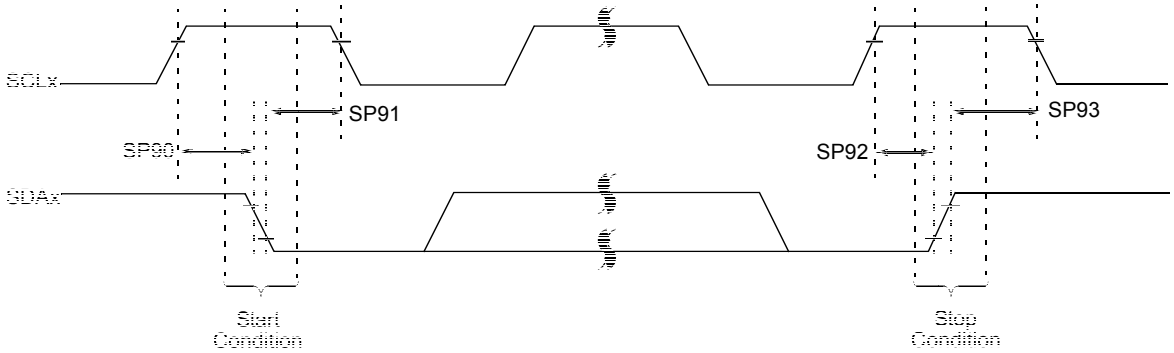
* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

**2:** PLL required for 32 MHz operation.

**FIGURE 30-20: I²C™ BUS START/STOP BITS TIMING**



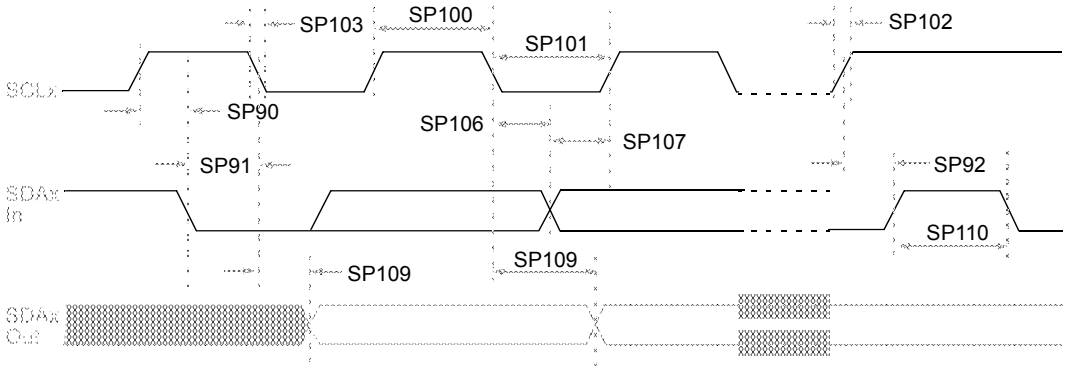

**Note**: Refer to Figure 30-5 for load conditions.

**TABLE 30-16: I²C™ BUS START/STOP BITS REQUIREMENTS**

| Param No. | Symbol | Characteristic | | Min. | Typ | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| SP90* | TSU:STA | Start condition | 100 kHz mode | 4700 | — | — | ns | Only relevant for Repeated Start condition |
| | | Setup time | 400 kHz mode | 600 | — | — | | |
| SP91* | THD:STA | Start condition | 100 kHz mode | 4000 | — | — | ns | After this period, the first clock pulse is generated |
| | | Hold time | 400 kHz mode | 600 | — | — | | |
| SP92* | TSU:STO | Stop condition | 100 kHz mode | 4700 | — | — | ns | |
| | | Setup time | 400 kHz mode | 600 | — | — | | |
| SP93 | THD:STO | Stop condition | 100 kHz mode | 4000 | — | — | ns | |
| | | Hold time | 400 kHz mode | 600 | — | — | | |

* These parameters are characterized but not tested.

**FIGURE 30-21: I²C™ BUS DATA TIMING**




**Note:** Refer to Figure 30-5 for load conditions.

## 31.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified $V_{DD}$ range). This is for **information only** and devices are ensured to operate properly only within the specified range.

| | |
|---|---|
| **Note:** | The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range. |

**"Typical" represents the mean of the distribution at 25°C. "MAXIMUM", "Max.", "MINIMUM" or "Min." represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.**

## 32.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

## 32.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®