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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT, IBT LIN/J2602
Number of I/O	12
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1829lin-e-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.0 DEVICE OVERVIEW

The PIC16(L)F1825/9 are described within this data sheet. They are available in 14/20 pin packages. Figure 1-1 shows a block diagram of the PIC16(L)F1825/9 devices. Tables 1-2 and 1-3 show the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1:DEVICE PERIPHERALSUMMARY

Peripheral		PIC16(L)F1825	PIC16(L)F1829
ADC		•	•
Capacitive Sensing (CP	S) Module	•	•
Data EEPROM		٠	•
Digital-to-Analog Conve	erter (DAC)	٠	•
Digital Signal Modulator	r (DSM)	•	•
EUSART		•	•
Fixed Voltage Referenc	e (FVR)	•	•
SR Latch	•	•	
Capture/Compare/PWN	1 Modules		
	ECCP1	•	•
	ECCP2	•	•
	CCP3	٠	•
	CCP4	٠	•
Comparators			
	C1	•	•
	C2	٠	•
Master Synchronous Se	erial Ports		
	MSSP1	٠	•
	MSSP2		•
Timers			
	Timer0	•	•
	Timer1	•	•
	Timer2	٠	•
	Timer4	•	•
	Timer6	•	•

3.4 Stack

All devices have a 16-level x 15-bit wide hardware stack (refer to Figures 3-4 through 3-7). The stack space is not part of either program or data space. The PC is PUSHed onto the stack when CALL or CALLW instructions are executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer if the STVREN bit is programmed to '0' (Configuration Word 2). This means that after the stack has been PUSHed sixteen times, the seventeenth PUSH overwrites the value that was stored from the first PUSH. The eighteenth PUSH overwrites the second PUSH (and so on). The STKOVF and STKUNF flag bits will be set on an Overflow/Underflow, regardless of whether the Reset is enabled.

Note 1: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, CALLW, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

3.4.1 ACCESSING THE STACK

The stack is available through the TOSH, TOSL and STKPTR registers. STKPTR is the current value of the Stack Pointer. TOSH:TOSL register pair points to the TOP of the stack. Both registers are read/writable. TOS is split into TOSH and TOSL due to the 15-bit size of the PC. To access the stack, adjust the value of STKPTR, which will position TOSH:TOSL, then read/write to TOSH:TOSL. STKPTR is five bits to allow detection of overflow and underflow.

Note:	Care should be taken when modifying the
	STKPTR while interrupts are enabled.

During normal program operation, CALL, CALLW and Interrupts will increment STKPTR while RETLW, RETURN, and RETFIE will decrement STKPTR. At any time STKPTR can be inspected to see how much stack is left. The STKPTR always points at the currently used place on the stack. Therefore, a CALL or CALLW will increment the STKPTR and then write the PC, and a return will unload the PC and then decrement the STKPTR.

Reference Figure 3-4 through Figure 3-7 for examples of accessing the stack.

FIGURE 3-4: ACCESSING THE STACK EXAMPLE 1

TOSH:TOSL 0x0F	STKPTR = 0x1F Stack Reset Disabled (STVREN = 0)
` 0х0Е	
0x0D	
0x0C	
0x0B	
0x0A	Initial Staals Configuration
0x09	
0x08	After Reset, the stack is empty. The empty stack is initialized so the Stack
0x07	Pointer is pointing at 0x1F. If the Stack Overflow/Underflow Reset is enabled, the
0x06	TOSH/TOSL registers will return '0'. If the Stack Overflow/Underflow Reset is
0x05	disabled, the TOSH/TOSL registers will return the contents of stack address 0x0E
0x04	
0x03	
0x02	
0x01	
0x00	
TOSH:TOSL 0x1F 0x0000	STKPTR = 0x1F Stack Reset Enabled (STVREN = 1)

4.5 Device ID and Revision ID

The memory location 8006h is where the Device ID and Revision ID are stored. The upper nine bits hold the Device ID. The lower five bits hold the Revision ID. See **Section 11.5 "User ID, Device ID and Configuration Word Access**" for more information on accessing these memory locations.

Development tools, such as device programmers and debuggers, may be used to read the Device ID and Revision ID.

REGISTER 4-3: DEVICEID: DEVICE ID REGISTER⁽¹⁾

		R	R	R	R	R	R
		DEV8	DEV7	DEV6	DEV5	DEV4	DEV3
		bit 13					bit 8
R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0
Legend:							
R = Readable bit		'0' = Bit is clear	ed	'1' = Bit is set			
bit 13-5	DEV<8:0>: Device ID bits						
	100111011 = PIC16F1825						
	100111111 = PIC16F1829						
	101000011 = PIC	C16LF1825					
	101000111 = PIC	16LF1829					
bit 4-0	REV<4:0>: Revision ID bits						
	These bits are use	ed to identify the	revision.				

Note 1: This location cannot be written.

8.6 Interrupt Control Registers

8.6.1 INTCON REGISTER

The INTCON register is a readable and writable register, that contains the various enable and flag bits for TMR0 register overflow, interrupt-on-change and external INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 8-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0/0	R-0/0						
GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF ⁽¹⁾
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	GIE: Global Interrupt Enable bit
	1 = Enables all active interrupts 0 = Disables all interrupts
bit 6	PEIE: Peripheral Interrupt Enable bit 1 = Enables all active peripheral interrupts 0 = Disables all peripheral interrupts
bit 5	TMR0IE: Timer0 Overflow Interrupt Enable bit 1 = Enables the Timer0 interrupt 0 = Disables the Timer0 interrupt
bit 4	INTE: INT External Interrupt Enable bit 1 = Enables the INT external interrupt 0 = Disables the INT external interrupt
bit 3	IOCIE: Interrupt-on-Change Enable bit 1 = Enables the interrupt-on-change 0 = Disables the interrupt-on-change
bit 2	TMR0IF: Timer0 Overflow Interrupt Flag bit 1 = TMR0 register has overflowed 0 = TMR0 register did not overflow
bit 1	INTF: INT External Interrupt Flag bit 1 = The INT external interrupt occurred 0 = The INT external interrupt did not occur
bit 0	IOCIF: Interrupt-on-Change Interrupt Flag bit ⁽¹⁾ 1 = When at least one of the interrupt-on-change pins changed state 0 = None of the interrupt-on-change pins have changed state
Note 1:	The IOCIF Flag bit is read-only and cleared when all the Interrupt-on-Change flags in the IOCxF register

Note 1: The IOCIF Flag bit is read-only and cleared when all the Interrupt-on-Change flags in the IOCxF register have been cleared by software.

15.0 TEMPERATURE INDICATOR MODULE

This family of devices is equipped with a temperature circuit designed to measure the operating temperature of the silicon die. The circuit's range of operating temperature falls between -40°C and +85°C. The output is a voltage that is proportional to the device temperature. The output of the temperature indicator is internally connected to the device ADC.

The circuit may be used as a temperature threshold detector or a more accurate temperature indicator, depending on the level of calibration performed. A one-point calibration allows the circuit to indicate a temperature closely surrounding that point. A two-point calibration allows the circuit to sense the entire range of temperature more accurately. Reference Application Note AN1333, *"Use and Calibration of the Internal Temperature Indicator"* (DS01333) for more details regarding the calibration process.

15.1 Circuit Operation

Figure 15-1 shows a simplified block diagram of the temperature circuit. The proportional voltage output is achieved by measuring the forward voltage drop across multiple silicon junctions.

Equation 15-1 describes the output characteristics of the temperature indicator.

EQUATION 15-1: VOUT RANGES

High Range: VOUT = VDD - 4VT

Low Range: VOUT = VDD - 2VT

The temperature sense circuit is integrated with the Fixed Voltage Reference (FVR) module. See **Section 14.0 "Fixed Voltage Reference (FVR)"** for more information.

The circuit is enabled by setting the TSEN bit of the FVRCON register. When disabled, the circuit draws no current.

The circuit operates in either high or low range. The high range, selected by setting the TSRNG bit of the FVRCON register, provides a wider output voltage. This provides more resolution over the temperature range, but may be less consistent from part to part. This range requires a higher bias voltage to operate and thus, a higher VDD is needed.

The low range is selected by clearing the TSRNG bit of the FVRCON register. The low range generates a lower voltage drop and thus, a lower bias voltage is needed to operate the circuit. The low range is provided for low voltage operation.

FIGURE 15-1: TEMPERATURE CIRCUIT DIAGRAM



15.2 Minimum Operating VDD vs. Minimum Sensing Temperature

When the temperature circuit is operated in low range, the device may be operated at any operating voltage that is within specifications.

When the temperature circuit is operated in high range, the device operating voltage, VDD, must be high enough to ensure that the temperature circuit is correctly biased.

Table 15-1 shows the recommended minimum VDD vs. range setting.

TABLE 15-1: RECOMMENDED VDD VS. RANGE

Min. VDD, TSRNG = 1	Min. VDD, TSRNG = 0
3.6V	1.8V

15.3 Temperature Output

The output of the circuit is measured using the internal Analog-to-Digital converter. A channel is reserved for the temperature circuit output. Refer to **Section 16.0 "Analog-to-Digital Converter (ADC) Module"** for detailed information.

15.4 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait at least 200 μ s after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200 μ s between sequential conversions of the temperature indicator output.

17.0 DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 32 selectable output levels.

The input of the DAC can be connected to:

- External VREF pins
- VDD supply voltage
- FVR Buffer2

The output of the DAC can be configured to supply a reference voltage to the following:

- Comparator positive input
- ADC input channel
- DACOUT pin
- · Capacitive Sensing module (CPS)

The Digital-to-Analog Converter (DAC) can be enabled by setting the DACEN bit of the DACCON0 register.

EQUATION 17-1: DAC OUTPUT VOLTAGE

<u>**IF DACEN = 1**</u> $VOUT = \left((VSOURCE - VSOURCE -) \times \frac{DACR[4:0]}{2^5} \right) + VSOURCE -$

IF DACEN = 0 and DACLPS = 1 and DACR[4:0] = 11111

VOUT = VSOURCE +

IF DACEN = 0 and DACLPS = 0 and DACR[4:0] = 00000

VOUT = VSOURCE -

VSOURCE+ = VDD, VREF, or FVR BUFFER 2

VSOURCE - = VSS

17.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

The value of the individual resistors within the ladder can be found in **Section 30.0** "**Electrical Specifications**".

17.1 Output Voltage Selection

The DAC has 32 voltage level ranges. The 32 levels are set with the DACR<4:0> bits of the DACCON1 register.

The DAC output voltage is determined by the following equations:

17.3 DAC Voltage Reference Output

The DAC can be output to the DACOUT pin by setting the DACOE bit of the DACCON0 register to '1'. Selecting the DAC reference voltage for output on the DACOUT pin automatically overrides the digital output buffer and digital input threshold detector functions of that pin. Reading the DACOUT pin when it has been configured for DAC reference voltage output will always return a '0'.

Due to the limited current drive capability, a buffer must be used on the DAC voltage reference output for external connections to DACOUT. Figure 17.5 shows an example buffering technique.

17.7 DAC Control Registers

REGISTER 17-1: DACCONO: VOLTAGE REFERENCE CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	U-0	R/W-0/0
DACEN	DACLES	DACOE	_		SS<1:0>	_	DACNSS
bit 7	DROEFO	DROOL		Briory	00 11.02		bit 0
Sit 7							
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'	
u = Bit is uncha	anged	x = Bit is unkr	iown	-n/n = Value a	at POR and BO	R/Value at all o	other Resets
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7	Dit 7 DACEN: DAC Enable bit 1 = DAC is enabled D = DAC is discalled						
bit 6	DACLPS: DA	C Low-Power '	Voltage State	Select bit			
	1 = DAC Positive reference source selected 0 = DAC Negative reference source selected						
bit 5	 DACOE: DAC Voltage Output Enable bit 1 = DAC voltage level is also an output on the DACOUT pin 0 = DAC voltage level is disconnected from the DACOUT pin 						
bit 4	it 4 Unimplemented: Read as '0'						
bit 3-2	3-2 DACPSS<1:0>: DAC Positive Source Select bits 00 = VDD 01 = VREF+ 10 = FVR Buffer2 output 11 = Reserved, do not use						
bit 1	Unimplemen	ted: Read as '	כי				
bit 0	DACNSS: DAC Negative Source Select bits 1 = VREF- 0 = VSS						

REGISTER 17-2: DACCON1: VOLTAGE REFERENCE CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—			DACR<4:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 Unimplemented: Read as '0'	
------------------------------------	--

```
bit 4-0 DACR<4:0>: DAC Voltage Output Select bits
```

Vout = ((Vsrc+) - (Vsrc-))*(DACR<4:0>/(2⁵)) + Vsrc-

Note 1: The output select bits are always right justified to ensure that any number of bits can be used without affecting the register layout

R/W-0/0	R-0/0	R/W-0/0	R/W-0/0	U-0	R/W-1/1	R/W-0/0	R/W-0/0	
CxON	CxOUT	CxOE	CxPOL	_	CxSP	CxHYS	CxSYNC	
bit 7		·	•	·			bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'		
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value a	at POR and BC	R/Value at all	other Resets	
'1' = Bit is set		'0' = Bit is cle	'0' = Bit is cleared					
bit 7	CxON: Comp	arator Enable	bit					
	1 = Compara	tor is enabled						
	0 = Compara	tor is disabled	and consumes	s no active pow	er			
bit 6	CxOUT: Com	parator Output	bit					
	$\frac{\text{If CxPOL} = 1}{1 - CyVD < 0}$	(inverted polar	<u>ity):</u>					
	1 = CXVP < 0 0 = CXVP > 0							
	If $CxPOL = 0$	(non-inverted)	<u>oolarity):</u>					
	1 = CxVP > 0							
bit 5	$0 = C_{XVP} < 0$	OXVIN Approximation	Enabla bit					
DIL 5	$1 = C \times O \cup T $	s present on th		Requires that th	ne associated T	RIS hit he clea	red to actually	
	drive the	pin. Not affect	ed by CxON.					
	0 = CxOUT i	s internal only						
bit 4	CxPOL: Com	parator Output	Polarity Select	ct bit				
	1 = Compara	tor output is inv	/erted					
hit 3		tor output is no						
bit 2	CxSP: Comp	arator Speed/F	o ∕ower Select h	it				
Sit 2	1 = Compara	tor operates in	normal power	, higher speed	mode			
	0 = Comparator operates in low-power, low-speed mode							
bit 1	CxHYS: Comparator Hysteresis Enable bit							
	1 = Compara	ator hysteresis	enabled					
h # 0	0 = Comparator hysteresis disabled							
U JID	It U CXSYNC: Comparator Output Synchronous Mode bit							
	Output updated on the falling edge of Timer1 clock source.							
	0 = Compara	ator output to T	imer1 and I/O	pin is asynchro	nous.			

REGISTER 19-1: CMxCON0: COMPARATOR Cx CONTROL REGISTER 0

FIGURE 23-4:	CARRIER LOW SYNCHRONIZATION (MDSHSYNC = 0, MDCLSYNC = 1)
Carrier High (CARH)	
Carrier Low (CARL)	
Modulator (MOD)	
MDCHSYNC = 0 MDCLSYNC = 1	
Active Carrier State	CARH X CARL CARH X CARL



24.4.2 FULL-BRIDGE MODE

In Full-Bridge mode, all four pins are used as outputs. An example of full-bridge application is shown in Figure 24-10.

In the Forward mode, pin CCPx/PxA is driven to its active state, pin PxD is modulated, while PxB and PxC will be driven to their inactive state as shown in Figure 24-11.

In the Reverse mode, PxC is driven to its active state, pin PxB is modulated, while PxA and PxD will be driven to their inactive state as shown Figure 24-11.

PxA, PxB, PxC and PxD outputs are multiplexed with the PORT data latches. The associated TRIS bits must be cleared to configure the PxA, PxB, PxC and PxD pins as outputs.

FIGURE 24-10: EXAMPLE OF FULL-BRIDGE APPLICATION



25.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSPxCON2 register. When this bit is set, the SCLx pin is pulled low and the contents of the Acknowledge data bit are presented on the SDAx pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCLx pin is deasserted (pulled high). When the SCLx pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCLx pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSPx module then goes into Idle mode (Figure 25-30).

25.6.8.1 WCOL Status Flag

If the user writes the SSPxBUF when an Acknowledge sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

STOP CONDITION TIMING 25.6.9

A Stop bit is asserted on the SDAx pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSPxCON2 register. At the end of a receive/transmit, the SCLx line is held low after the falling edge of the ninth clock. When the PEN bit is set. the master will assert the SDAx line low. When the SDAx line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCLx pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDAx pin will be deasserted. When the SDAx pin is sampled high while SCLx is high, the P bit of the SSPxSTAT register is set. A TBRG later, the PEN bit is cleared and the SSPxIF bit is set (Figure 25-31).

25.6.9.1 WCOL Status Flag

If the user writes the SSPxBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).



FIGURE 25-30: ACKNOWLEDGE SEQUENCE WAVEFORM



FIGURE 25-31: STOP CONDITION RECEIVE OR TRANSMIT MODE



25.6.13.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

- a) After the SDAx pin has been deasserted and allowed to float high, SDAx is sampled low after the BRG has timed out. (CASE 1)
- b) After the SCLx pin is deasserted, SCLx is sampled low before SDAx goes high. (CASE 2)

The Stop condition begins with SDAx asserted low. When SDAx is sampled low, the SCLx pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSPxADD and counts down to zero. After the BRG times out, SDAx is sampled. If SDAx is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 25-38). If the SCLx pin is sampled low before SDAx is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 25-39).

FIGURE 25-38: BUS COLLISION DURING A STOP CONDITION (CASE 1)



FIGURE 25-39: BUS COLLISION DURING A STOP CONDITION (CASE 2)



FIGURE 26-2: EUSART RECEIVE BLOCK DIAGRAM



The operation of the EUSART module is controlled through three registers:

- Transmit Status and Control (TXSTA)
- Receive Status and Control (RCSTA)
- Baud Rate Control (BAUDCON)

These registers are detailed in Register 26-1, Register 26-2 and Register 26-3, respectively.

When the receiver or transmitter section is not enabled then the corresponding RX or TX pin may be used for general purpose input and output.





TABLE 26-1: SUMMARY OF REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON0	RXDTSEL	SDO1SEL ⁽²⁾	SS1SEL ⁽²⁾		T1GSEL	TXCKSEL		—	118
BAUDCON	ABDOVF	RCIDL	_	SCKP	BRG16	_	WUE	ABDEN	292
INLVLA ⁽³⁾	—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	124
INLVLB ⁽¹⁾	INLVLB7	INLVLB6	INLVLB5	INLVLB4		_		_	129
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	135
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	87
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	88
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	92
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	291
SPBRGL	SPBRG<7:0>								293*
SPBRGH	SPBRG<15:8>								293*
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	122
TRISB ⁽¹⁾	TRISB7	TRISB6	TRISB5	TRISB4	-	—	—	—	128
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	133
TXREG	EUSART Transmit Data Register								283
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	290

Legend: — Unimplemented location, read as '0'. Shaded cells are not used for asynchronous transmission.

* Page provides register information.

Note 1: PIC16(L)F1829 only.

2: PIC16(L)F1825 only.

3: Unshaded cells apply to PIC16(L)F1825 only.

26.1.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCSTA register which resets the EUSART. Clearing the CREN bit of the RCSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

Note:	If all receive characters in the receive						
	FIFO have framing errors, repeated reads						
	of the RCREG will not clear the FERR bit.						

26.1.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCSTA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCSTA register or by resetting the EUSART by clearing the SPEN bit of the RCSTA register.

26.1.2.6 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

26.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.









FIGURE 31-55: COMPARATOR HYSTERESIS, LOW-POWER MODE (CxSP = 0, CxHYS = 1)



33.1 Package Marking Information (Continued)



16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (JQ) - 4x4x0.5 mm Body [UQFN]





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20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





l	Jnits	Ν	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	
Number of Pins	Ν	20			
Pitch	е		1.27 BSC		
Overall Height	А	-	-	2.65	
Molded Package Thickness	A2	2.05	-	-	
Standoff §	A1	0.10	-	0.30	
Overall Width	Е	10.30 BSC			
Molded Package Width	E1	7.50 BSC			
Overall Length	D	12.80 BSC			
Chamfer (Optional)	h	0.25	-	0.75	
Foot Length	L	0.40	-	1.27	
Footprint	L1	1.40 REF			
Lead Angle	Θ	0°	-	-	
Foot Angle	φ	0°	-	8°	
Lead Thickness	С	0.20	-	0.33	
Lead Width	b	0.31	-	0.51	
Mold Draft Angle Top	α	5°	-	15°	
Mold Draft Angle Bottom	β	5°	-	15°	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

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