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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1829t-i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

0/	14-Pin PDIP/SOIC/TSSOP	16-Pin QFN/UQFN	A/D	Reference	Cap Sense	Comparator	SR Latch	Timers	ECCP	EUSART	ASSM	Interrupt	Modulator	Pull-up	Basic
RA0	13	12	AN0	VREF- DACOUT	CPS0	C1IN+	—			TX ⁽¹⁾ CK ⁽¹⁾		IOC	—	Y	ICSPDAT ICDDAT
RA1	12	11	AN1	VREF+	CPS1	C12IN0-	SRI			RX ⁽¹⁾ DT ⁽¹⁾		IOC	—	Y	ICSPCLK ICDCLK
RA2	11	10	AN2	-	CPS2	C1OUT	SRQ	TOCKI	CCP3 FLT0	-	-	INT/ IOC	-	Y	-
RA3	4	3	_	_	_	_	—	T1G ⁽¹⁾	_	_	SS1 ⁽¹⁾	IOC	_	Y	MCLR VPP
RA4	3	2	AN3	_	CPS3	_	_	T1G ⁽¹⁾ T1OSO	P2B ⁽¹⁾	_	SDO1 ⁽¹⁾	IOC	_	Y	OSC2 CLKOUT CLKR
RA5	2	1	_	—	-		—	T1CKI T1OSI	CCP2 P2A ⁽¹⁾			IOC	—	Y	OSC1 CLKIN
RC0	10	9	AN4	—	CPS4	C2IN+	_		P1D ⁽¹⁾		SCL SCK		—	Y	
RC1	9	8	AN5	—	CPS5	C12IN1-	_	1	CCP4 P1C ⁽¹⁾		SDA SDI		—	Y	
RC2	8	7	AN6	—	CPS6	C12IN2-	_		P1D ⁽¹⁾ P2B ⁽¹⁾		SDO1 ⁽¹⁾		MDCIN1	Y	
RC3	7	6	AN7	—	CPS7	C12IN3-	—		CCP2 ⁽¹⁾ P1C ⁽¹⁾ P2A ⁽¹⁾		SS1 ⁽¹⁾		MDMIN	Y	_
RC4	6	5		_		C2OUT	SRNQ		P1B	TX ⁽¹⁾ CK ⁽¹⁾			MDOUT	Y	_
RC5	5	4	_		_	_		_	CCP1 P1A	RX ⁽¹⁾ DT ⁽¹⁾	_	_	MDCIN2	Y	_
Vdd	1	16	—	—	—	—	—	_	—	—	_	—	—	—	Vdd
Vss	14	13	—	—	—	—	—	—	—	—	—	—	—	—	Vss

TABLE 1: 14-PIN AND 16-PIN ALLOCATION TABLE (PIC16(L)F1825)

Note 1: Pin function is selectable via the APFCON0 or APFCON1 register.

HPINTOSC/	GURE 5-7:	INTERNAL OSCILLATOR SWITCH TIMING
HEINTOSC/		
HFINTOSC John Soc Remark IRCF <3:0> ≠0 =0 System Clock	363830302	LPINTOSC (PSCM and WOT distabled)
Minintosci Creditory Dolg/31 (Storale Basic Remitty LFINTOSC #0 =0 IRCF <3:0> #0 =0 System Clock		
LFINTOSC #0 =0 System Clock	MENTOSC	Cardinator Onlay ⁶³ Science Synce Running
IRCF <3:0> ≠0 =0 System Clock	LFINTOSC	
System Clock	IRCF <3:0>	$\neq 0$ $= 0$
PHYNYIOSCI LFINTOSC (EIBHAR PISCAI or WDY enabled) HFINTOSC LFINTOSC LFINTOSC IRCF <3:0> = 0 = 0 System Clock UFINTOSC NETINTOSC/MEENTOSC LFINTOSC NETINTOSC/MEENTOSC	System Clock	
HFINTOSC/ NETIMICAL 24-yes Presides LFINTOSC 24-yes Presides IRCF <3:0> # 0 = 0 System Clock	NENETOSO/	LFINTOSC (ERHer POCM of WOT shabiled)
NETRITION 2xyest kyst Provint LFINTOSC ≠ 0 = 0 IRCF <3:0> ≠ 0 = 0 System Clock	HFINTOSC/	
LFINTOSC	terran rana.	l <u>iji 2-ovota konta</u> liji <u>Posasino</u>
IRCF <3:0> = 0 = 0 System Clock	LFINTOSC	
System Clock	IRCF <3:0>	$\neq 0$ $\chi = 0$
System Clock		
LEBYTOSC NEINTOSC/REFINITOSC LEVELOSC Lange off ontone WOY or PSCNA is enabled LEVELOSC Lange off ontone WOY or PSCNA is enabled Originator Geogr ⁽¹¹) Crystic Sync (Accessing) MENOTOSC (PCP < 3:62	System Clock	
LEINTOSC NEENTOSC/BEEENTOSC LEINTOSC LEINTOSC/BEEENTOSC LEINTOSC LEINTOSC/ MEENTOSC/ MEENTOSC		
CERVICUSC EXERCISSCONCENENCISC LEVICUSC tures of unious WSY or FSOM is enabled CRIMINOSC HEVETOSC System Clook	n ann na h-ann an an an	
LERRITOSC	- 1922 I 1997	PERMITERAL METAL AND COMPANY
Childran Gaoy ⁽¹⁾ (2-syste Sanc.) HIPENTOSC HIPENTOSC HIPENTOSC System Cloope	LEBITOSC	
bifin(TOBC/ MFIN(TOBC) Image: Control of the contro		California California Computer Sona 🕴 🦷 🥵 🥵 🥵
9:CF <3:G> <u>2:C</u> <u>7:0</u> System Ci>>> []	MENTOSC/ MENTOSC	
	\$2CE <3:0>	
aamaamaamaamaamaamaamaamaamaa	System Crock	

11.2 Using the Data EEPROM

The data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). When variables in one section change frequently, while variables in another section do not change, it is possible to exceed the total number of write cycles to the EEPROM without exceeding the total number of write cycles to a single byte. Refer to **Section 30.0 "Electrical Specifications**". If this is the case, then a refresh of the array must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in Flash program memory.

11.2.1 READING THE DATA EEPROM MEMORY

To read a data memory location, the user must write the address to the EEADRL register, clear the EEPGD and CFGS control bits of the EECON1 register, and then set control bit RD. The data is available at the very next cycle, in the EEDATL register; therefore, it can be read in the next instruction. EEDATL will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 11-1: DATA EEPROM READ

BANKSEL	EEADRL	i
MOVLW	DATA_EE_ADDR	;
MOVWF	EEADRL	;Data Memory
		;Address to read
BCF	EECON1, CFGS	;Deselect Config space
BCF	EECON1, EEPG	D;Point to DATA memory
BSF	EECON1, RD	;EE Read
MOVF	EEDATL, W	;W = EEDATL

Note: Data EEPROM can be read regardless of the setting of the CPD bit.

11.2.2 WRITING TO THE DATA EEPROM MEMORY

To write an EEPROM data location, the user must first write the address to the EEADRL register and the data to the EEDATL register. Then the user must follow a specific sequence to initiate the write for each byte.

The write will not initiate if the above sequence is not followed exactly (write 55h to EECON2, write AAh to EECON2, then set the WR bit) for each byte. Interrupts should be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. EEIF must be cleared by software.

11.2.3 PROTECTION AGAINST SPURIOUS WRITE

There are conditions when the user may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built-in. On power-up, WREN is cleared. Also, the Power-up Timer (64 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during:

- Brown-out
- · Power glitch
- · Software malfunction

11.2.4 DATA EEPROM OPERATION DURING CODE-PROTECT

Data memory can be code-protected by programming the CPD bit in the Configuration Word 1 (Register 5-1) to '0'.

When the data memory is code-protected, only the CPU is able to read and write data to the data EEPROM. It is recommended to code-protect the program memory when code-protecting data memory. This prevents anyone from replacing your program with a program that will access the contents of the data EEPROM.

REGISTER 12-9: PORTB: PORTB REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0
RB7	RB6	RB5	RB4		—		_
bit 7							bit 0
Legend:							
R = Readable I	oit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
u = Bit is uncha	anged	x = Bit is unkn	nown	-n/n = Value a	at POR and BO	R/Value at all o	ther Resets
'1' = Bit is set		'0' = Bit is clea	ared				

bit 7-4	RB<7:4> : PORTB General Purpose I/O Pin bits
	1 = Port pin is <u>></u> Vін
	0 = Port pin is <u><</u> VI ∟
bit 3-0	Unimplemented: Read as '0'

REGISTER 12-10: TRISB: PORTB TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0
TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **TRISB<7:4>:** PORTB Tri-State Control bits 1 = PORTB pin configured as an input (tri-stated) 0 = PORTB pin configured as an output

bit 3-0 Unimplemented: Read as '0'

REGISTER 12-11: LATB: PORTB DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0
LATB7	LATB6	LATB5	LATB4	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 LATB<7:4>: PORTB Output Latch Value bits⁽¹⁾

bit 3-0 Unimplemented: Read as '0'

Note 1: Writes to PORTB are actually written to corresponding LATB register. Reads from PORTB register is return of actual I/O pin values.

12.4.2 PORTC FUNCTIONS AND OUTPUT PRIORITIES

Each PORTC pin is multiplexed with other functions. The pins, their combined functions and their output priorities are briefly described here. For additional information, refer to the appropriate section in this data sheet.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the lowest number in the following lists.

Analog input and some digital input functions are not included in the list below. These input functions can remain active when the pin is configured as an output. Certain digital input functions override other port functions and are included in the priority list.

Pin Name	Function Priority ⁽¹⁾
RC0	SCL (PIC16(L)F1825 only) SCK (PIC16(L)F1825 only) P1D ⁽²⁾
RC1	SDA1 (PIC16(L)F1825 only) SDA1 (PIC16(L)F1825 only) P1C ⁽²⁾
RC2	SDO1 ⁽²⁾ (PIC16(L)F1825 only) P1D ⁽²⁾ P2B ⁽²⁾
RC3	SS1 ⁽²⁾ (PIC16(L)F1825 only) CCP2 ⁽²⁾ P1C ⁽²⁾ P2A ⁽²⁾
RC4	MDOUT SRNQ C2OUT TX ⁽²⁾ /CK ⁽²⁾ P1B
RC5	RX ⁽²⁾ /DT ⁽²⁾ CCP1/P1A
RC6 ⁽³⁾	SS1 CCP4
RC7 ⁽³⁾	SDO1

TABLE 12-7: PORTC OUTPUT PRIORITY

Note 1: Priority listed from highest to lowest.

2: Pin function is selectable via the APFCON0 or APFCON1 register.

3: PIC16(L)F1829 only.

15.0 TEMPERATURE INDICATOR MODULE

This family of devices is equipped with a temperature circuit designed to measure the operating temperature of the silicon die. The circuit's range of operating temperature falls between -40°C and +85°C. The output is a voltage that is proportional to the device temperature. The output of the temperature indicator is internally connected to the device ADC.

The circuit may be used as a temperature threshold detector or a more accurate temperature indicator, depending on the level of calibration performed. A one-point calibration allows the circuit to indicate a temperature closely surrounding that point. A two-point calibration allows the circuit to sense the entire range of temperature more accurately. Reference Application Note AN1333, *"Use and Calibration of the Internal Temperature Indicator"* (DS01333) for more details regarding the calibration process.

15.1 Circuit Operation

Figure 15-1 shows a simplified block diagram of the temperature circuit. The proportional voltage output is achieved by measuring the forward voltage drop across multiple silicon junctions.

Equation 15-1 describes the output characteristics of the temperature indicator.

EQUATION 15-1: VOUT RANGES

High Range: VOUT = VDD - 4VT

Low Range: VOUT = VDD - 2VT

The temperature sense circuit is integrated with the Fixed Voltage Reference (FVR) module. See **Section 14.0 "Fixed Voltage Reference (FVR)"** for more information.

The circuit is enabled by setting the TSEN bit of the FVRCON register. When disabled, the circuit draws no current.

The circuit operates in either high or low range. The high range, selected by setting the TSRNG bit of the FVRCON register, provides a wider output voltage. This provides more resolution over the temperature range, but may be less consistent from part to part. This range requires a higher bias voltage to operate and thus, a higher VDD is needed.

The low range is selected by clearing the TSRNG bit of the FVRCON register. The low range generates a lower voltage drop and thus, a lower bias voltage is needed to operate the circuit. The low range is provided for low voltage operation.

FIGURE 15-1: TEMPERATURE CIRCUIT DIAGRAM



15.2 Minimum Operating VDD vs. Minimum Sensing Temperature

When the temperature circuit is operated in low range, the device may be operated at any operating voltage that is within specifications.

When the temperature circuit is operated in high range, the device operating voltage, VDD, must be high enough to ensure that the temperature circuit is correctly biased.

Table 15-1 shows the recommended minimum VDD vs. range setting.

TABLE 15-1: RECOMMENDED VDD VS. RANGE

Min. VDD, TSRNG = 1	Min. VDD, TSRNG = 0
3.6V	1.8V

15.3 Temperature Output

The output of the circuit is measured using the internal Analog-to-Digital converter. A channel is reserved for the temperature circuit output. Refer to **Section 16.0 "Analog-to-Digital Converter (ADC) Module"** for detailed information.

15.4 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait at least 200 μ s after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200 μ s between sequential conversions of the temperature indicator output.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	—			CHS<4:0>			GO/DONE	ADON	150
ADCON1	ADFM		ADCS<2:0>		—	ADNREF	ADPR	EF<1:0	151
ADRESH	A/D Result Re	egister High							152, 153
ADRESL	A/D Result Re	egister Low							152, 153
ANSELA	—	_	_	ANSA4	_	ANSA2	ANSA1	ANSA0	123
ANSELB ⁽¹⁾	—	_	ANSB5	ANSB4	_	—	—	—	129
ANSELC	ANSC7 ⁽¹⁾	ANSC6 ⁽¹⁾	_	—	ANSC3	ANSC2	ANSC1	ANSC0	134
CCP4CON	P4M•	<1:0>	DC4B	l<1:0>		CCP4M<3:0>			
INLVLA	_	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	124
INLVLB ⁽¹⁾	INLVLB7	INLVLB6	INLVLB5	INLVLB4	_	_	_	—	129
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	135
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	87
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	88
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	92
TRISA	—	-	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	122
TRISB ⁽¹⁾	TRISB7	TRISB6	TRISB5	TRISB4	_	—	—	—	128
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	133
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFV	′R<1:0>	ADFVR<1:0>		142
DACCON0	DACEN	DACLPS	DACOE	- DACPSS<1:0>			_	160	
DACCON1	—	_	_			DACR<4:0>			160

TABLE 16-3: SUMMARY OF REGISTERS ASSOCIATED WITH ADC

x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends on condition. Shaded cells are not used for ADC Legend: module. PIC16(L)F1829 only.

Note 1:

21.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

21.4 Timer1 Oscillator

A dedicated low-power 32.768 kHz oscillator circuit is built-in between pins T1OSI (input) and T1OSO (amplifier output). This internal circuit is to be used in conjunction with an external 32.768 kHz crystal.

The oscillator circuit is enabled by setting the T1OSCEN bit of the T1CON register. The oscillator will continue to run during Sleep.

Note: The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to using Timer1. A suitable delay similar to the OST delay can be implemented in software by clearing the TMR1IF bit then presetting the TMR1H:TMR1L register pair to FC00h. The TMR1IF flag will be set when 1024 clock cycles have elapsed, thereby indicating that the oscillator is running and reasonably stable.

21.5 Timer1 Operation in Asynchronous Counter Mode

If control bit T1SYNC of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If the external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see Section 21.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode").

Note:	When switching from synchronous to
	asynchronous operation, it is possible to
	skip an increment. When switching from
	asynchronous to synchronous operation,
	it is possible to produce an additional
	increment.

21.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

21.6 Timer1 Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using Timer1 gate circuitry. This is also referred to as Timer1 Gate Enable.

Timer1 gate can also be driven by multiple selectable sources.

21.6.1 TIMER1 GATE ENABLE

The Timer1 Gate Enable mode is enabled by setting the TMR1GE bit of the T1GCON register. The polarity of the Timer1 Gate Enable mode is configured using the T1GPOL bit of the T1GCON register.

When Timer1 Gate Enable mode is enabled, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 Gate Enable mode is disabled, no incrementing will occur and Timer1 will hold the current count. See Figure 21-3 for timing details.

TABLE 21-3: TIMER1 GATE ENABLE SELECTIONS

T1CLK	T1GPOL	T1G	Timer1 Operation
\uparrow	0	0	Counts
\uparrow	0	1	Holds Count
\uparrow	1	0	Holds Count
1	1	1	Counts

22.1 Timer2/4/6 Operation

The clock input to the Timer2/4/6 modules is the system instruction clock (Fosc/4).

TMRx increments from 00h on each clock edge.

A 4-bit counter/prescaler on the clock input allows direct input, divide-by-4 and divide-by-16 prescale options. These options are selected by the prescaler control bits, TxCKPS<1:0> of the TxCON register. The value of TMRx is compared to that of the Period register, PRx, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal also resets the value of TMRx to 00h on the next cycle and drives the output counter/postscaler (see Section 22.2 "Timer2/4/6 Interrupt").

The TMRx and PRx registers are both directly readable and writable. The TMRx register is cleared on any device Reset, whereas the PRx register initializes to FFh. Both the prescaler and postscaler counters are cleared on the following events:

- a write to the TMRx register
- · a write to the TxCON register
- · Power-on Reset (POR)
- Brown-out Reset (BOR)
- MCLR Reset
- · Watchdog Timer (WDT) Reset
- Stack Overflow Reset
- Stack Underflow Reset
- RESET Instruction

Note: TMRx is not cleared when TxCON is written.

22.2 Timer2/4/6 Interrupt

Timer2/4/6 can also generate an optional device interrupt. The Timer2/4/6 output signal (TMRx-to-PRx match) provides the input for the 4-bit counter/postscaler. This counter generates the TMRx match interrupt flag which is latched in TMRxIF of the PIRx register. The interrupt is enabled by setting the TMRx Match Interrupt Enable bit, TMRxIE of the PIEx register.

A range of 16 postscale options (from 1:1 through 1:16 inclusive) can be selected with the postscaler control bits, TxOUTPS<3:0>, of the TxCON register.

22.3 Timer2/4/6 Output

The unscaled output of TMRx is available primarily to the CCP modules, where it is used as a time base for operations in PWM mode.

Timer2 can be optionally used as the shift clock source for the MSSPx modules operating in SPI mode. Additional information is provided in Section 25.0 "Master Synchronous Serial Port (MSSP1 and MSSP2) Module".

22.4 Timer2/4/6 Operation During Sleep

The Timer2/4/6 timers cannot be operated while the processor is in Sleep mode. The contents of the TMRx and PRx registers will remain unchanged while the processor is in Sleep mode.

FIGURE 25-9.	SPI MODE WAVEFORM		
FIGURE 23-9.	SFI WODE WAVEFORW	(SLAVE WODE WITH CRE = 0)	

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Write Collinear											
deteción activo											

FIGURE 25-10: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)

SSx SCKx (CKP = 0 CKE = 1) SCKx (CKP = 1 CKE = 1) Write to					
SSPxBUF		1 1 1 1 1 1 1 1 1 111			
SDOX	bit 7 bit 6	bit 5 bit 4	bit 3 bit 2	bit 1 bit 0	
SDIx	bit 7		\sim	bit 0	
Input Sample	<u> </u>	<u>↑</u> ↑	<u>†</u> †	<u>†</u> †	· · ·
SSPxIF Interrupt Flag					
SSPxSR to SSPxBUF		1 1 1 1 1 1 1 1 1 1 1 1		1 I 1 I 1 I 1 I	-
Write Collisies			•		•

25.2.6 SPI OPERATION IN SLEEP MODE

In SPI Master mode, module clocks may be operating at a different speed than when in full power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSPx clock is much faster than the system clock.

In Slave mode, when MSSPx interrupts are enabled, after the master completes sending data, an MSSPx interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSPx interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the MSSPx interrupt flag bit will be set and if enabled, will wake the device.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	_	—	ANSA4	_	ANSA2	ANSA1	ANSA0	122
ANSELB ⁽¹⁾	_	_	ANSB5	ANSB4	_	_	_	—	129
ANSELC	ANSC7 ⁽¹⁾	ANSC6 ⁽¹⁾	_	_	ANSC3	ANSC2	ANSC1	ANSC0	134
APFCON0	RXDTSEL	SDO1SEL ⁽²⁾	SS1SEL ⁽²⁾	_	T1GSEL	TXCKSEL	—	_	118
APFCON1	—	-	SDO2SEL ⁽¹⁾	SS2SEL ⁽¹⁾	P1DSEL	P1CSEL	P2BSEL	CCP2SEL	119
INLVLA	—	_	INLVLA5 ⁽¹⁾	INLVLA4 ⁽¹⁾	INLVLA3	INLVLA2	INLVLA1	INLVLA0	124
INLVLB ⁽¹⁾	INLVLB7	INLVLB6	INLVLB5	INLVLB4	-	—	—	—	129
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1 ⁽¹⁾	INLVLC0 ⁽¹⁾	135
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	87
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	88
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	92
SSP1BUF	Synchronous	Serial Port Rece	eive Buffer/Tran	smit Register					233*
SSP1CON1	WCOL	SSPOV	SSPEN	CKP		SSPM	<3:0>		277
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	279
SSP1STAT	SMP	CKE	D/Ā	Р	S	R/W	UA	BF	276
TRISA	_	_	TRISA5 ⁽¹⁾	TRISA4 ⁽¹⁾	TRISA3	TRISA2	TRISA1	TRISA0	122
TRISB ⁽¹⁾	TRISB7	TRISB6	TRISB5	TRISB4	_	—	—	_	128
TRISC	TRISC7(1)	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1 ⁽¹⁾	TRISC0 ⁽¹⁾	133

TABLE 25-1: SUMMARY OF REGISTERS ASSOCIATED WITH SPI OPERATION

Legend: — Unimplemented location, read as '0'. Shaded cells are not used by the MSSP1 in SPI mode.

* Page provides register information.

Note 1: PIC16(L)F1829 only.

2: PIC16(L)F1825 only.

FIGURE 26-2: EUSART RECEIVE BLOCK DIAGRAM



The operation of the EUSART module is controlled through three registers:

- Transmit Status and Control (TXSTA)
- Receive Status and Control (RCSTA)
- Baud Rate Control (BAUDCON)

These registers are detailed in Register 26-1, Register 26-2 and Register 26-3, respectively.

When the receiver or transmitter section is not enabled then the corresponding RX or TX pin may be used for general purpose input and output.

					SYNC	C = 0, BRGH	l = 1, BRC	G16 = 0				
BAUD	Fos	c = 8.000	0 MHz	Fos	Fosc = 4.000 MHz			= 3.686	4 MHz	Fosc = 1.000 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	_		_	_	_	_	_	_	300	0.16	207
1200	_	_	_	1202	0.16	207	1200	0.00	191	1202	0.16	51
2400	2404	0.16	207	2404	0.16	103	2400	0.00	95	2404	0.16	25
9600	9615	0.16	51	9615	0.16	25	9600	0.00	23	—	—	_
10417	10417	0.00	47	10417	0.00	23	10473	0.53	21	10417	0.00	5
19.2k	19231	0.16	25	19.23k	0.16	12	19.2k	0.00	11	—	—	_
57.6k	55556	-3.55	8	—	—	—	57.60k	0.00	3	—	—	_
115.2k	—	_		—	—		115.2k	0.00	1	—	—	

TABLE 26-5: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

	SYNC = 0, BRGH = 0, BRG16 = 1											
BAUD	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Foso	c = 18.43	2 MHz	Fosc = 11.0592 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	6666	300.0	-0.01	4166	300.0	0.00	3839	300.0	0.00	2303
1200	1200	-0.02	3332	1200	-0.03	1041	1200	0.00	959	1200	0.00	575
2400	2401	-0.04	832	2399	-0.03	520	2400	0.00	479	2400	0.00	287
9600	9615	0.16	207	9615	0.16	129	9600	0.00	119	9600	0.00	71
10417	10417	0.00	191	10417	0.00	119	10378	-0.37	110	10473	0.53	65
19.2k	19.23k	0.16	103	19.23k	0.16	64	19.20k	0.00	59	19.20k	0.00	35
57.6k	57.14k	-0.79	34	56.818	-1.36	21	57.60k	0.00	19	57.60k	0.00	11
115.2k	117.6k	2.12	16	113.636	-1.36	10	115.2k	0.00	9	115.2k	0.00	5

	SYNC = 0, BRGH = 0, BRG16 = 1											
BAUD	Fos	c = 8.000	0 MHz	Fos	Fosc = 4.000 MHz		Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	299.9	-0.02	1666	300.1	0.04	832	300.0	0.00	767	300.5	0.16	207
1200	1199	-0.08	416	1202	0.16	207	1200	0.00	191	1202	0.16	51
2400	2404	0.16	207	2404	0.16	103	2400	0.00	95	2404	0.16	25
9600	9615	0.16	51	9615	0.16	25	9600	0.00	23	_	_	_
10417	10417	0.00	47	10417	0.00	23	10473	0.53	21	10417	0.00	5
19.2k	19.23k	0.16	25	19.23k	0.16	12	19.20k	0.00	11	_	_	_
57.6k	55556	-3.55	8	—	_	_	57.60k	0.00	3	—	_	_
115.2k		_	_	—	_	_	115.2k	0.00	1	_	_	_

ΜΟνιω	Move INDFn to W
Syntax:	[<i>label</i>] MOVIW ++FSRn [<i>label</i>] MOVIWFSRn [<i>label</i>] MOVIW FSRn++ [<i>label</i>] MOVIW FSRn [<i>label</i>] MOVIW k[FSRn]
Operands:	n ∈ [0,1] mm ∈ [00,01, 10, 11] -32 ≤ k ≤ 31
Operation:	$\begin{split} &\text{INDFn} \rightarrow \text{W} \\ &\text{Effective address is determined by} \\ &\text{FSR + 1 (preincrement)} \\ &\text{FSR - 1 (predecrement)} \\ &\text{FSR + k (relative offset)} \\ &\text{After the Move, the FSR value will be either:} \\ &\text{FSR + 1 (all increments)} \\ &\text{FSR - 1 (all decrements)} \\ &\text{Unchanged} \end{split}$
Status Affected:	Z

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn	11

Description:

This instruction is used to move data between W and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

Note: The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h -FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap-around.

Syntax:	[<i>label</i>] MOVLB k
Operands:	$0 \leq k \leq 15$
Operation:	$k \rightarrow BSR$
Status Affected:	None
Description:	The 5-bit literal 'k' is loaded into the Bank Select Register (BSR).

MOVLP	Move literal to PCLATH				
Syntax:	[<i>label</i>]MOVLP k				
Operands:	$0 \le k \le 127$				
Operation:	$k \rightarrow PCLATH$				
Status Affected:	None				
Description:	The 7-bit literal 'k' is loaded into the PCLATH register.				
MOVLW	Move literal to W				
Syntax:	[<i>label</i>] MOVLW k				
Operands:	$0 \leq k \leq 255$				
Operation:	$k \rightarrow (W)$				
Status Affected:	None				
Description:	The 8-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.				
Words:	1				
Cycles:	1				
Example:	MOVLW 0x5A				
	After Instruction W = 0x5A				
MOVWF	Move W to f				
Syntax:	[<i>label</i>] MOVWF f				
Operands:	$0 \leq f \leq 127$				
Operation:	$(W) \rightarrow (f)$				
Status Affected:	None				
Description:	Move data from W register to register 'f'.				
Words:	1				
Cycles:	1				
<u>Example:</u>	MOVWF OPTION_REG				
	Before Instruction OPTION_REG = 0xFF				

W = 0x4F After Instruction OPTION_REG = 0x4F W = 0x4F



FIGURE 30-4: POR AND POR REARM WITH SLOW RISING VDD



FIGURE 31-13: IDD, MFINTOSC MODE (Fosc = 500 kHz), PIC16LF1825/9 ONLY



FIGURE 31-14: IDD, MFINTOSC MODE (Fosc = 500 kHz), PIC16F1825/9 ONLY









32.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers (MCU) and dsPIC[®] digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
- MPLAB[®] X IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB XC Compiler
 - MPASM[™] Assembler
 - MPLINK[™] Object Linker/ MPLIB[™] Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- · Simulators
 - MPLAB X SIM Software Simulator
- · Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
 - MPLAB ICD 3
 - PICkit™ 3
- Device Programmers
- MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

32.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows[®], Linux and Mac $OS^{®}$ X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- · Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- · Call graph window
- Project-Based Workspaces:
- Multiple projects
- Multiple tools
- · Multiple configurations
- · Simultaneous debugging sessions

File History and Bug Tracking:

- · Local file history feature
- Built-in support for Bugzilla issue tracker

16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
Dim	Dimension Limits		NOM	MAX	
Number of Pins	N	16			
Pitch	е	0.65 BSC			
Overall Height	А	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3	0.20 REF			
Overall Width	E	4.00 BSC			
Exposed Pad Width	E2	2.50	2.65	2.80	
Overall Length	D	4.00 BSC			
Exposed Pad Length	D2	2.50	2.65	2.80	
Contact Width	b	0.25	0.30	0.35	
Contact Length	L	0.30	0.40	0.50	
Contact-to-Exposed Pad	K	0.20	-	-	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B





Microchip Technology Drawing C04-255A Sheet 1 of 2