Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1825-e-ml

TABLE 3-8: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Banks 9-30											
x00h/ x80h[1]	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
x00h/ x81h[1]	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx
x02h/ x82h[1]	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
x03h/ x83h[1]	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
x04h/ x84h[1]	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
x05h/ x85h[1]	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
x06h/ x86h[1]	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
x07h/ x87h[1]	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
x08h/ x88h[1]	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000
x09h/ x89h[1]	WREG	Working Register								0000 0000	uuuu uuuu
x0Ah/ x8Ah[1]	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
x0Bh/ x8Bh[1]	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000
x0Ch/ x8Ch — x1Fh/ x9Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved.
Shaded locations are unimplemented, read as '0'.

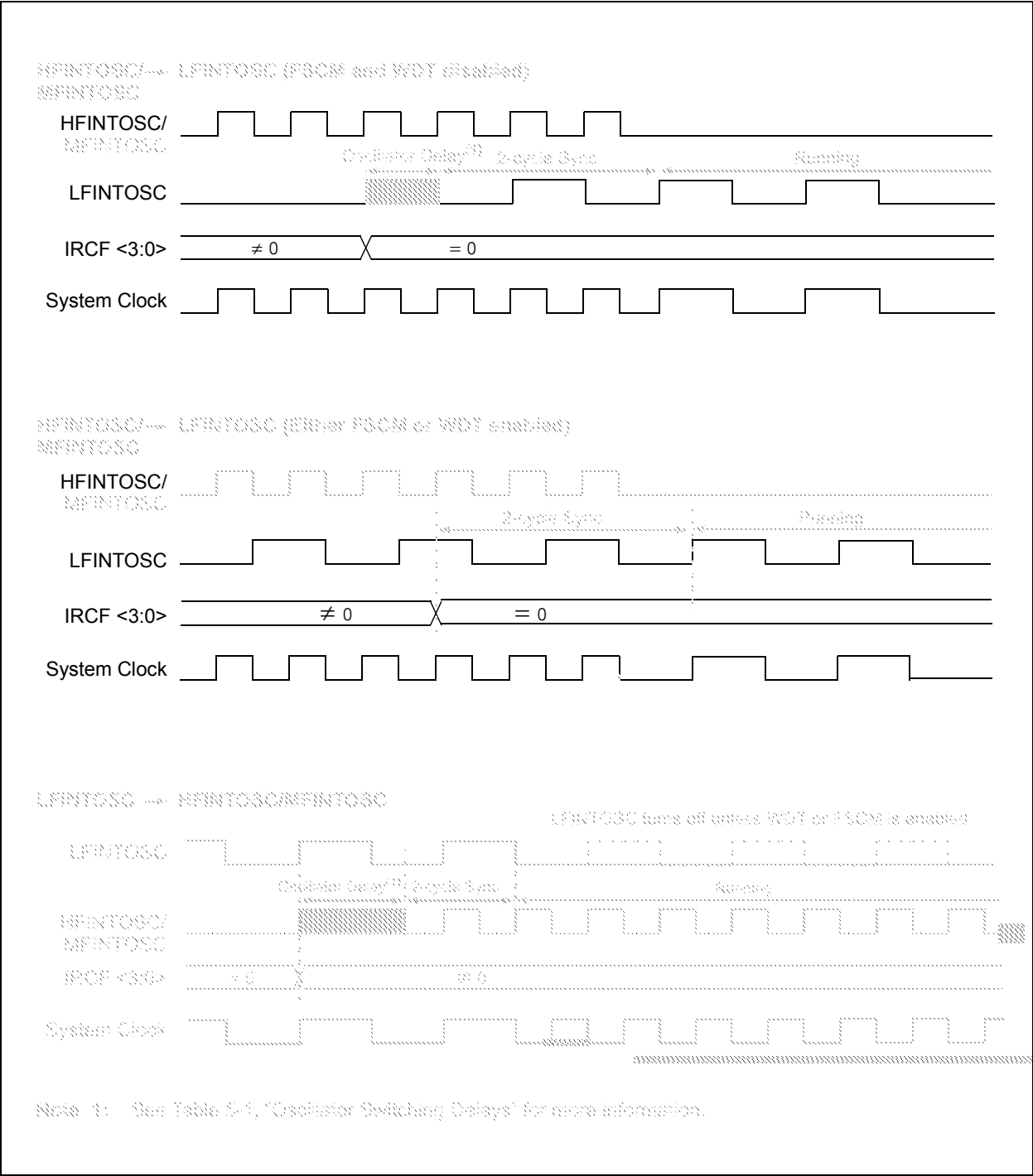**Note** 1: These registers can be addressed from any bank.
2: PIC16(L)F1829 only.
3: PIC16(L)F1825 only.
4: Unimplemented, read as '1'.

PIC16(L)F1825/9

FIGURE 5-7: **INTERNAL OSCILLATOR SWITCH TIMING**

11.2   Using the Data EEPROM

The data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). When variables in one section change frequently, while variables in another section do not change, it is possible to exceed the total number of write cycles to the EEPROM without exceeding the total number of write cycles to a single byte. Refer to **Section 30.0 "Electrical Specifications"**. If this is the case, then a refresh of the array must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in Flash program memory.

11.2.1   READING THE DATA EEPROM MEMORY

To read a data memory location, the user must write the address to the EEADRL register, clear the EEPGD and CFGS control bits of the EECON1 register, and then set control bit RD. The data is available at the very next cycle, in the EEDATL register; therefore, it can be read in the next instruction. EEDATL will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 11-1:   DATA EEPROM READ

```
BANKSEL EEADRL        ;
MOVLW   DATA_EE_ADDR ;
MOVWF   EEADRL        ;Data Memory
                      ;Address to read
BCF     EECON1, CFGS ;Deselect Config space
BCF     EECON1, EEPGD;Point to DATA memory
BSF     EECON1, RD   ;EE Read
MOVF    EEDATL, W    ;W = EEDATL
```

Note: Data EEPROM can be read regardless of the setting of the CPD bit.

11.2.2   WRITING TO THE DATA EEPROM MEMORY

To write an EEPROM data location, the user must first write the address to the EEADRL register and the data to the EEDATL register. Then the user must follow a specific sequence to initiate the write for each byte.

The write will not initiate if the above sequence is not followed exactly (write 55h to EECON2, write AAh to EECON2, then set the WR bit) for each byte. Interrupts should be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. EEIF must be cleared by software.

11.2.3   PROTECTION AGAINST SPURIOUS WRITE

There are conditions when the user may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built-in. On power-up, WREN is cleared. Also, the Power-up Timer (64 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during:

• Brown-out
• Power glitch
• Software malfunction

11.2.4   DATA EEPROM OPERATION DURING CODE-PROTECT

Data memory can be code-protected by programming the CPD bit in the Configuration Word 1 (Register 5-1) to '0'.

When the data memory is code-protected, only the CPU is able to read and write data to the data EEPROM. It is recommended to code-protect the program memory when code-protecting data memory. This prevents anyone from replacing your program with a program that will access the contents of the data EEPROM.

REGISTER 13-2: IOCAN: INTERRUPT-ON-CHANGE PORTA NEGATIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6   **Unimplemented:** Read as '0'

bit 5-0   **IOCAN<5:0>:** Interrupt-on-Change PORTA Negative Edge Enable bits
        1 = Interrupt-on-change enabled on the pin for a negative going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
        0 = Interrupt-on-change disabled for the associated pin.

REGISTER 13-3: IOCAF: INTERRUPT-ON-CHANGE PORTA FLAG REGISTER

U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-6   **Unimplemented:** Read as '0'

bit 5-0   **IOCAF<5:0>:** Interrupt-on-Change PORTA Flag bits
        1 = An enabled change was detected on the associated pin.
            Set when IOCAPx = 1 and a rising edge was detected on RAx, or when IOCANx = 1 and a falling edge was detected on RAx.
        0 = No change was detected, or the user cleared the detected change.

REGISTER 13-4: IOCBP: INTERRUPT-ON-CHANGE PORTB POSITIVE EDGE REGISTER
                    (PIC16(L)F1829 ONLY)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
IOCBP7	IOCBP6	IOCBP5	IOCBP4	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4   **IOCBP<7:4>:** Interrupt-on-Change PORTB Positive Edge Enable bits
        1 = Interrupt-on-change enabled on the pin for a positive going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.
        0 = Interrupt-on-change disabled for the associated pin.

bit 3-0   **Unimplemented:** Read as '0'

PIC16(L)F1825/9

18.0   SR LATCH

The module consists of a single SR latch with multiple Set and Reset inputs as well as separate latch outputs. The SR latch module includes the following features:

- Programmable input selection
- SR latch output is available externally
- Separate Q and $\overline{Q}$ outputs
- Firmware Set and Reset

The SR latch can be used in a variety of analog applications, including oscillator circuits, one-shot circuit, hysteretic controllers, and analog timing applications.

18.1   Latch Operation

The latch is a Set-Reset Latch that does not depend on a clock source. Each of the Set and Reset inputs are active-high. The latch can be Set or Reset by:

- Software control (SRPS and SRPR bits)
- Comparator C1 output (sync_C1OUT)
- Comparator C2 output (sync_C2OUT) (PIC16(L)F1829 only)
- SRI pin
- Programmable clock (SRCLK)

The SRPS and the SRPR bits of the SRCON0 register may be used to Set or Reset the SR latch, respectively. The latch is Reset-dominant. Therefore, if both Set and Reset inputs are high, the latch will go to the Reset state. Both the SRPS and SRPR bits are self resetting which means that a single write to either of the bits is all that is necessary to complete a latch Set or Reset operation.

The output from Comparator C1 or C2 can be used as the Set or Reset inputs of the SR latch. The output of either Comparator can be synchronized to the Timer1 clock source. See **Section 19.0 "Comparator Module"** and **Section 21.0 "Timer1 Module with Gate Control"** for more information.

An external source on the SRI pin can be used as the Set or Reset inputs of the SR latch.

An internal clock source is available that can periodically Set or Reset the SR latch. The SRCLK<2:0> bits in the SRCON0 register are used to select the clock source period. The SRSCKE and SRRCKE bits of the SRCON1 register enable the clock source to Set or Reset the SR latch, respectively.

18.2   Latch Output

The SRQEN and SRNQEN bits of the SRCON0 register control the Q and $\overline{Q}$ latch outputs. Both of the SR latch outputs may be directly output to an I/O pin at the same time.

The applicable TRIS bit of the corresponding port must be cleared to enable the port pin output driver.

18.3   Effects of a Reset

Upon any device Reset, the SR latch output is not initialized to a known state. The user's firmware is responsible for initializing the latch output before enabling the output pins.

PIC16(L)F1825/9

23.5 Carrier Source Polarity Select

The signal provided from any selected input source for the carrier high and carrier low signals can be inverted. Inverting the signal for the carrier high source is enabled by setting the MDCHPOL bit of the MDCARH register. Inverting the signal for the carrier low source is enabled by setting the MDCLPOL bit of the MDCARL register.

23.6 Carrier Source Pin Disable

Some peripherals assert control over their corresponding output pin when they are enabled. For example, when the CCP1 module is enabled, the output of CCP1 is connected to the CCP1 pin.

This default connection to a pin can be disabled by setting the MDCHODIS bit in the MDCARH register for the carrier high source and the MDCLODIS bit in the MDCARL register for the carrier low source.

23.7 Programmable Modulator Data

The MDBIT of the MDCON register can be selected as the source for the modulator signal. This gives the user the ability to program the value used for modulation.

23.8 Modulator Source Pin Disable

The modulator source default connection to a pin can be disabled by setting the MDMSODIS bit in the MDSRC register.

23.9 Modulated Output Polarity

The modulated output signal provided on the MDOUT pin can also be inverted. Inverting the modulated output signal is enabled by setting the MDOPOL bit of the MDCON register.

23.10 Slew Rate Control

The slew rate limitation on the output port pin can be disabled. The slew rate limitation can be removed by clearing the MDSLR bit in the MDCON register.

23.11 Operation in Sleep Mode

The DSM module is not affected by Sleep mode. The DSM can still operate during Sleep, if the Carrier and Modulator input sources are also still operable during Sleep.

23.12 Effects of a Reset

Upon any device Reset, the DSM module is disabled. The user's firmware is responsible for initializing the module before enabling the output. The registers are reset to their default values.

TABLE 24-10: SUMMARY OF REGISTERS ASSOCIATED WITH ENHANCED PWM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON1	—	—	SDO2SEL[2]	SS2SEL[2]	P1DSEL	P1CSEL	P2BSEL	CCP2SEL	119
CCP1CON	P1M<1:0>[1]		DC1B<1:0>		CCP1M<3:0>				224
CCP2CON	P2M<1:0>[1]		DC2B<1:0>		CCP2M<3:0>				224
CCP3CON	—	—	DC3B<1:0>		CCP3M<3:0>				224
CCP4CON	—	—	DC4B<1:0>		CCP4M<3:0>				224
CCP1AS	CCP1ASE	CCP1AS<2:0>			PSS1AC<1:0>		PSS1BD<1:0>		226
CCP2AS	CCP2ASE	CCP2AS<2:0>			PSS2AC<1:0>		PSS2BD<1:0>		226
CCPTMRS	C4TSEL<1:0>		C3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		225
INLVLA	—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	124
INLVLC	INLVLC7[1]	INLVLC6[1]	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	135
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	87
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	88
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	—	—	CCP2IE	89
PIE3	—	—	CCP4IE	CCP3IE	TMR6IE	—	TMR4IE	—	90
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	92
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	—	CCP2IF	93
PIR3	—	—	CCP4IF	CCP3IF	TMR6IF	—	TMR4IF	—	94
PRx	Timer2/4/6 Period Register								188*
PSTR1CON	—	—	—	STR1SYNC	STR1D	STR1C	STR1B	STR1A	228
PSTR2CON	—	—	—	STR2SYNC	STR2D	STR2C	STR2B	STR2A	228
PWM1CON	P1RSEN	P1DC<6:0>							227
PWM2CON	P2RSEN	P2DC<6:0>							227
T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		190
T4CON	—	T4OUTPS<3:0>				TMR4ON	T4CKPS<1:0>		190
T6CON	—	T6OUTPS<3:0>				TMR6ON	T6CKPS<1:0>		190
TMRx	Timer2/4/6 Module Register								188*
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	122
TRISC	TRISC7[2]	TRISC6[2]	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	133

Legend: — Unimplemented location, read as '0'. Shaded cells are not used by the PWM.

* Page provides register information.

Note 1: Applies to ECCP modules only.
2: PIC16(L)F1829 only.

25.2.4 SPI SLAVE MODE

In Slave mode, the data is transmitted and received as external clock pulses appear on SCKx. When the last bit is latched, the SSPxIF interrupt flag bit is set.

Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCKx pin. The Idle state is determined by the CKP bit of the SSPxCON1 register.

While in Slave mode, the external clock is supplied by the external clock source on the SCKx pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. The shift register is clocked from the SCKx pin input and when a byte is received, the device will generate an interrupt. If enabled, the device will wake-up from Sleep.

25.2.4.1 Daisy-Chain Configuration

The SPI bus can sometimes be connected in a daisy-chain configuration. The first slave output is connected to the second slave input, the second slave output is connected to the third slave input, and so on. The final slave output is connected to the master input. Each slave sends out, during a second group of clock pulses, an exact copy of what was received during the first group of clock pulses. The whole chain acts as one large communication shift register. The daisy-chain feature only requires a single Slave Select line from the master device.

Figure 25-7 shows the block diagram of a typical daisy-chain connection when operating in SPI mode.

In a daisy-chain configuration, only the most recent byte on the bus is required by the slave. Setting the BOEN bit of the SSPxCON3 register will enable writes to the SSPxBUF register, even if the previous byte has not been read. This allows the software to ignore data that may not apply to it.

25.2.5 SLAVE SELECT SYNCHRONIZATION

The Slave Select can also be used to synchronize communication. The Slave Select line is held high until the master device is ready to communicate. When the Slave Select line is pulled low, the slave knows that a new transmission is starting.

If the slave fails to receive the communication properly, it will be reset at the end of the transmission, when the Slave Select line returns to a high state. The slave is then ready to receive a new transmission when the Slave Select line is pulled low again. If the Slave Select line is not used, there is a risk that the slave will eventually become out of sync with the master. If the slave misses a bit, it will always be one bit off in future transmissions. Use of the Slave Select line allows the slave and master to align themselves at the beginning of each transmission.

The $\overline{SSx}$ pin allows a Synchronous Slave mode. The SPI must be in Slave mode with $\overline{SSx}$ pin control enabled (SSPxCON1<3:0> = 0100).

When the $\overline{SSx}$ pin is low, transmission and reception are enabled and the SDOx pin is driven.

When the $\overline{SSx}$ pin goes high, the SDOx pin is no longer driven, even if in the middle of a transmitted byte and becomes a floating output. External pull-up/pull-down resistors may be desirable depending on the application.

Note 1: When the SPI is in Slave mode with $\overline{SSx}$ pin control enabled (SSPxCON1<3:0> = 0100), the SPI module will reset if the $\overline{SSx}$ pin is set to V_{DD}.

2: When the SPI is used in Slave mode with CKE set; the user must enable $\overline{SSx}$ pin control.

3: While operated in SPI Slave mode the SMP bit of the SSPxSTAT register must remain clear.

When the SPI module resets, the bit counter is forced to '0'. This can be done by either forcing the $\overline{SSx}$ pin to a high level or clearing the SSPEN bit.

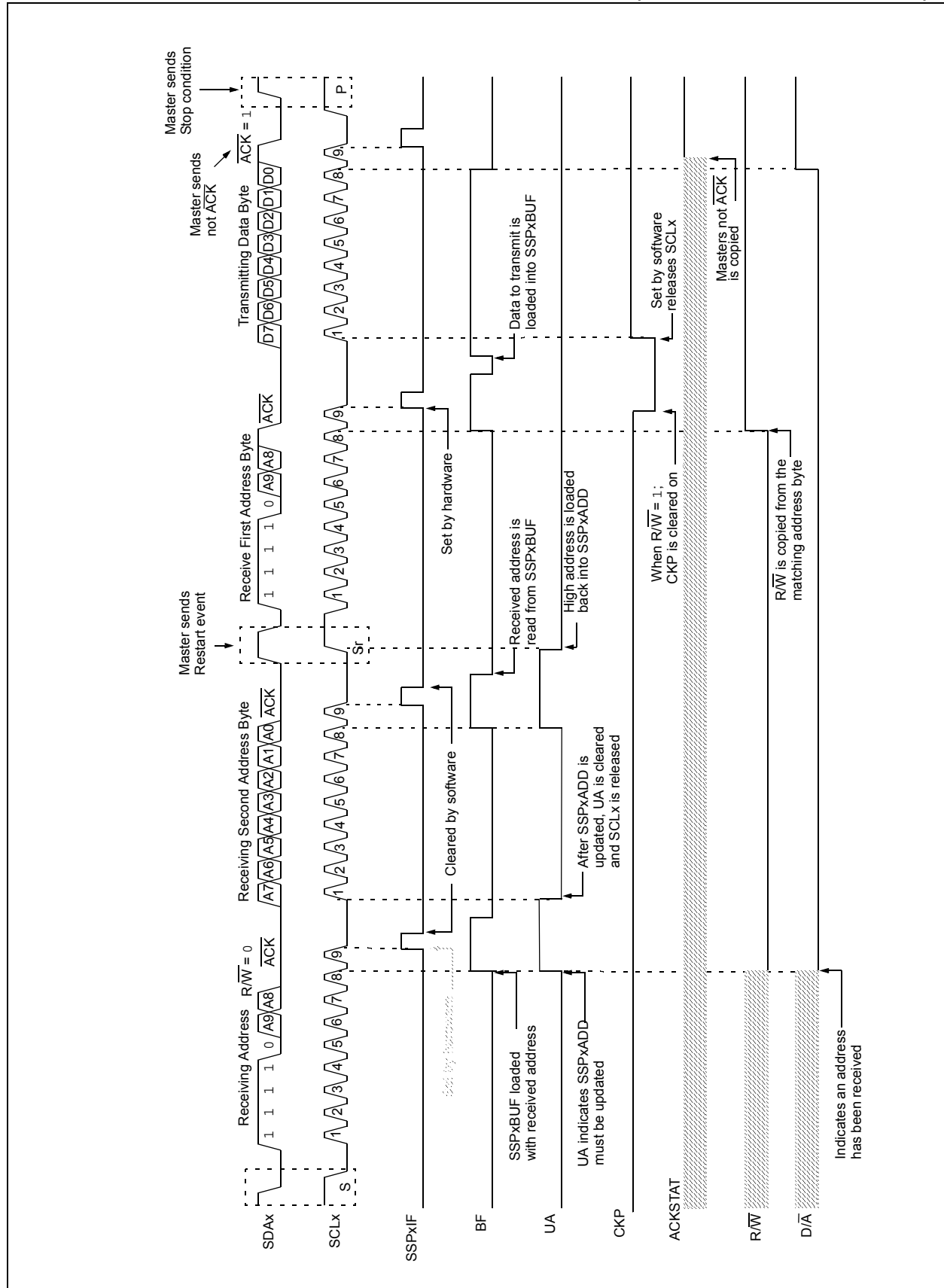**FIGURE 25-22:** **I²C SLAVE, 10-BIT ADDRESS, TRANSMISSION (SEN = 0, AHEN = 0, DHEN = 0)**

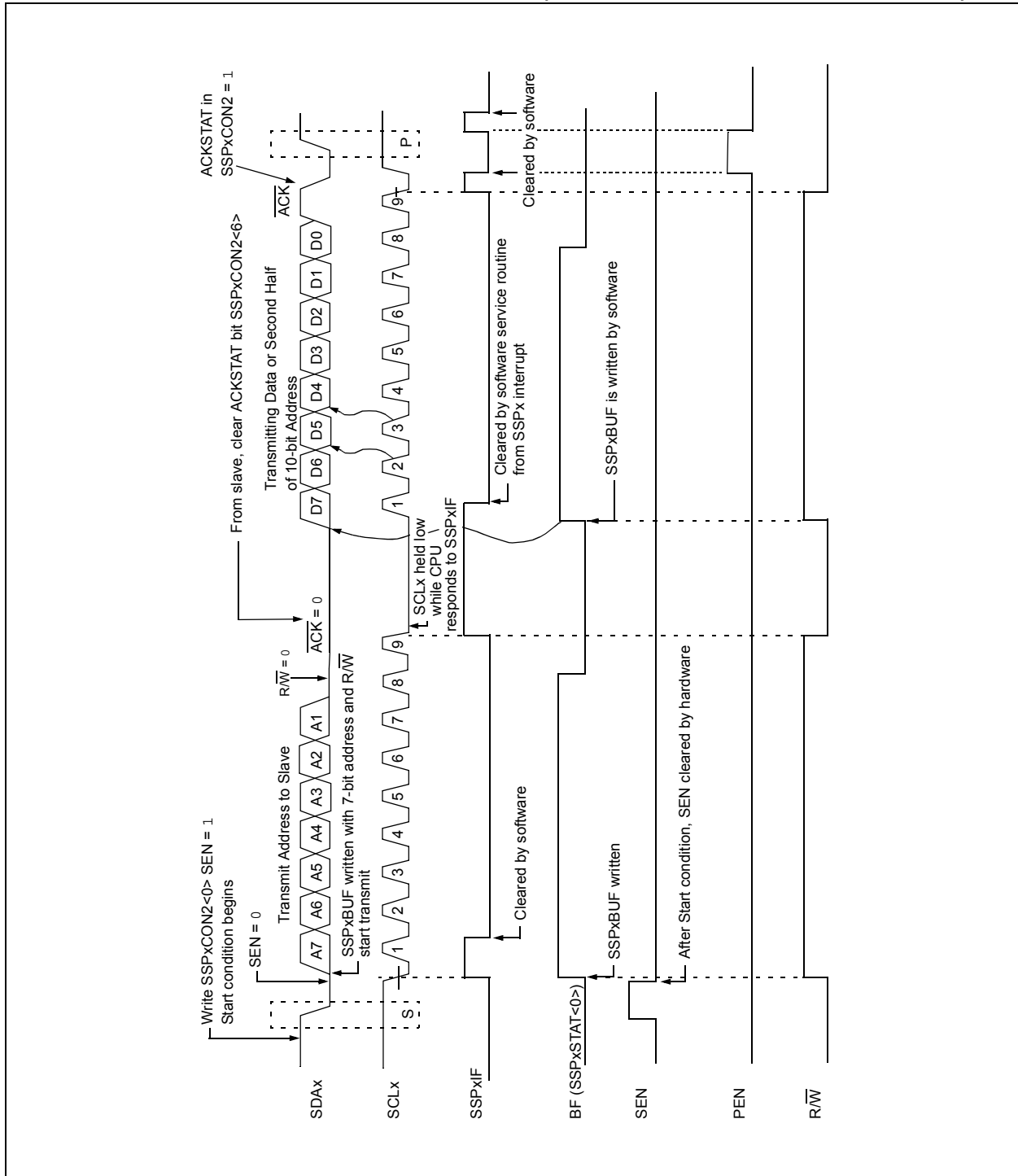**FIGURE 25-28:** **I²C MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)**

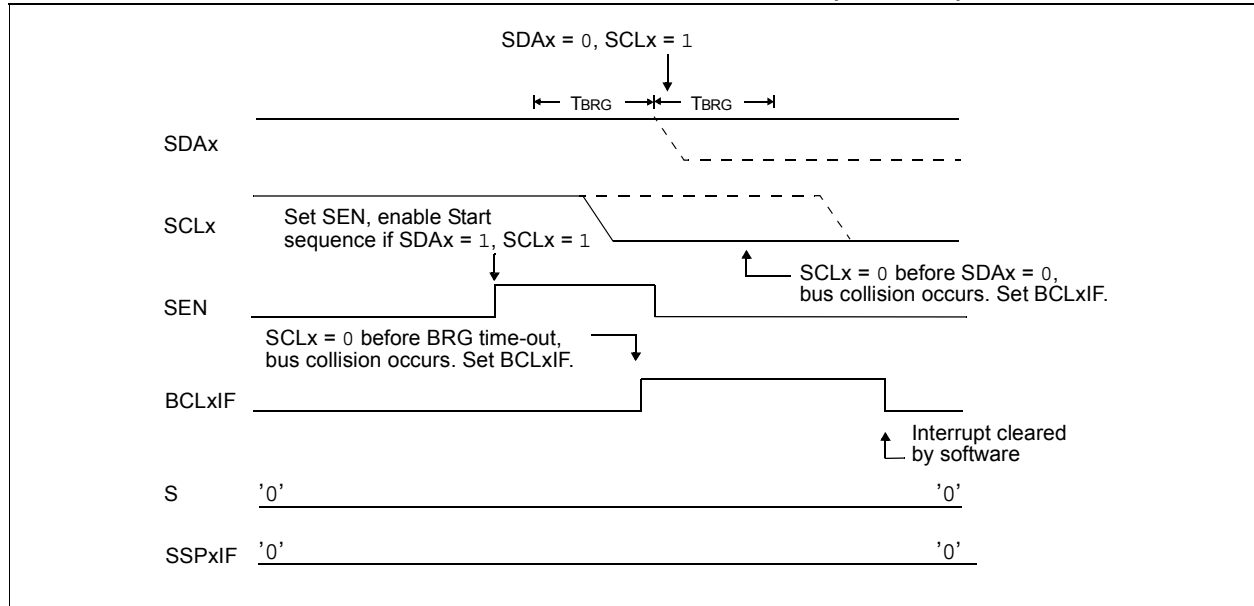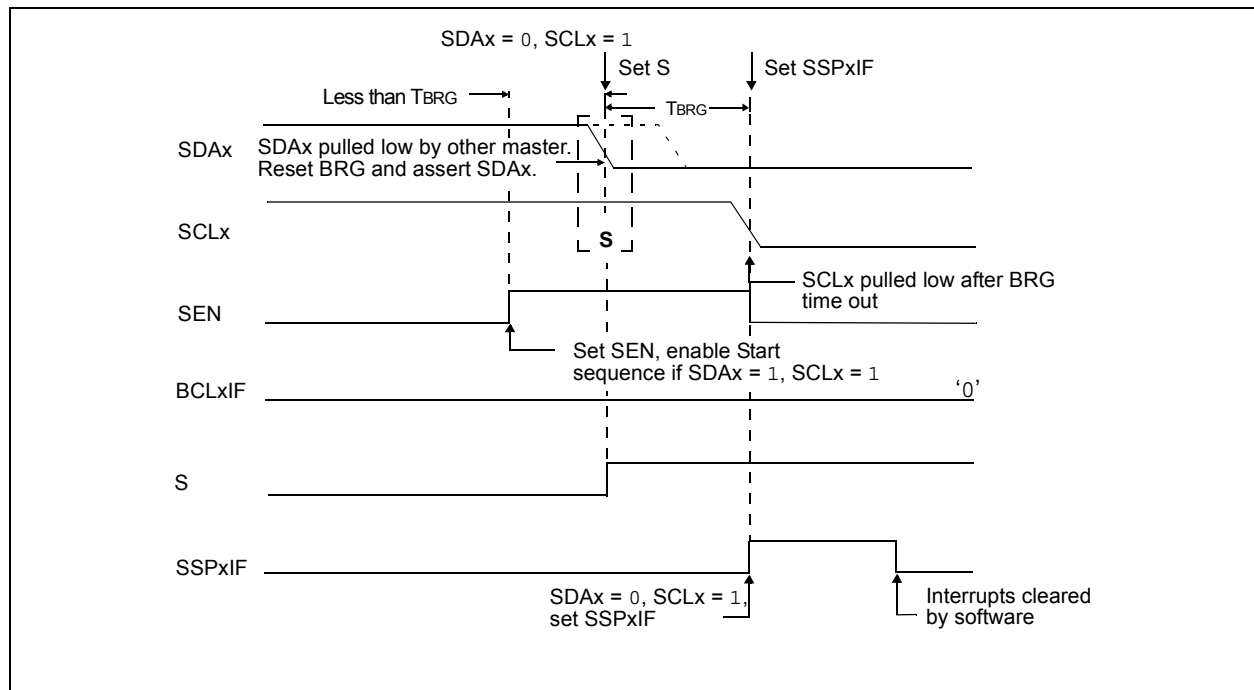**FIGURE 25-34:** **BUS COLLISION DURING START CONDITION (SCLX = 0)**

FIGURE 25-35: **BRG RESET DUE TO SDA ARBITRATION DURING START CONDITION**

REGISTER 25-2: SSPxCON1: SSPx CONTROL REGISTER 1

R/C/HS-0/0	R/C/HS-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Bit is set by hardware C = User cleared

bit 7
WCOL: Write Collision Detect bit
Master mode:
1 = A write to the SSPxBUF register was attempted while the I^{2}C conditions were not valid for a transmission to be started
0 = No collision
Slave mode:
1 = The SSPxBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

bit 6
SSPOV: Receive Overflow Indicator bit[1]
In SPI mode:
1 = A new byte is received while the SSPxBUF register is still holding the previous data. In case of overflow, the data in SSPxSR is lost. Overflow can only occur in Slave mode. In Slave mode, the user must read the SSPxBUF, even if only transmitting data, to avoid setting overflow. In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPxBUF register (must be cleared in software).
0 = No overflow
In I^{2}C mode:
1 = A byte is received while the SSPxBUF register is still holding the previous byte. SSPOV is a "don't care" in Transmit mode (must be cleared in software).
0 = No overflow

bit 5
SSPEN: Synchronous Serial Port Enable bit
In both modes, when enabled, these pins must be properly configured as input or output
In SPI mode:
1 = Enables serial port and configures SCKx, SDOx, SDIx and $\overline{SSx}$ as the source of the serial port pins[2]
0 = Disables serial port and configures these pins as I/O port pins
In I^{2}C mode:
1 = Enables the serial port and configures the SDAx and SCLx pins as the source of the serial port pins[3]
0 = Disables serial port and configures these pins as I/O port pins

bit 4
CKP: Clock Polarity Select bit
In SPI mode:
1 = Idle state for clock is a high level
0 = Idle state for clock is a low level
In I^{2}C Slave mode:
SCLx release control
1 = Enable clock
0 = Holds clock low (clock stretch). (Used to ensure data setup time.)
In I^{2}C Master mode:
Unused in this mode

bit 3-0
SSPM<3:0>: Synchronous Serial Port Mode Select bits
0000 = SPI Master mode, clock = F$_{OSC}$/4
0001 = SPI Master mode, clock = F$_{OSC}$/16
0010 = SPI Master mode, clock = F$_{OSC}$/64
0011 = SPI Master mode, clock = TMR2 output/2
0100 = SPI Slave mode, clock = SCKx pin, $\overline{SSx}$ pin control enabled
0101 = SPI Slave mode, clock = SCKx pin, $\overline{SSx}$ pin control disabled, $\overline{SSx}$ can be used as I/O pin
0110 = I^{2}C Slave mode, 7-bit address
0111 = I^{2}C Slave mode, 10-bit address
1000 = I^{2}C Master mode, clock = F$_{OSC}$ / (4 * (SSPxADD+1))[4]
1001 = Reserved
1010 = SPI Master mode, clock = F$_{OSC}$/(4 * (SSPxADD+1))[5]
1011 = I^{2}C firmware controlled Master mode (Slave Idle)
1100 = Reserved
1101 = Reserved
1110 = I^{2}C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
1111 = I^{2}C Slave mode, 10-bit address with Start and Stop bit interrupts enabled

Note 1: In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPxBUF register.
2: When enabled, these pins must be properly configured as input or output.
3: When enabled, the SDAx and SCLx pins must be configured as inputs.
4: SSPxADD values of 0, 1 or 2 are not supported for I^{2}C Mode.
5: SSPxADD value of '0' is not supported. Use SSPM = 0000 instead.

30.2   DC Characteristics: PIC16(L)F1825/9-I/E (Industrial, Extended) (Continued)

PIC16LF1825/9	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
PIC16F1825/9	**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					

Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						V_{DD}	Note
Supply Current (IDD)[1,2]							
D020		—	2.7	3.6	mA	3.0	F_{OSC} = 32 MHz
		—	3.2	4.2	mA	3.6	HS Oscillator mode **(Note 4)**
D020		—	2.7	4.0	mA	3.0	F_{OSC} = 32 MHz
		—	3.2	4.3	mA	5.0	HS Oscillator mode **(Note 4)**
D021		—	222	350	μA	1.8	F_{OSC} = 4 MHz
		—	400	690	μA	3.0	EXTRC mode **(Note 5)**
D021		—	240	500	μA	1.8	F_{OSC} = 4 MHz
		—	416	800	μA	3.0	EXTRC mode **(Note 5)**
		—	497	900	μA	5.0	

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note   1:   The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2:   The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3:   8 MHz internal RC oscillator with 4xPLL enabled.

4:   8 MHz crystal oscillator with 4xPLL enabled.

5:   For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ..

30.9 High Temperature Operation

This section outlines the specifications for the following devices operating in the high temperature range between -40°C and 150°C.[1]

- PIC16F1825[4]
- PIC16F1829[4]

When the value of any parameter is identical for both the 125°C Extended and the 150°C High Temp. temperature ranges, then that value will be found in the standard specification tables shown earlier in this chapter, under the fields listed for the 125°C Extended temperature range. If the value of any parameter is unique to the 150°C High Temp. temperature range, then it will be listed here, in this section of the data sheet.

If a Silicon Errata exists for the product and it lists a modification to the 125°C Extended temperature range value, one that is also shared at the 150°C High Temp. temperature range, then that modified value will apply to both temperature ranges.

Note 1: AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

2: Writes are **not allowed** for Flash program memory above 125°C.

3: The temperature range indicator in the catalog part number and device marking is "H" for -40°C to 150°C.

Example: PIC16F1825T-H/SL indicates the device is shipped in a Tape and Reel configuration, in the SOIC package, and is rated for operation from -40°C to 150°C.

4: The low voltage versions of these devices, PIC16LF1825 and PIC16LF1829, are not released for operation above +125°C.

5: Errata Sheet DS80517 lists various mask revisions. 150°C operation applies only to revisions A4 and later.

6: The Capacitive Sensing module (CPS) should not be used in high temperature devices. Function and its parametrics are not warranted.

7: Only SOIC (SL), TSSOP (ST), SSOP (SS) and QFN (ML) packages will be offered, not PDIP or UQFN.

TABLE 30-18: ABSOLUTE MAXIMUM RATINGS

Parameter	Condition	Value
Max. Current: V_{DD}	Source	15 mA
Max. Current: V_{SS}	Sink	15 mA
Max. Current: Pin	Source	5 mA
Max. Current: Pin	Sink	5 mA
Max. Storage Temperature	—	-65°C to 155°C
Max. Junction Temperature	—	+155°C
Ambient Temperature under Bias	—	-40°C to +150°C

Note: Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

TABLE 30-19: **DC CHARACTERISTICS FOR PIC16F1825/9-H (High Temp.)**

PIC16F1825/9							Standard Operating Conditions: (unless otherwise stated) Operating Temperature: -40°C $\leq$ TA $\leq$ +150°C for High Temperature
Param No.	Sym.	Characteristics	Min.	Typ.	Max.	Units	Condition
D001	VDD	Supply Voltage	2.5	—	5.5	V	FOSC $\leq$ 32 MHz **(Note 2)**
D002*	VDR	RAM Data Retention Voltage[1]	2.1	—	5.5	V	Device in Sleep mode
D003	VADFVR	Fixed Voltage Reference Voltage for ADC	-10	—	8	%	1.024V, VDD $\geq$ 2.5V 2.048V, VDD $\geq$ 2.5V 4.096V, VDD $\geq$ 4.75V
D003A	VCDAFVR	Fixed Voltage Reference Voltage for ADC	-13	—	9	%	1.024V, VDD $\geq$ 2.5V 2.048V, VDD $\geq$ 2.5V 4.096V, VDD $\geq$ 4.75V

    * These parameters are characterized but not tested.

    † Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

  Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

      2: PLL required for 32 MHz operation.

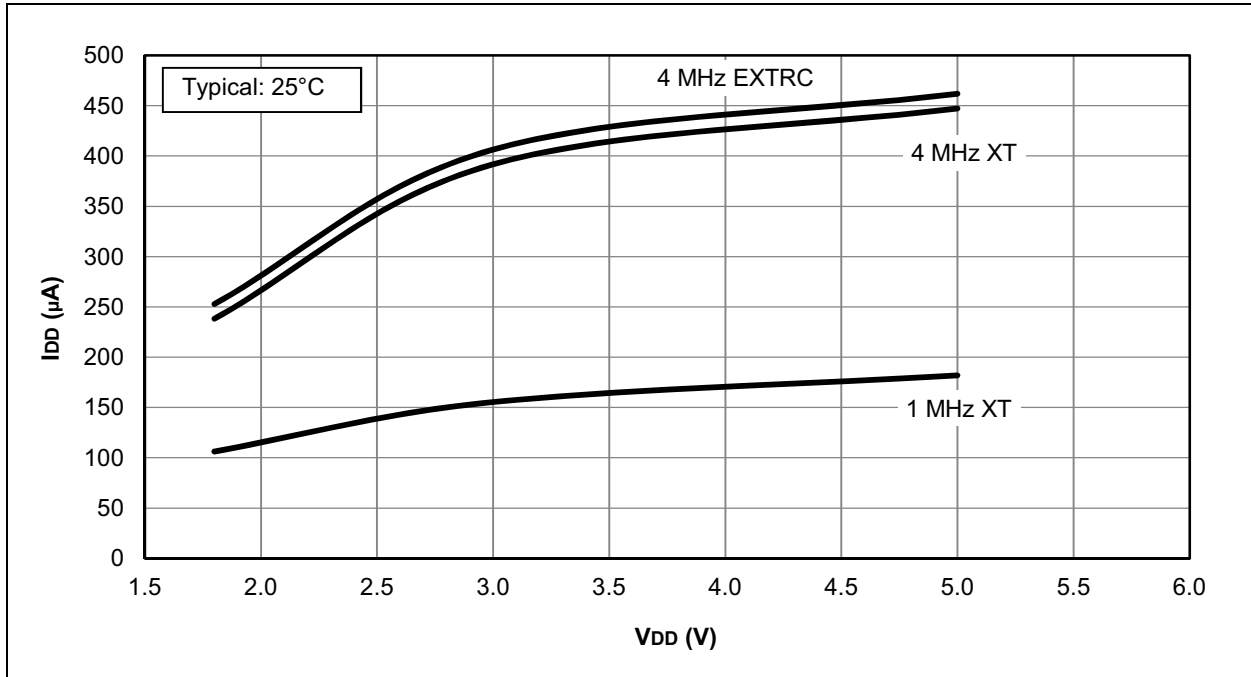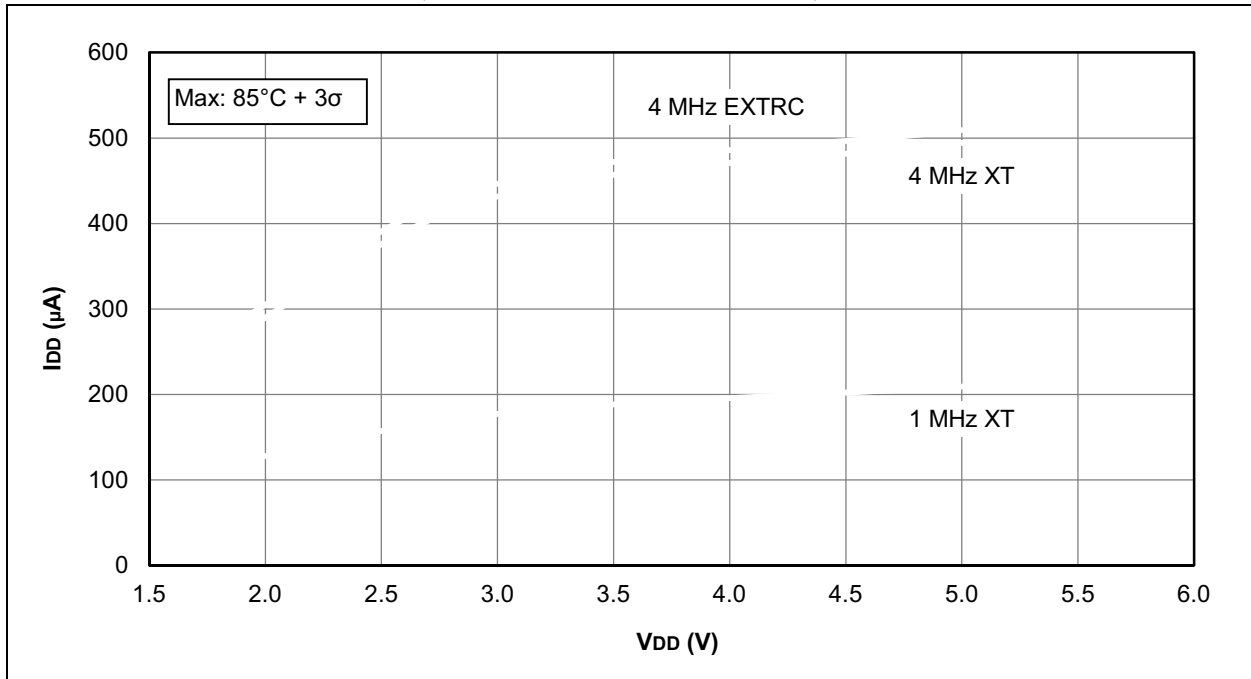**FIGURE 31-5:** I_DD **TYPICAL, XT AND EXTRC OSCILLATOR, PIC16F1825/9 ONLY**

FIGURE 31-6: I_DD **MAXIMUM, XT AND EXTRC OSCILLATOR, PIC16F1825/9 ONLY**

PIC16(L)F1825/9

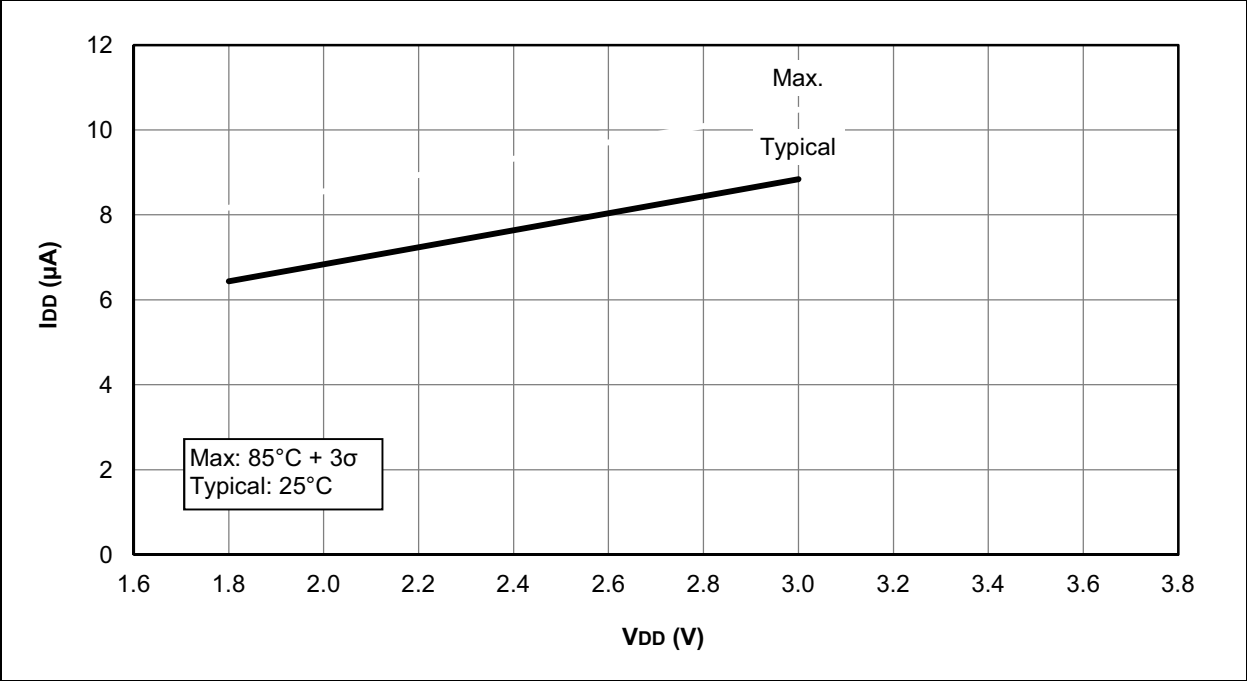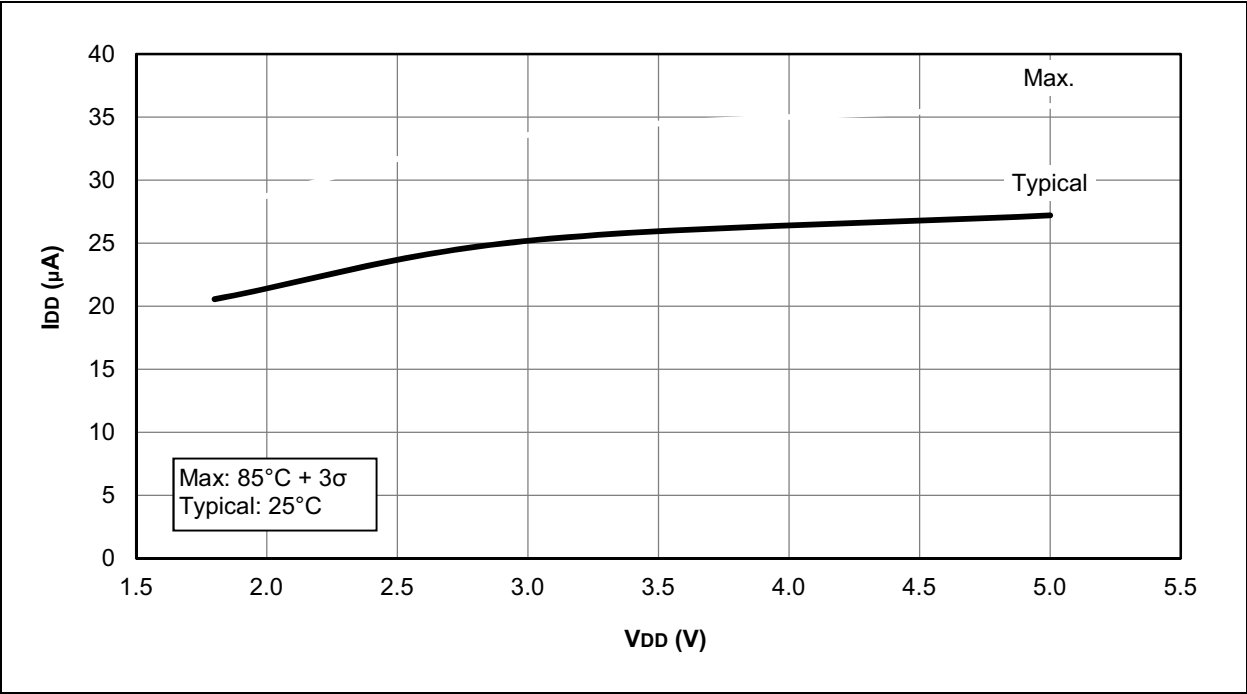**FIGURE 31-11:** I_{DD}, LFINTOSC MODE (F_{OSC} = 31 kHz), PIC16LF1825/9 ONLY

FIGURE 31-11: I_{DD}, LFINTOSC MODE (F_{OSC} = 31 kHz), PIC16LF1825/9 ONLY

Max.

Typical

Max: 85°C + 3σ
Typical: 25°C

I_{DD} (µA)

V_{DD} (V)

FIGURE 31-12: I_{DD}, LFINTOSC MODE (F_{OSC} = 31 kHz), PIC16F1825/9 ONLY

Max.

Typical

Max: 85°C + 3σ
Typical: 25°C

I_{DD} (µA)

V_{DD} (V)

PIC16(L)F1825/9
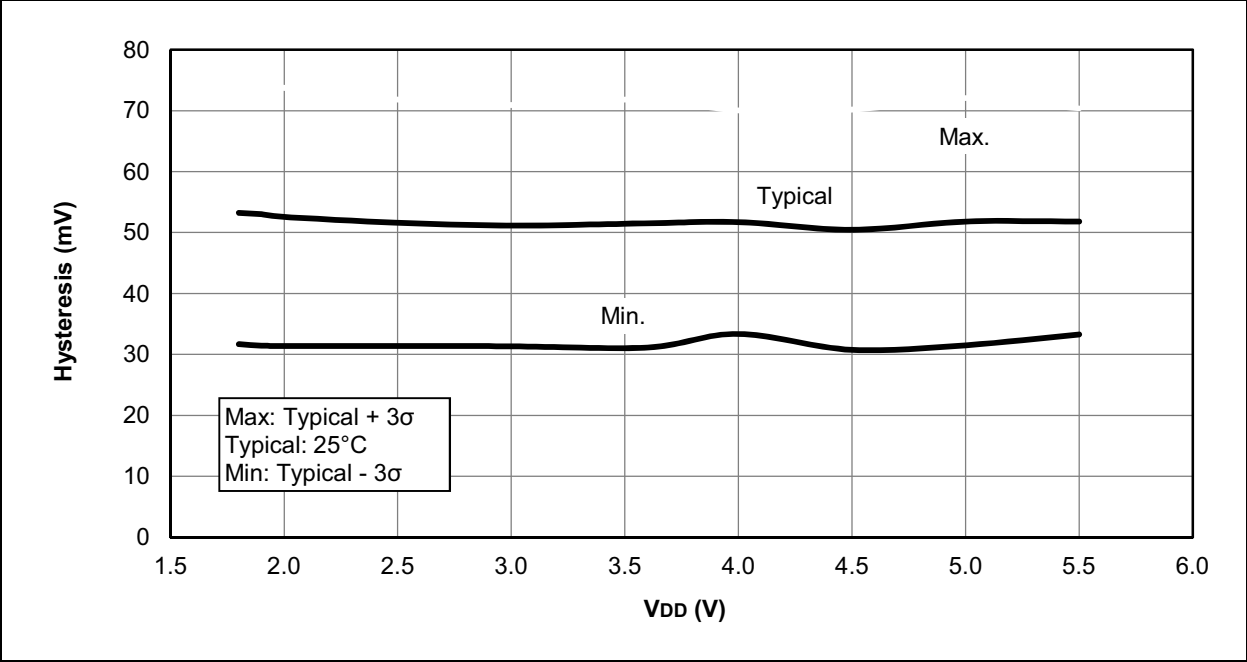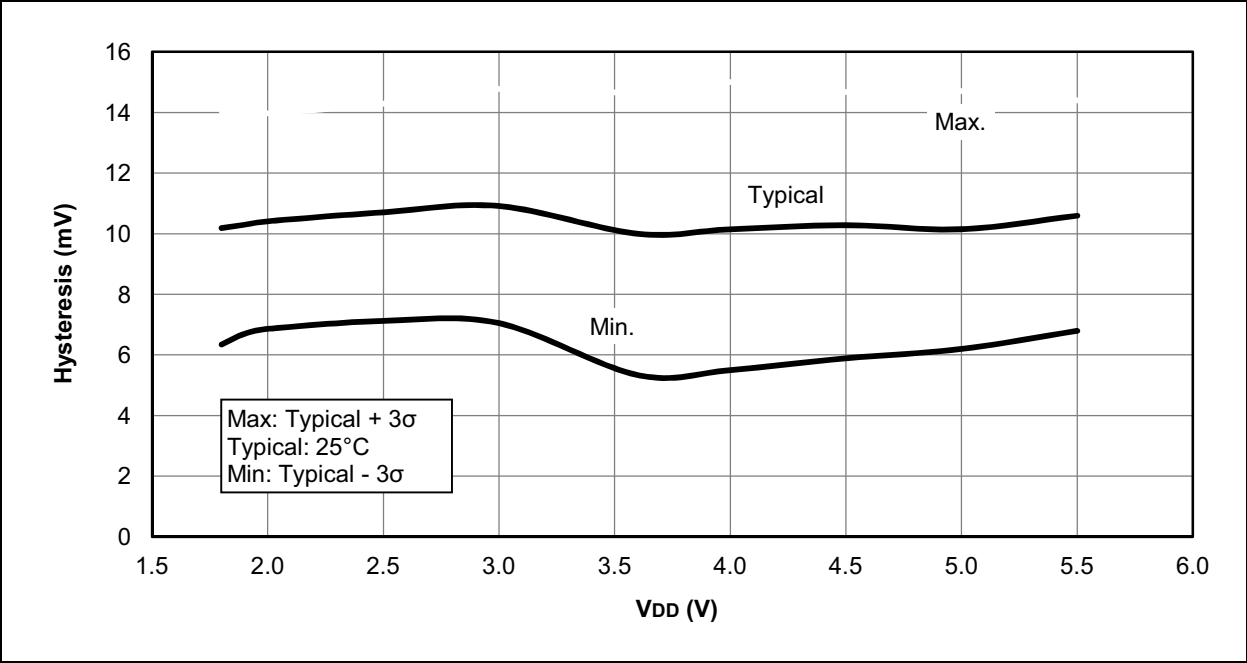
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

VIEW C
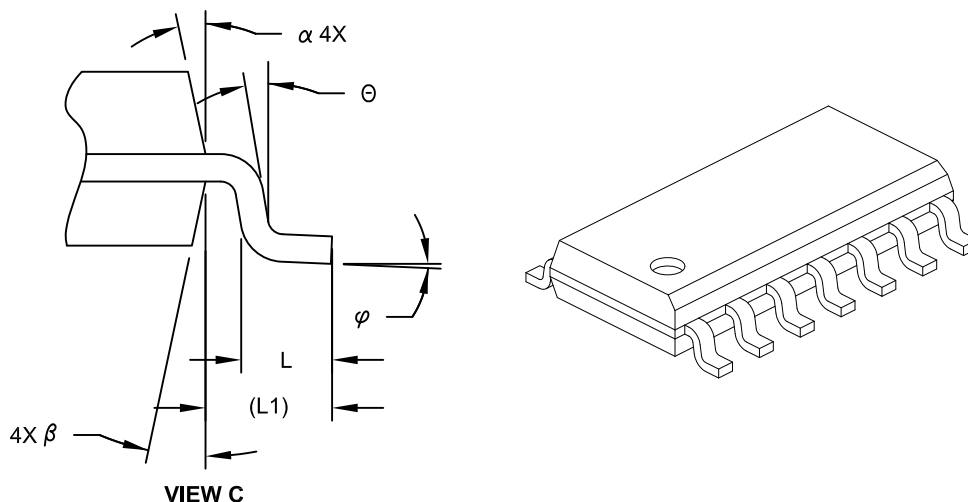
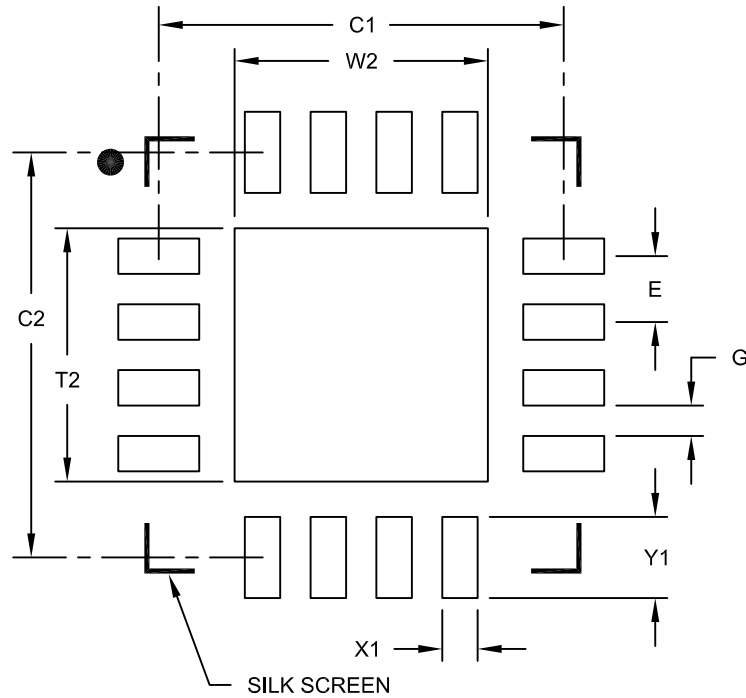|	Units		MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N			14	
Pitch	e			1.27 BSC	
Overall Height	A		-	-	1.75
Molded Package Thickness	A2		1.25	-	-
Standoff §	A1		0.10	-	0.25
Overall Width	E			6.00 BSC	
Molded Package Width	E1			3.90 BSC	
Overall Length	D			8.65 BSC	
Chamfer (Optional)	h		0.25	-	0.50
Foot Length	L		0.40	-	1.27
Footprint	L1			1.04 REF	
Lead Angle	Θ		0°	-	-
Foot Angle	φ		0°	-	8°
Lead Thickness	c		0.10	-	0.25
Lead Width	b		0.31	-	0.51
Mold Draft Angle Top	α		5°	-	15°
Mold Draft Angle Bottom	β		5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

    REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

16-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4x0.9mm Body [QFN]

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

	Units		MILLIMETERS	
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			2.50
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X16)	X1			0.35
Contact Pad Length (X16)	Y1			0.80
Distance Between Pads	G	0.30		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2127A