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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-UQFN (4x4)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1829-e-gz">https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1829-e-gz</a>

**TABLE 1-2: PIC16(L)F1825 PINOUT DESCRIPTION**

Name	Function	Input Type	Output Type	Description
RA0/AN0/CPS0/C1IN+/VREF-/DACOUT/TX <sup>(1)</sup> /CK <sup>(1)</sup> /ICSPDAT/ICDDAT	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	—	A/D Channel 0 input.
	CPS0	AN	—	Capacitive sensing input 0.
	C1IN+	AN	—	Comparator C1 positive input.
	VREF-	AN	—	A/D and DAC Negative Voltage Reference input.
	DACOUT	—	AN	Digital-to-Analog Converter output.
	TX	—	CMOS	USART asynchronous transmit.
	CK	ST	CMOS	USART synchronous clock.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
	ICDDAT	ST	CMOS	In-Circuit Data I/O.
RA1/AN1/CPS1/C12IN0-/VREF+/SRI/RX <sup>(1)</sup> /DT <sup>(1)</sup> /ICSPCLK/ICDCLK	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	—	A/D Channel 1 input.
	CPS1	AN	—	Capacitive sensing input 1.
	C12IN0-	AN	—	Comparator C1 or C2 negative input.
	VREF+	AN	—	A/D and DAC Positive Voltage Reference input.
	SRI	ST	—	SR Latch input.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
	ICSPCLK	ST	—	Serial Programming Clock.
	ICDCLK	ST	—	In-Circuit Debug Clock.
RA2/AN2/CPS2/T0CKI/INT/C1OUT/SRQ/CCP3/FLT0	RA2	ST	CMOS	General purpose I/O.
	AN2	AN	—	A/D Channel 2 input.
	CPS2	AN	—	Capacitive sensing input 2.
	T0CKI	ST	—	Timer0 clock input.
	INT	ST	—	External interrupt.
	C1OUT	—	CMOS	Comparator C1 output.
	SRQ	—	CMOS	SR Latch non-inverting output.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
	FLT0	ST	—	ECCP Auto-Shutdown Fault input.
RA3/SS1 <sup>(1)</sup> /T1G <sup>(1)</sup> /VPP/MCLR	RA3	TTL	—	General purpose input.
	SS1	ST	—	Slave Select input.
	T1G	ST	—	Timer1 Gate input.
	VPP	HV	—	Programming voltage.
	MCLR	ST	—	Master Clear with internal pull-up.

**Legend:** AN = Analog input or output    CMOS = CMOS compatible input or output    OD = Open Drain  
TTL = TTL compatible input    ST = Schmitt Trigger input with CMOS levels    I<sup>2</sup>C™ = Schmitt Trigger input with I<sup>2</sup>C levels  
HV = High Voltage    XTAL = Crystal

**Note 1:** Pin functions can be moved using the APFCON0 or APFCON1 register.

**2:** Default function location.

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**TABLE 3-8: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets	
Bank 3												
180h <sup>(1)</sup>	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx	
181h <sup>(1)</sup>	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx	
182h <sup>(1)</sup>	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000	
183h <sup>(1)</sup>	STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	---1 1000	---q quuu	
184h <sup>(1)</sup>	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu	
185h <sup>(1)</sup>	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000	
186h <sup>(1)</sup>	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu	
187h <sup>(1)</sup>	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000	
188h <sup>(1)</sup>	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000	
189h <sup>(1)</sup>	WREG	Working Register								0000 0000	uuuu uuuu	
18Ah <sup>(1)</sup>	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter								-000 0000	-000 0000
18Bh <sup>(1)</sup>	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000	
18Ch	ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	---1 -111	---1 -111	
18Dh	ANSELB <sup>(2)</sup>	—	—	ANSB5	ANSB4	—	—	—	—	--11 ----	--11 ----	
18Eh	ANSELC	ANSC7 <sup>(2)</sup>	ANSC6 <sup>(2)</sup>	—	—	ANSC3	ANSC2	ANSC1	ANSC0	11-- 1111	11-- 1111	
18Fh	—	Unimplemented								—	—	
190h	—	Unimplemented								—	—	
191h	EEADRL	EEPROM / Program Memory Address Register Low Byte								0000 0000	0000 0000	
192h	EEADRH	— <sup>(4)</sup>	EEPROM / Program Memory Address Register High Byte								1000 0000	1000 0000
193h	EEDATL	EEPROM / Program Memory Read Data Register Low Byte								xxxx xxxx	uuuu uuuu	
194h	EEDATH	—	—	EEPROM / Program Memory Read Data Register High Byte							--xx xxxx	--uu uuuu
195h	EECON1	EEPGD	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	0000 x000	0000 q000	
196h	EECON2	EEPROM control register 2								0000 0000	0000 0000	
197h	—	Unimplemented								—	—	
198h	—	Unimplemented								—	—	
199h	RCREG	USART Receive Data Register								0000 0000	0000 0000	
19Ah	TXREG	USART Transmit Data Register								0000 0000	0000 0000	
19Bh	SPBRGL	Baud Rate Generator Data Register Low								0000 0000	0000 0000	
19Ch	SPBRGH	Baud Rate Generator Data Register High								0000 0000	0000 0000	
19Dh	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x	
19Eh	TXSTA	CSRC	TX9	TXEN	SYNC	SEnDB	BRGH	TRMT	TX9D	0000 0010	0000 0010	
19Fh	BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	01-0 0-00	

**Legend:** x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved.  
Shaded locations are unimplemented, read as '0'.

- Note** 1: These registers can be addressed from any bank.  
2: PIC16(L)F1829 only.  
3: PIC16(L)F1825 only.  
4: Unimplemented, read as '1'.

## 8.6.9 PIR4 REGISTER<sup>(1)</sup>

The PIR4 register contains the interrupt flag bits, as shown in Register 8-9.

**Note 1:** The PIR4 register is available only on the PIC16(L)F1829 device.

**2:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

### REGISTER 8-9: PIR4: PERIPHERAL INTERRUPT REQUEST REGISTER 4<sup>(1)</sup>

U-0	U-0	U-0	U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0
—	—	—	—	—	—	BCL2IF	SSP2IF
bit 7						bit 0	

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

HS = Bit is set by hardware

bit 7-6 **Unimplemented:** Read as '0'

bit 1 **BCL2IF:** MSSP2 Bus Collision Interrupt Flag bit

1 = A Bus Collision was detected (must be cleared in software)

0 = No Bus collision was detected

bit 0 **SSP2IF:** Master Synchronous Serial Port 2 (MSSP2) Interrupt Flag bit

1 = The Transmission/Reception/Bus Condition is complete (must be cleared in software)

0 = Waiting to Transmit/Receive/Bus Condition in progress

**Note 1:** This register is only available on PIC16(L)F1829.

**TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCFIE	TMR0IF	INTF	IOCFIF	87
OPTION_REG	WPUEN	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			176
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	88
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	—	—	CCP2IE	89
PIE3	—	—	CCP4IE	CCP3IE	TMR6IE	—	TMR4IE	—	90
PIE4 <sup>(1)</sup>	—	—	—	—	—	—	BCL2IE	SSP2IE	91
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	92
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	—	CCP2IF	93
PIR3	—	—	CCP4IF	CCP3IF	TMR6IF	—	TMR4IF	—	94
PIR4 <sup>(1)</sup>	—	—	—	—	—	—	BCL2IF	SSP2IF	95

**Legend:** — Unimplemented locations read as '0'. Shaded cells are not used by interrupts.

**Note 1:** PIC16(L)F1829 only.

# PIC16(L)F1825/9

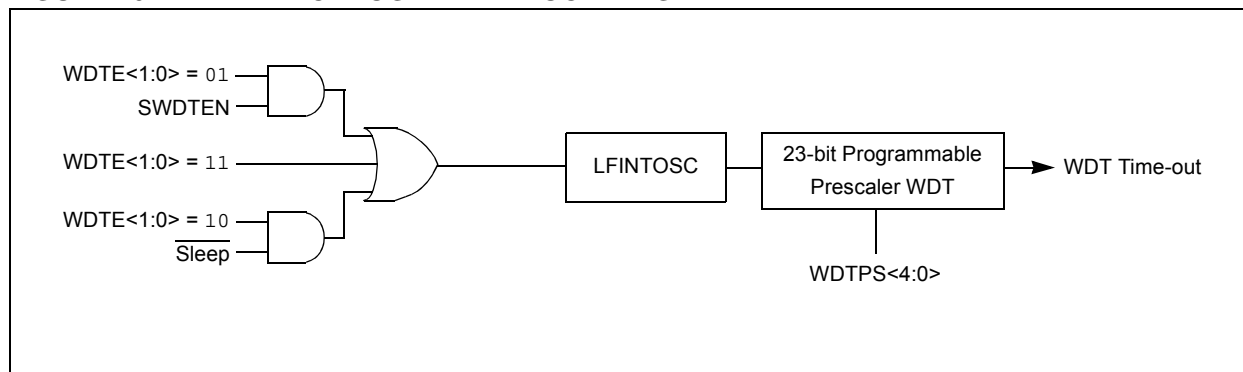
## 10.0 WATCHDOG TIMER

The Watchdog Timer is a system timer that generates a Reset if the firmware does not issue a `CLRWDT` instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events.

The WDT has the following features:

- Independent clock source
- Multiple operating modes
  - WDT is always on
  - WDT is off when in Sleep
  - WDT is controlled by software
  - WDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (typical)
- Multiple Reset conditions
- Operation during Sleep

**FIGURE 10-1: WATCHDOG TIMER BLOCK DIAGRAM**



## REGISTER 16-5: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	—	—	—	ADRES<9:8>	
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-2

**Reserved:** Do not use.

bit 1-0

**ADRES<9:8>:** ADC Result Register bits

Upper two bits of 10-bit conversion result

## REGISTER 16-6: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADRES<7:0>							
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

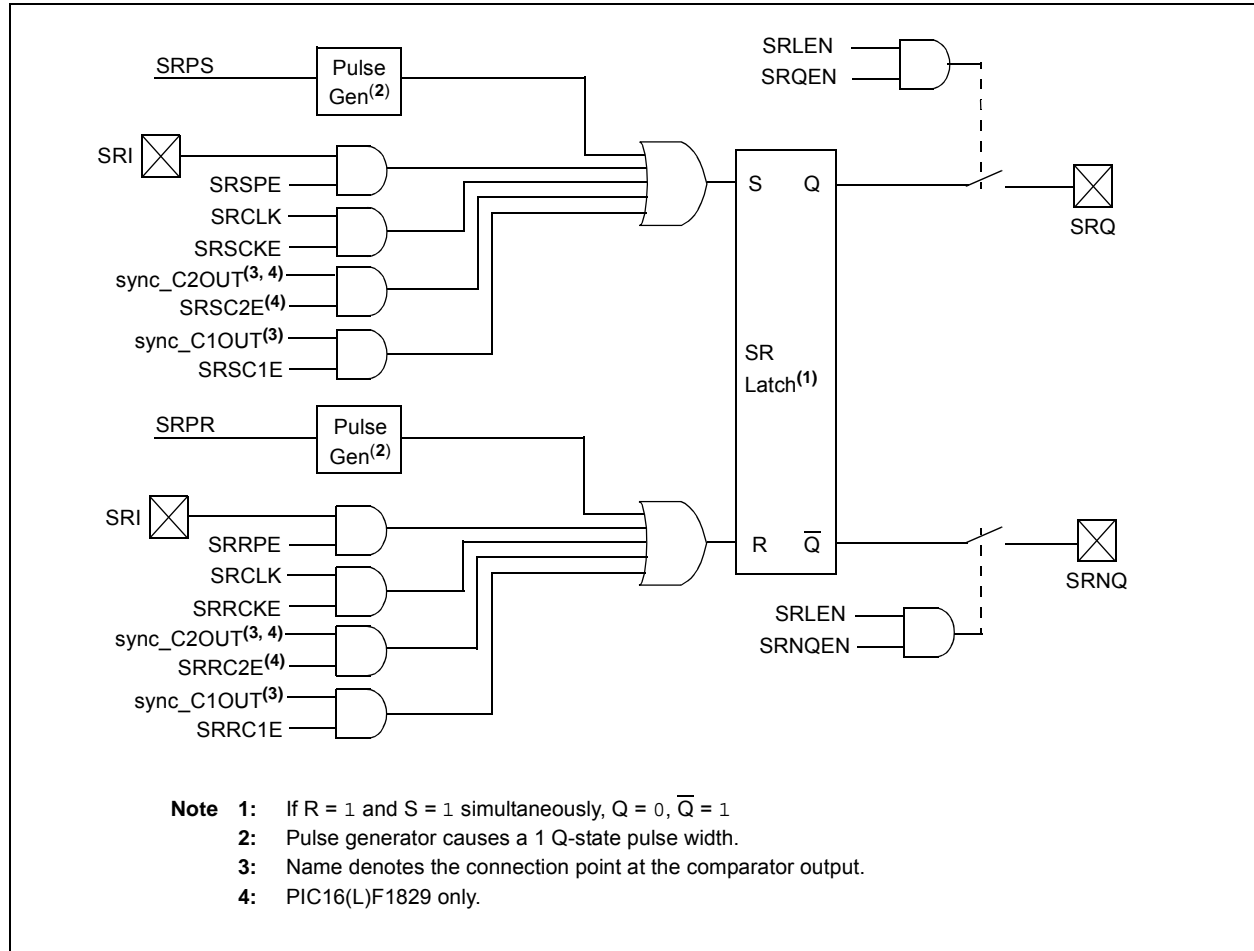
'0' = Bit is cleared

bit 7-0

**ADRES<7:0>:** ADC Result Register bits

Lower eight bits of 10-bit conversion result

**FIGURE 18-1: SR LATCH SIMPLIFIED BLOCK DIAGRAM**



## REGISTER 18-2: SRCON1: SR LATCH CONTROL 1 REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
SRSPPE	SRSCKE	SRSC2E <sup>(1)</sup>	SRSC1E	SRRPE	SRRCKE	SRRC2E <sup>(1)</sup>	SRRC1E
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7 **SRSPPE**: SR Latch Peripheral Set Enable bit  
1 = SR latch is set when the SRI pin is high  
0 = SRI pin has no effect on the set input of the SR latch
- bit 6 **SRSCKE**: SR Latch Set Clock Enable bit  
1 = Set input of SR latch is pulsed with SRCLK  
0 = SRCLK has no effect on the set input of the SR latch
- bit 5 **SRSC2E**: SR Latch C2 Set Enable bit<sup>(1)</sup>  
1 = SR latch is set when the C2 Comparator output is high  
0 = C2 Comparator output has no effect on the set input of the SR latch
- bit 4 **SRSC1E**: SR Latch C1 Set Enable bit  
1 = SR latch is set when the C1 Comparator output is high  
0 = C1 Comparator output has no effect on the set input of the SR latch
- bit 3 **SRRPE**: SR Latch Peripheral Reset Enable bit  
1 = SR latch is reset when the SRI pin is high  
0 = SRI pin has no effect on the Reset input of the SR latch
- bit 2 **SRRCKE**: SR Latch Reset Clock Enable bit  
1 = Reset input of SR latch is pulsed with SRCLK  
0 = SRCLK has no effect on the Reset input of the SR latch
- bit 1 **SRRC2E**: SR Latch C2 Reset Enable bit<sup>(1)</sup>  
1 = SR latch is reset when the C2 Comparator output is high  
0 = C2 Comparator output has no effect on the Reset input of the SR latch
- bit 0 **SRRC1E**: SR Latch C1 Reset Enable bit  
1 = SR latch is reset when the C1 Comparator output is high  
0 = C1 Comparator output has no effect on the Reset input of the SR latch

**Note 1:** PIC16(L)F1829 only.



FIGURE 21-3: TIMER1 GATE ENABLE MODE

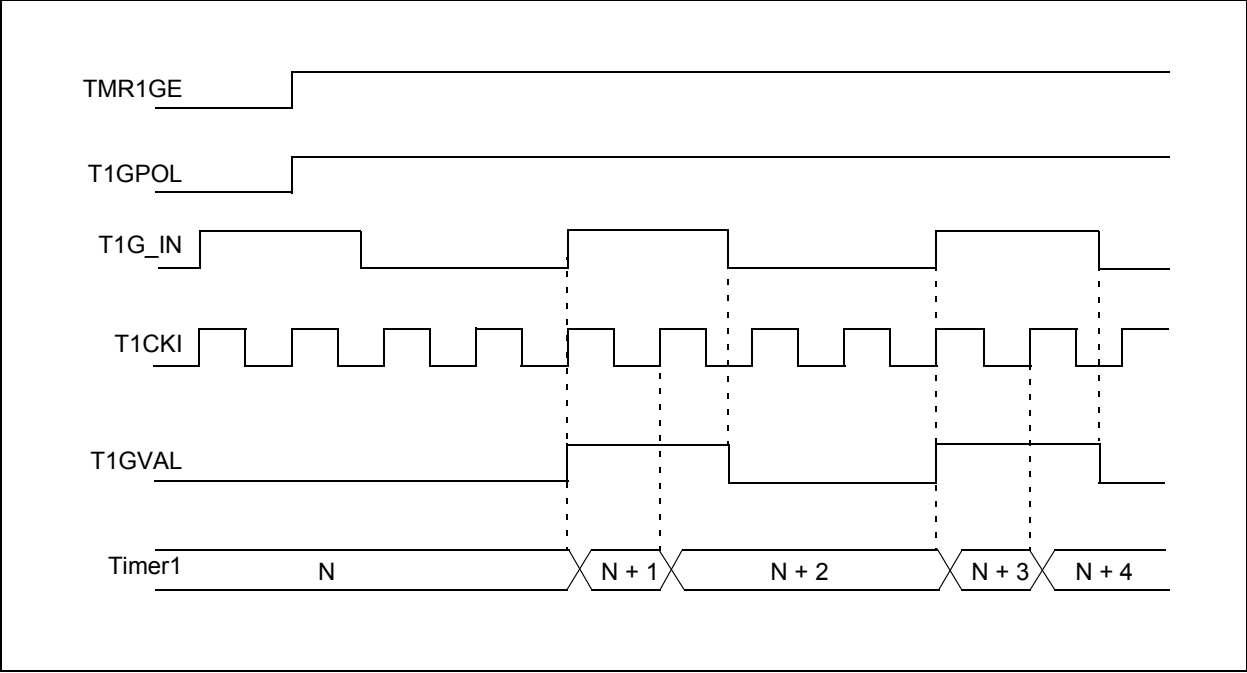
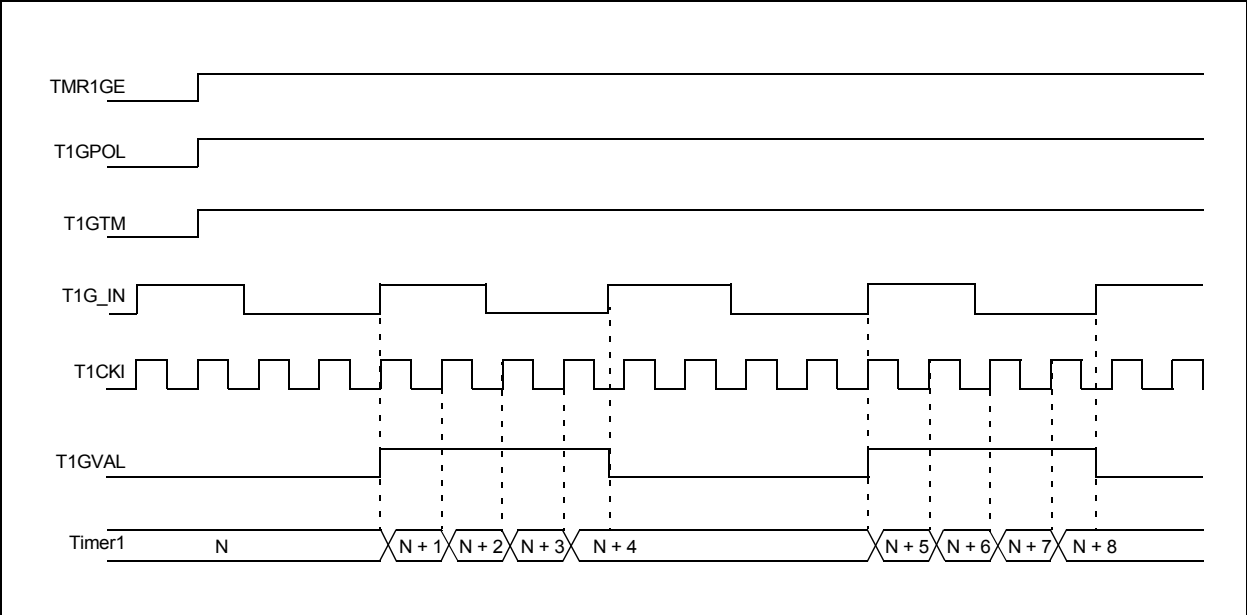


FIGURE 21-4: TIMER1 GATE TOGGLE MODE



## 25.5.2.3 7-bit Transmission with Address Hold Enabled

Setting the AHEN bit of the SSPxCON3 register enables additional clock stretching and interrupt generation after the eighth falling edge of a received matching address. Once a matching address has been clocked in, CKP is cleared and the SSPxIF interrupt is set.

Figure 25-19 displays a standard waveform of a 7-bit Address Slave Transmission with AHEN enabled.

1. Bus starts Idle.
2. Master sends Start condition; the S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
3. Master sends matching address with  $\overline{R/W}$  bit set. After the eighth falling edge of the SCLx line the CKP bit is cleared and SSPxIF interrupt is generated.
4. Slave software clears SSPxIF.
5. Slave software reads ACKTIM bit of SSPxCON3 register, and  $\overline{R/W}$  and D/A of the SSPxSTAT register to determine the source of the interrupt.
6. Slave reads the address value from the SSPxBUF register clearing the BF bit.
7. Slave software decides from this information if it wishes to ACK or not ACK and sets the ACKDT bit of the SSPxCON2 register accordingly.
8. Slave sets the CKP bit releasing SCLx.
9. Master clocks in the  $\overline{ACK}$  value from the slave.
10. Slave hardware automatically clears the CKP bit and sets SSPxIF after the  $\overline{ACK}$  if the  $\overline{R/W}$  bit is set.
11. Slave software clears SSPxIF.
12. Slave loads value to transmit to the master into SSPxBUF setting the BF bit.

**Note:** SSPxBUF cannot be loaded until after the  $\overline{ACK}$ .

13. Slave sets CKP bit releasing the clock.
14. Master clocks out the data from the slave and sends an  $\overline{ACK}$  value on the 9th SCLx pulse.
15. Slave hardware copies the  $\overline{ACK}$  value into the ACKSTAT bit of the SSPxCON2 register.
16. Steps 10-15 are repeated for each byte transmitted to the master from the slave.
17. If the master sends a not  $\overline{ACK}$  the slave releases the bus allowing the master to send a Stop and end the communication.

**Note:** Master must send a not  $\overline{ACK}$  on the last byte to ensure that the slave releases the SCLx line to receive a Stop.

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## 25.6.13.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

- A low level is sampled on SDAx when SCLx goes from low level to high level. (CASE 1)
- SCLx goes low before SDAx is asserted low, indicating that another master is attempting to transmit a data '1'. (CASE 2)

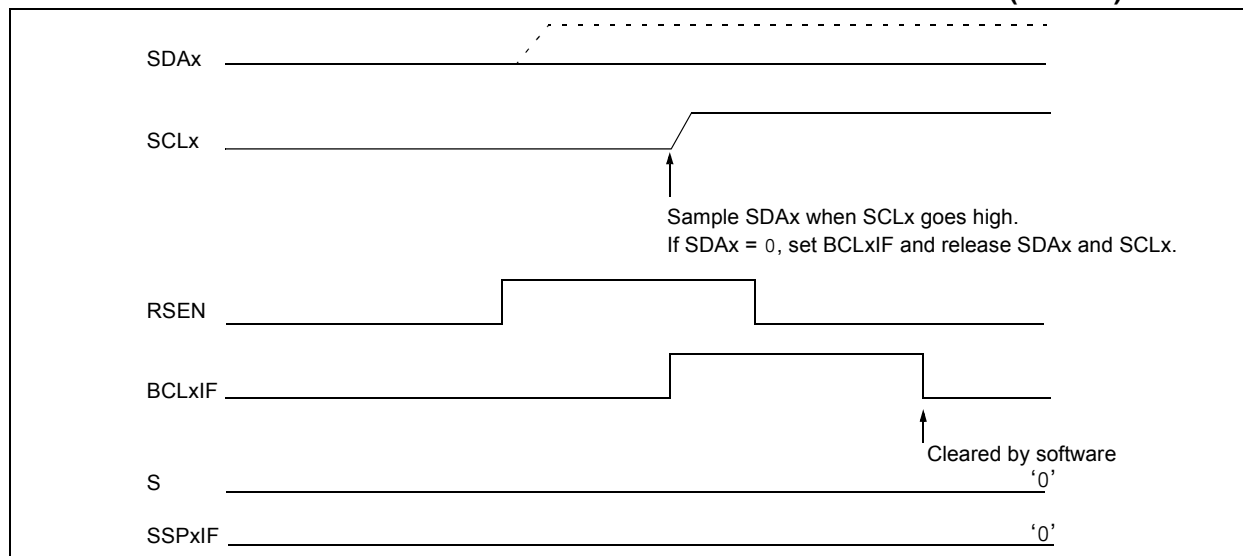
When the user releases SDAx and the pin is allowed to float high, the BRG is loaded with SSPxADD and counts down to zero. The SCLx pin is then deasserted and when sampled high, the SDAx pin is sampled.

If SDAx is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0' (Figure 25-36). If SDAx is sampled high, the BRG is reloaded and begins counting. If SDAx goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDAx at exactly the same time.

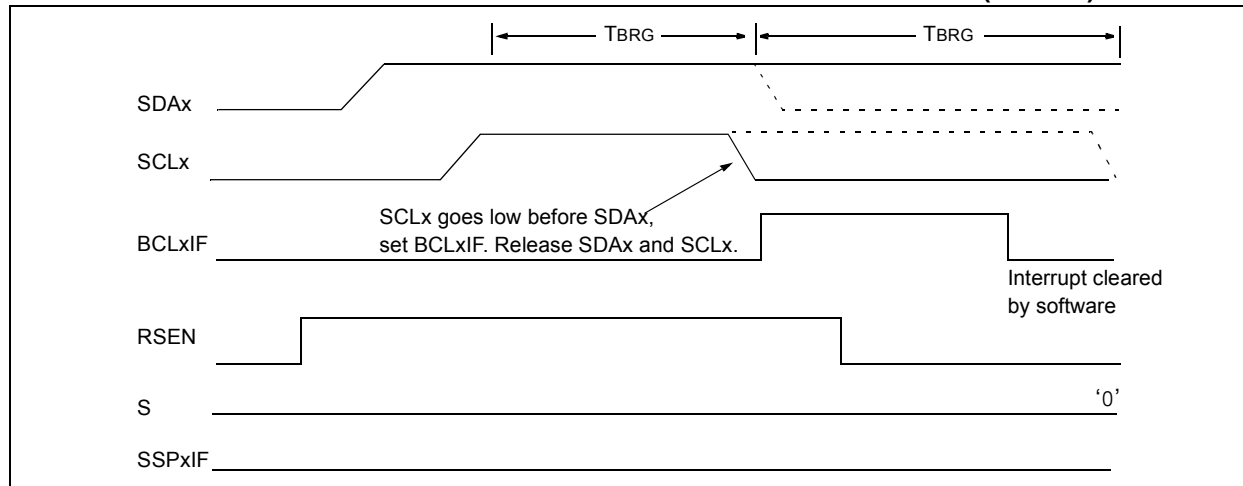
If SCLx goes from high-to-low before the BRG times out and SDAx has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition (Figure 25-37).

If, at the end of the BRG time-out, both SCLx and SDAx are still high, the SDAx pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCLx pin, the SCLx pin is driven low and the Repeated Start condition is complete.

**FIGURE 25-36: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)**



**FIGURE 25-37: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)**



# PIC16(L)F1825/9

## REGISTER 25-3: SSPxCON2: SSPx CONTROL REGISTER 2

R/W-0/0	R-0/0	R/W-0/0	R/S/HS-0/0	R/S/HS-0/0	R/S/HS-0/0	R/S/HS-0/0	R/W/HS-0/0
GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Cleared by hardware S = User set

- bit 7 **GCEN:** General Call Enable bit (in I<sup>2</sup>C Slave mode only)  
1 = Enable interrupt when a general call address (0x00 or 00h) is received in the SSPxSR  
0 = General call address disabled
- bit 6 **ACKSTAT:** Acknowledge Status bit (in I<sup>2</sup>C mode only)  
1 = Acknowledge was not received  
0 = Acknowledge was received
- bit 5 **ACKDT:** Acknowledge Data bit (in I<sup>2</sup>C mode only)  
In Receive mode:  
Value transmitted when the user initiates an Acknowledge sequence at the end of a receive  
1 = Not Acknowledge  
0 = Acknowledge
- bit 4 **ACKEN:** Acknowledge Sequence Enable bit (in I<sup>2</sup>C Master mode only)  
In Master Receive mode:  
1 = Initiate Acknowledge sequence on SDAx and SCLx pins, and transmit ACKDT data bit.  
Automatically cleared by hardware.  
0 = Acknowledge sequence Idle
- bit 3 **RCEN:** Receive Enable bit (in I<sup>2</sup>C Master mode only)  
1 = Enables Receive mode for I<sup>2</sup>C  
0 = Receive Idle
- bit 2 **PEN:** Stop Condition Enable bit (in I<sup>2</sup>C Master mode only)  
SCKx Release Control:  
1 = Initiate Stop condition on SDAx and SCLx pins. Automatically cleared by hardware.  
0 = Stop condition Idle
- bit 1 **RSEN:** Repeated Start Condition Enabled bit (in I<sup>2</sup>C Master mode only)  
1 = Initiate Repeated Start condition on SDAx and SCLx pins. Automatically cleared by hardware.  
0 = Repeated Start condition Idle
- bit 0 **SEN:** Start Condition Enable/Stretch Enable bit  
In Master mode:  
1 = Initiate Start condition on SDAx and SCLx pins. Automatically cleared by hardware.  
0 = Start condition Idle  
In Slave mode:  
1 = Clock stretching is enabled for both slave transmit and slave receive (stretch enabled)  
0 = Clock stretching is disabled

**Note 1:** For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I<sup>2</sup>C module is not in the Idle mode, this bit may not be set (no spooling) and the SSPxBUF may not be written (or writes to the SSPxBUF are disabled).

## 26.1.2 EUSART ASYNCHRONOUS RECEIVER

The Asynchronous mode is typically used in RS-232 systems. The receiver block diagram is shown in Figure 26-2. The data is received on the RX/DT pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at 16 times the baud rate, whereas the serial Receive Shift Register (RSR) operates at the bit rate. When all eight or nine bits of the character have been shifted in, they are immediately transferred to a two character First-In-First-Out (FIFO) memory. The FIFO buffering allows reception of two complete characters and the start of a third character before software must start servicing the EUSART receiver. The FIFO and RSR registers are not directly accessible by software. Access to the received data is via the RCREG register.

### 26.1.2.1 Enabling the Receiver

The EUSART receiver is enabled for asynchronous operation by configuring the following three control bits:

- CREN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the CREN bit of the RCSTA register enables the receiver circuitry of the EUSART. Clearing the SYNC bit of the TXSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the EUSART. The programmer must set the corresponding TRIS bit to configure the RX/DT I/O pin as an input.

**Note 1:** If the RX/DT function is on an analog pin, the corresponding ANSEL bit must be cleared for the receiver to function.

### 26.1.2.2 Receiving Data

The receiver data recovery circuit initiates character reception on the falling edge of the first bit. The first bit, also known as the Start bit, is always a zero. The data recovery circuit counts one-half bit time to the center of the Start bit and verifies that the bit is still a zero. If it is not a zero then the data recovery circuit aborts character reception, without generating an error, and resumes looking for the falling edge of the Start bit. If the Start bit zero verification succeeds then the data recovery circuit counts a full bit time to the center of the next bit. The bit is then sampled by a majority detect circuit and the resulting '0' or '1' is shifted into the RSR. This repeats until all data bits have been sampled and shifted into the RSR. One final bit time is measured and the level sampled. This is the Stop bit, which is always a '1'. If the data recovery circuit samples a '0' in the Stop bit position then a framing error is set for this character, otherwise the framing error is cleared for this character. See **Section 26.1.2.4 "Receive Framing Error"** for more information on framing errors.

Immediately after all data bits and the Stop bit have been received, the character in the RSR is transferred to the EUSART receive FIFO and the RCIF interrupt flag bit of the PIR1 register is set. The top character in the FIFO is transferred out of the FIFO by reading the RCREG register.

**Note:** If the receive FIFO is overrun, no additional characters will be received until the overrun condition is cleared. See **Section 26.1.2.5 "Receive Overrun Error"** for more information on overrun errors.

### 26.1.2.3 Receive Interrupts

The RCIF interrupt flag bit of the PIR1 register is set whenever the EUSART receiver is enabled and there is an unread character in the receive FIFO. The RCIF interrupt flag bit is read-only, it cannot be set or cleared by software.

RCIF interrupts are enabled by setting all of the following bits:

- RCIE interrupt enable bit of the PIE1 register
- PEIE Peripheral Interrupt Enable bit of the INTCON register
- GIE Global Interrupt Enable bit of the INTCON register

The RCIF interrupt flag bit will be set when there is an unread character in the FIFO, regardless of the state of interrupt enable bits.

## 26.1.2.8 Asynchronous Reception Setup:

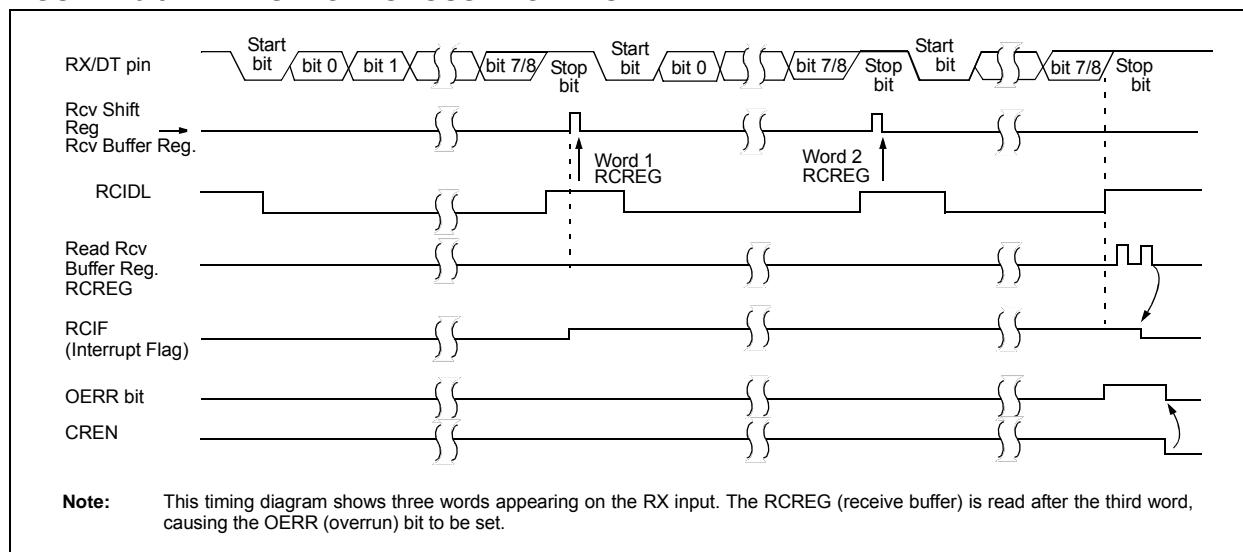
1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 26.3 “EUSART Baud Rate Generator (BRG)”**).
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
5. If 9-bit reception is desired, set the RX9 bit.
6. Enable reception by setting the CREN bit.
7. The RCIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
8. Read the RCSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
9. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register.
10. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

## 26.1.2.9 9-bit Address Detection Mode Setup

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 26.3 “EUSART Baud Rate Generator (BRG)”**).
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
5. Enable 9-bit reception by setting the RX9 bit.
6. Enable address detection by setting the ADDEN bit.
7. Enable reception by setting the CREN bit.
8. The RCIF interrupt flag bit will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
9. Read the RCSTA register to get the error flags. The ninth data bit will always be set.
10. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register. Software determines if this is the device's address.
11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
12. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.

**FIGURE 26-5: ASYNCHRONOUS RECEPTION**



# PIC16(L)F1825/9

## 26.2 Clock Accuracy with Asynchronous Operation

The factory calibrates the internal oscillator block output (INTOSC). However, the INTOSC frequency may drift as V<sub>DD</sub> or temperature changes, and this directly affects the asynchronous baud rate. Two methods may be used to adjust the baud rate clock, but both require a reference clock source of some kind.

The first (preferred) method uses the OSCTUNE register to adjust the INTOSC output. Adjusting the value in the OSCTUNE register allows for fine resolution changes to the system clock source. See **Section 5.2.2 “Internal Clock Sources”** for more information.

The other method adjusts the value in the Baud Rate Generator. This can be done automatically with the Auto-Baud Detect feature (see **Section 26.3.1 “Auto-Baud Detect”**). There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change in the peripheral clock frequency.

### REGISTER 26-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-1/1	R/W-0/0
CSRC	TX9	TXEN <sup>(1)</sup>	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

- bit 7      **CSRC:** Clock Source Select bit  
Asynchronous mode:  
Don't care  
Synchronous mode:  
1 = Master mode (clock generated internally from BRG)  
0 = Slave mode (clock from external source)
- bit 6      **TX9:** 9-bit Transmit Enable bit  
1 = Selects 9-bit transmission  
0 = Selects 8-bit transmission
- bit 5      **TXEN:** Transmit Enable bit<sup>(1)</sup>  
1 = Transmit enabled  
0 = Transmit disabled
- bit 4      **SYNC:** EUSART Mode Select bit  
1 = Synchronous mode  
0 = Asynchronous mode
- bit 3      **SENDB:** Send Break Character bit  
Asynchronous mode:  
1 = Send Sync Break on next transmission (cleared by hardware upon completion)  
0 = Sync Break transmission completed  
Synchronous mode:  
Don't care
- bit 2      **BRGH:** High Baud Rate Select bit  
Asynchronous mode:  
1 = High speed  
0 = Low speed  
Synchronous mode:  
Unused in this mode
- bit 1      **TRMT:** Transmit Shift Register Status bit  
1 = TSR empty  
0 = TSR full
- bit 0      **TX9D:** Ninth bit of Transmit Data  
Can be address/data bit or a parity bit.

**Note 1:** SREN/CREN overrides TXEN in Sync mode.

**TABLE 26-5: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)**

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	26666	300.0	0.00	16665	300.0	0.00	15359	300.0	0.00	9215
1200	1200	0.00	6666	1200	-0.01	4166	1200	0.00	3839	1200	0.00	2303
2400	2400	0.01	3332	2400	0.02	2082	2400	0.00	1919	2400	0.00	1151
9600	9604	0.04	832	9597	-0.03	520	9600	0.00	479	9600	0.00	287
10417	10417	0.00	767	10417	0.00	479	10425	0.08	441	10433	0.16	264
19.2k	19.18k	-0.08	416	19.23k	0.16	259	19.20k	0.00	239	19.20k	0.00	143
57.6k	57.55k	-0.08	138	57.47k	-0.22	86	57.60k	0.00	79	57.60k	0.00	47
115.2k	115.9k	0.64	68	116.3k	0.94	42	115.2k	0.00	39	115.2k	0.00	23

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	6666	300.0	0.01	3332	300.0	0.00	3071	300.1	0.04	832
1200	1200	-0.02	1666	1200	0.04	832	1200	0.00	767	1202	0.16	207
2400	2401	0.04	832	2398	0.08	416	2400	0.00	383	2404	0.16	103
9600	9615	0.16	207	9615	0.16	103	9600	0.00	95	9615	0.16	25
10417	10417	0	191	10417	0.00	95	10473	0.53	87	10417	0.00	23
19.2k	19.23k	0.16	103	19.23k	0.16	51	19.20k	0.00	47	19.23k	0.16	12
57.6k	57.14k	-0.79	34	58.82k	2.12	16	57.60k	0.00	15	—	—	—
115.2k	117.6k	2.12	16	111.1k	-3.55	8	115.2k	0.00	7	—	—	—



## 30.2 DC Characteristics: PIC16(L)F1825/9-I/E (Industrial, Extended) (Continued)

PIC16LF1825/9			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature    -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
PIC16F1825/9			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature    -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						VDD	Note
	Supply Current (IDD) <sup>(1, 2)</sup>						
D020		—	2.7	3.6	mA	3.0	Fosc = 32 MHz
		—	3.2	4.2	mA	3.6	HS Oscillator mode (Note 4)
D020		—	2.7	4.0	mA	3.0	Fosc = 32 MHz
		—	3.2	4.3	mA	5.0	HS Oscillator mode (Note 4)
D021		—	222	350	μA	1.8	Fosc = 4 MHz
		—	400	690	μA	3.0	EXTRC mode (Note 5)
D021		—	240	500	μA	1.8	Fosc = 4 MHz
		—	416	800	μA	3.0	EXTRC mode (Note 5)
		—	497	900	μA	5.0	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** The test conditions for all I<sub>DD</sub> measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V<sub>DD</sub>; MCLR = V<sub>DD</sub>; WDT disabled.
- Note 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
- Note 3:** 8 MHz internal RC oscillator with 4xPLL enabled.
- Note 4:** 8 MHz crystal oscillator with 4xPLL enabled.
- Note 5:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula  $I_R = V_{DD}/2R_{EXT}$  (mA) with REXT in kΩ.

**TABLE 30-2: OSCILLATOR PARAMETERS**

Standard Operating Conditions (unless otherwise stated) Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$								
Param No.	Sym.	Characteristic	Freq. Tolerance	Min.	Typ†	Max.	Units	Conditions
OS08	HFOSC	Internal Calibrated HFINTOSC Frequency <sup>(1)</sup>	$\pm 2\%$	—	16.0	—	MHz	$0^{\circ}\text{C} \leq T_A \leq +60^{\circ}\text{C}$ , $V_{DD} \geq 2.5\text{V}$
			$\pm 3\%$	—	16.0	—	MHz	$60^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ , $V_{DD} \geq 2.5\text{V}$
			$\pm 5\%$	—	16.0	—	MHz	$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$
OS08A	MFOSC	Internal Calibrated MFINTOSC Frequency <sup>(1)</sup>	$\pm 2\%$	—	500	—	kHz	$0^{\circ}\text{C} \leq T_A \leq +60^{\circ}\text{C}$ , $V_{DD} \geq 2.5\text{V}$
			$\pm 3\%$	—	500	—	kHz	$60^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ , $V_{DD} \geq 2.5\text{V}$
			$\pm 5\%$	—	500	—	kHz	$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$
OS09	LFOSC	Internal LFINTOSC Frequency	$\pm 25\%$	—	31	—	kHz	$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$
OS10*	TIOSC ST	HFINTOSC Wake-up from Sleep Start-up Time	—	—	5	8	$\mu\text{s}$	
		MFINTOSC Wake-up from Sleep Start-up Time	—	—	20	30	$\mu\text{s}$	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** To ensure these oscillator frequency tolerances,  $V_{DD}$  and  $V_{SS}$  must be capacitively decoupled as close to the device as possible. 0.1  $\mu\text{F}$  and 0.01  $\mu\text{F}$  values in parallel are recommended.

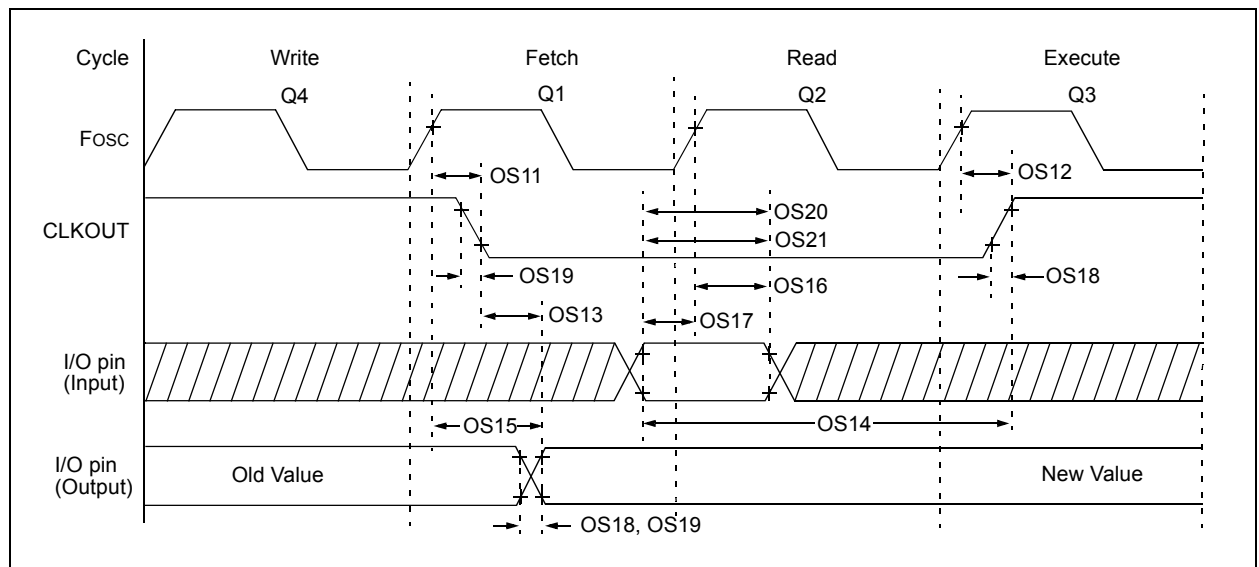
**TABLE 30-3: PLL CLOCK TIMING SPECIFICATIONS ( $V_{DD} = 2.7\text{V TO } 5.5\text{V}$ )**

Param No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
F10	FOSC	Oscillator Frequency Range	4	—	8	MHz	
F11	FSYS	On-Chip VCO System Frequency	16	—	32	MHz	
F12	TRC	PLL Start-up Time (Lock Time)	—	—	2	ms	
F13*	$\Delta\text{CLK}$	CLKOUT Stability (Jitter)	-0.25%	—	+0.25%	%	

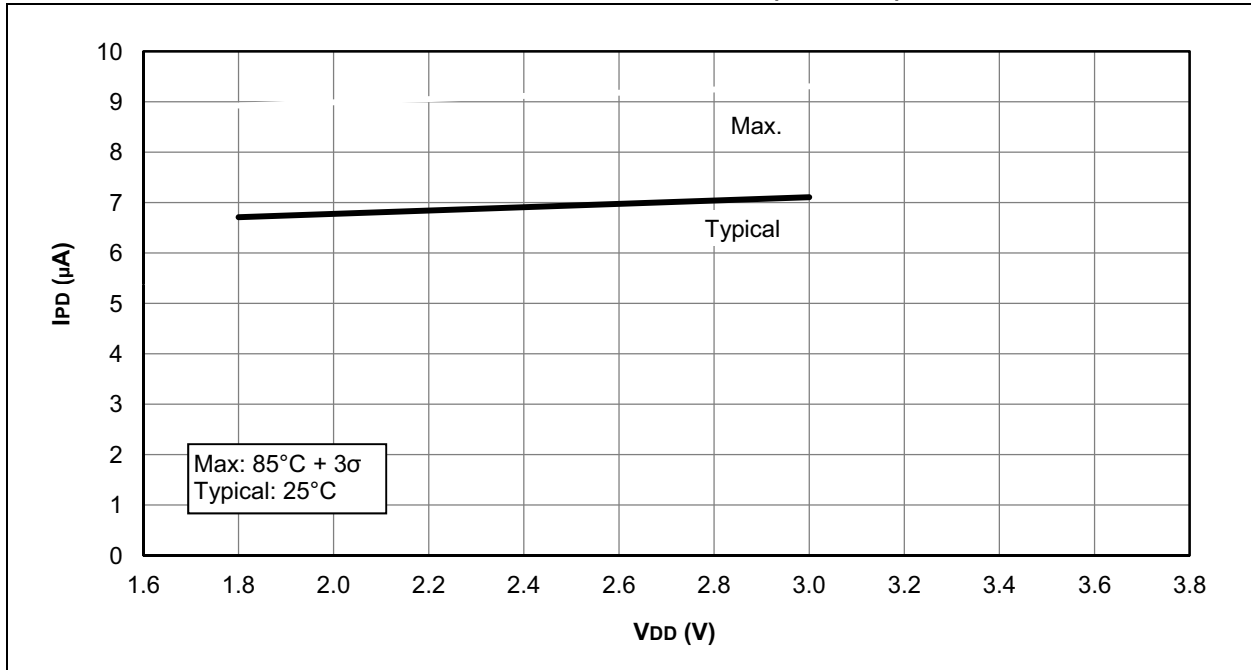
\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

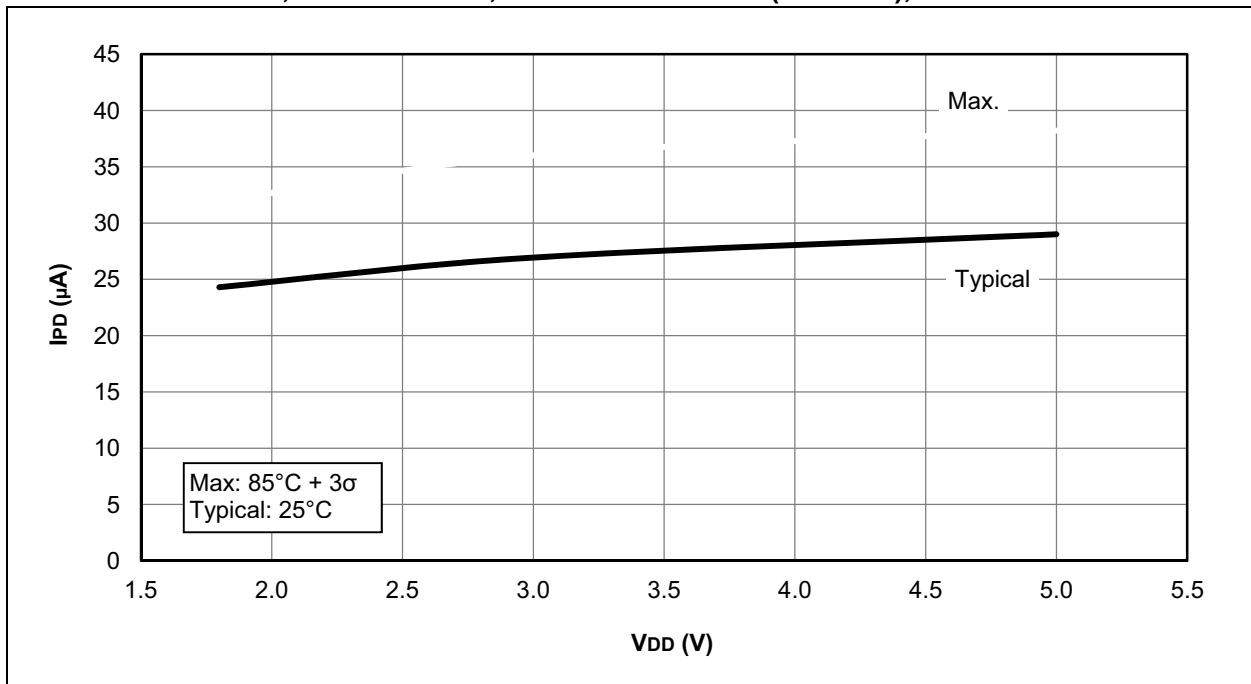
**FIGURE 30-7: CLKOUT AND I/O TIMING**



**FIGURE 31-37:  $I_{PD}$ , COMPARATOR, LOW-POWER MODE ( $CxSP = 0$ ), PIC16LF1825/9 ONLY**



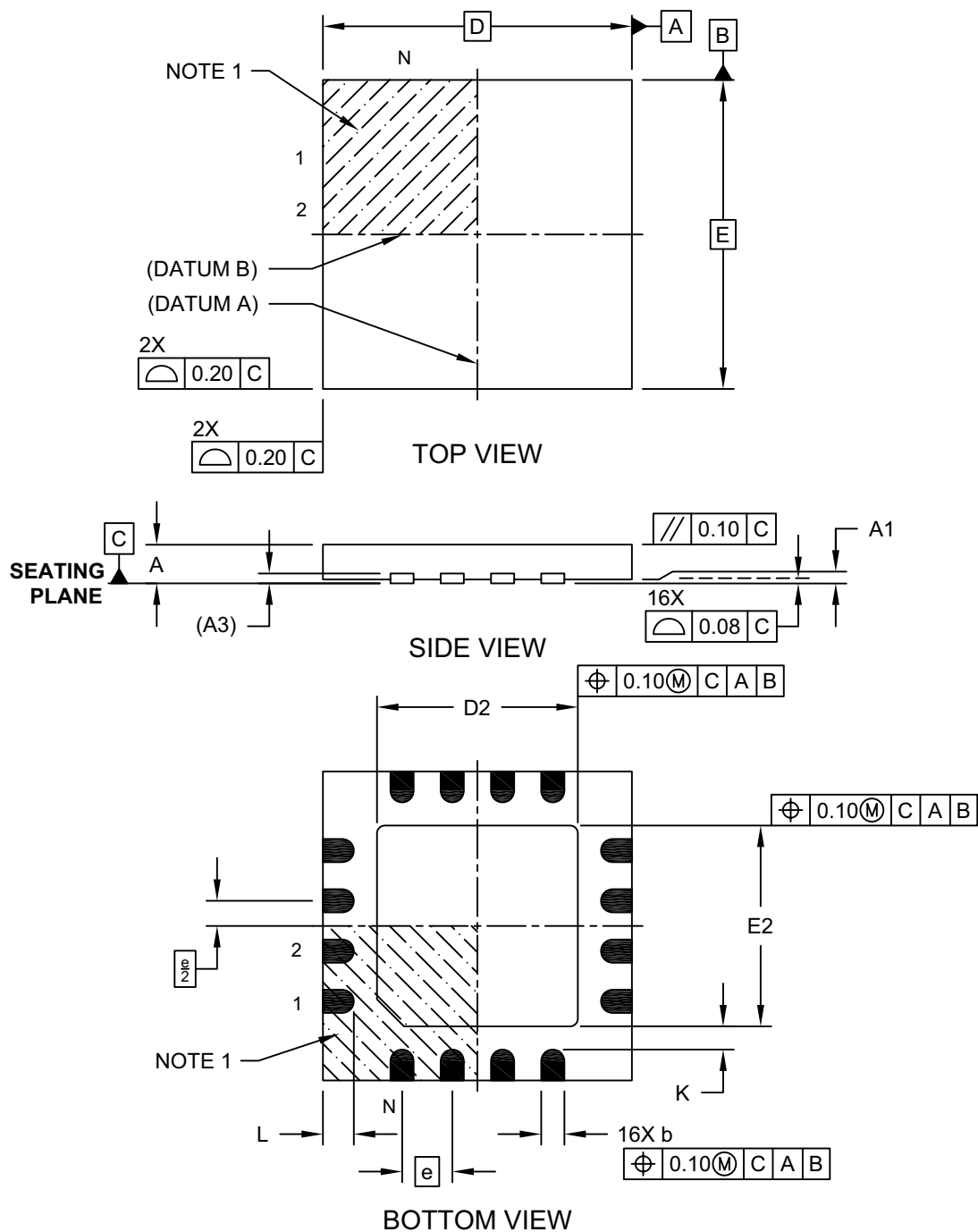
**FIGURE 31-38:  $I_{PD}$ , COMPARATOR, LOW-POWER MODE ( $CxSP = 0$ ), PIC16F1825/9 ONLY**



# PIC16(L)F1825/9

## 16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (JQ) - 4x4x0.5 mm Body [UQFN]

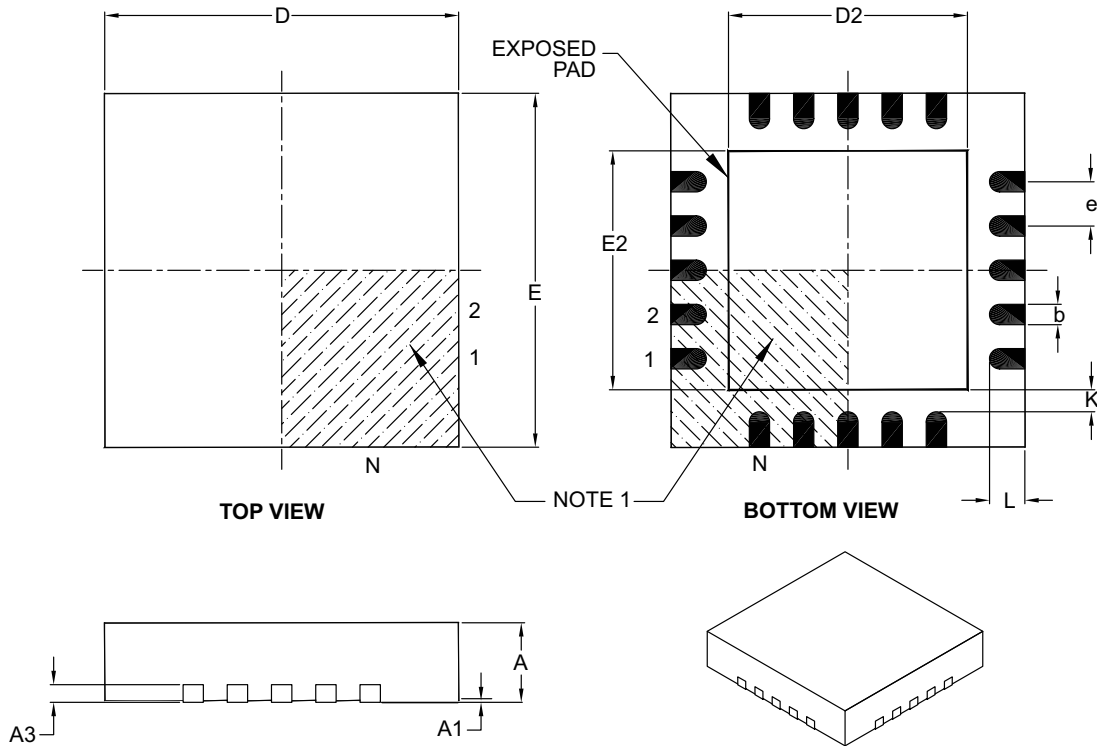
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-257A Sheet 1 of 2

## 20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	4.00 BSC		
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D	4.00 BSC		
Exposed Pad Length	D2	2.60	2.70	2.80
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	—	—

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
  - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B