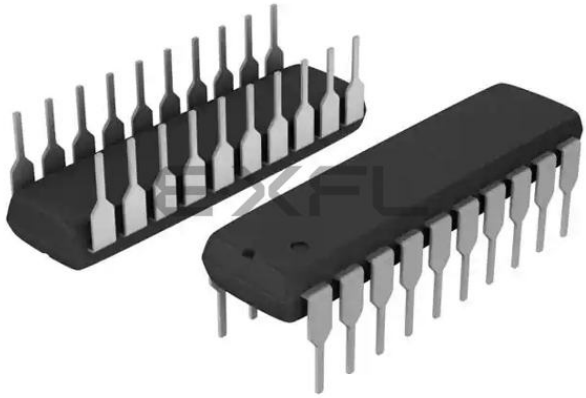

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	16MHz
Connectivity	LINbusSCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	15
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7flite35f2b6

2 PIN DESCRIPTION

Figure 2. 20-Pin QFN Package Pinout

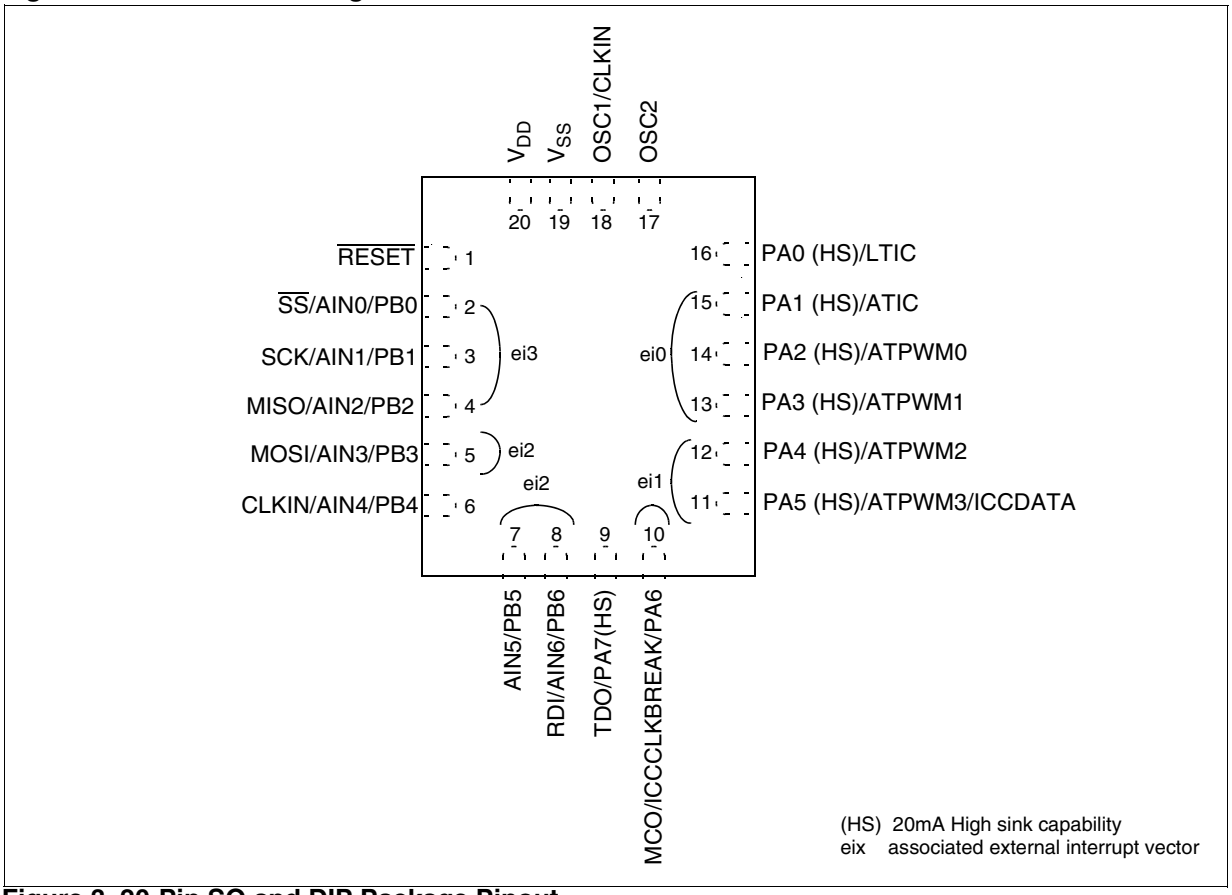
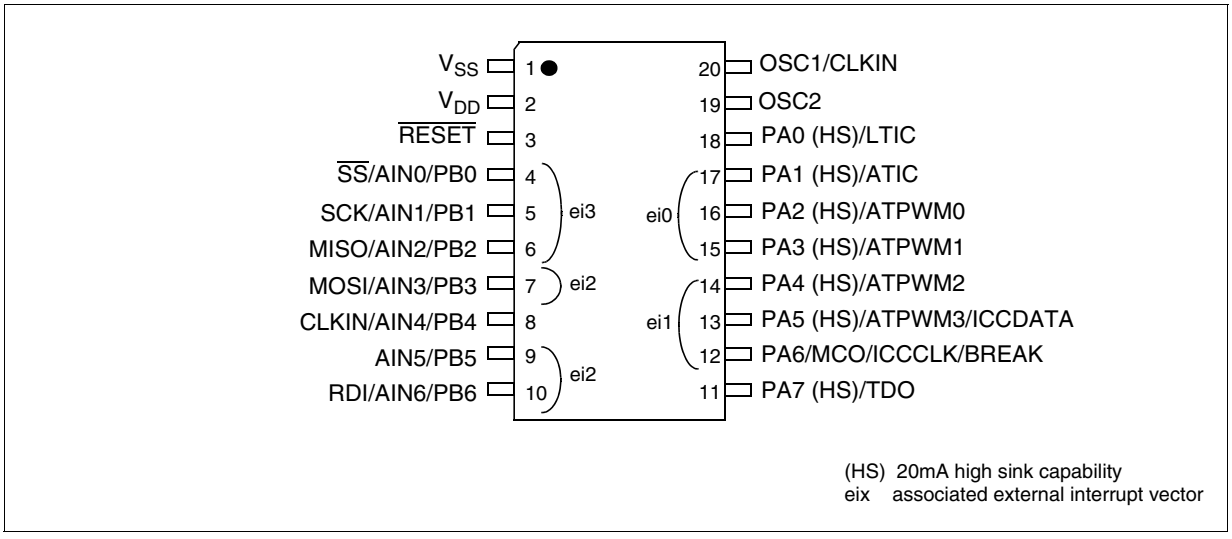


Figure 3. 20-Pin SO and DIP Package Pinout



QFN20	SO20/DIP20	Pin Name	Type	Level		Port / Control						Main Function (after reset)	Alternate Function
						Input				Output			
				Input	Output	float	wpu	int	ana	OD	PP		
10	12	PA6 /MCO/ ICCCLK/ BREAK	I/O	C_T		X	ei1			X	X	**Port A6**	Main Clock Output or In Circuit Communication Clock or External BREAK **Caution:** During normal operation this pin must be pulled- up, internally or externally (external pull-up of 10k mandatory in noisy environment). This is to avoid entering ICC mode unexpectedly during a reset. In the application, even if the pin is configured as output, any reset will put it back in input pull-up.
11	13	PA5 /ATPWM3/ ICCDATA	I/O	C_T	HS	**X**				X	X	**Port A5**	Auto-Reload Timer PWM3 or In Circuit Communication Data
12	14	PA4/ATPWM2	I/O	C_T	HS	**X**				X	X	**Port A4**	Auto-Reload Timer PWM2
13	15	PA3/ATPWM1	I/O	C_T	HS	**X**	ei0			X	X	**Port A3**	Auto-Reload Timer PWM1
14	16	PA2/ATPWM0	I/O	C_T	HS	**X**				X	X	**Port A2**	Auto-Reload Timer PWM0
15	17	PA1/ATIC	I/O	C_T	HS	**X**				X	X	**Port A1**	Auto-Reload Timer Input Capture
16	18	PA0/LTIC	I/O	C_T	HS	**X**	X			X	X	**Port A0**	Lite Timer Input Capture
17	19	OSC2	O									Resonator oscillator inverter output	
18	20	OSC1/CLKIN	I									Resonator oscillator inverter input or External clock input	

Notes:

1. It is mandatory to connect all available V_{DD} and V_{DDA} pins to the supply voltage and all V_{SS} and V_{SSA} pins to ground.

2. For input with interrupt possibility "ei_x" defines the associated external interrupt vector which can be assigned to one of the I/O pins using the EISR register. Each interrupt can be either weak pull-up or floating defined through option register OR.

6 CENTRAL PROCESSING UNIT

6.1 INTRODUCTION

This CPU has a full 8-bit architecture and contains six internal registers allowing efficient 8-bit data manipulation.

6.2 MAIN FEATURES

- 63 basic instructions
- Fast 8-bit by 8-bit multiply
- 17 main addressing modes
- Two 8-bit index registers
- 16-bit stack pointer
- Low power modes
- Maskable hardware interrupts
- Non-maskable software interrupt

6.3 CPU REGISTERS

The six CPU registers shown in Figure 10 are not present in the memory mapping and are accessed by specific instructions.

Accumulator (A)

The Accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations and to manipulate data.

Index Registers (X and Y)

In indexed addressing modes, these 8-bit registers are used to create either effective addresses or temporary storage areas for data manipulation. (The Cross-Assembler generates a precede instruction (PRE) to indicate that the following instruction refers to the Y register.)

The Y register is not affected by the interrupt automatic procedures (not pushed to and popped from the stack).

Program Counter (PC)

The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU. It is made of two 8-bit registers PCL (Program Counter Low which is the LSB) and PCH (Program Counter High which is the MSB).

Figure 10. CPU Registers

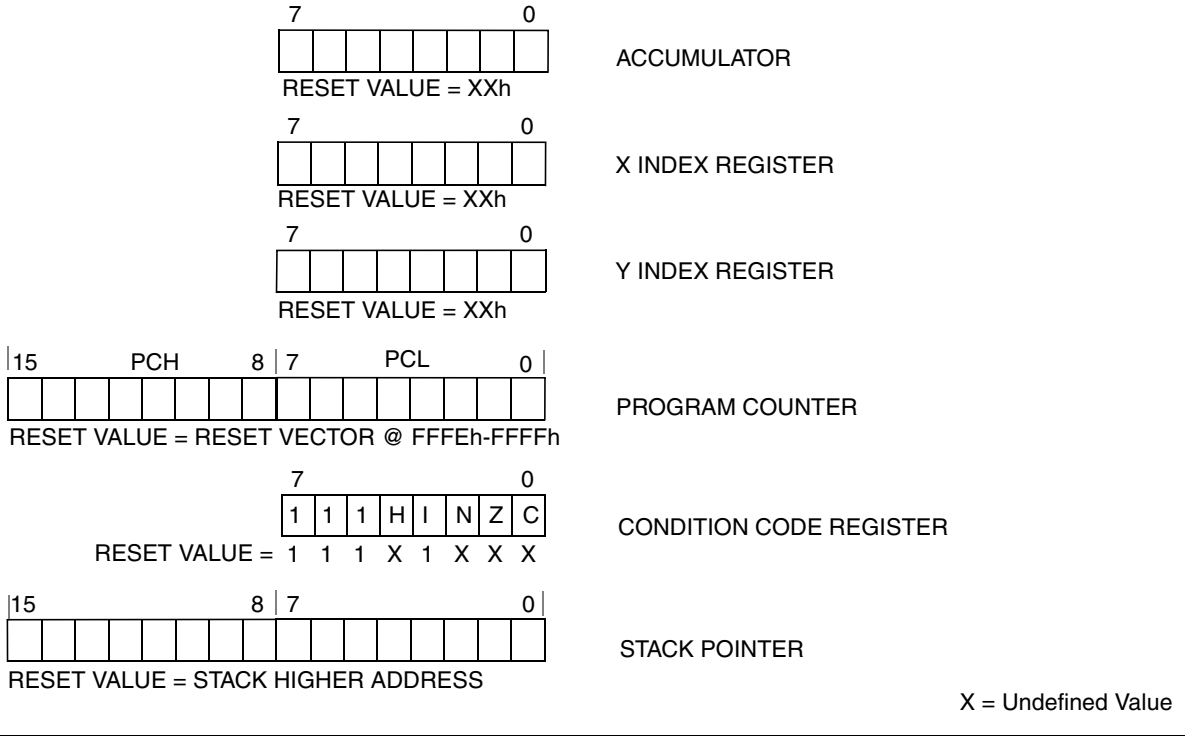
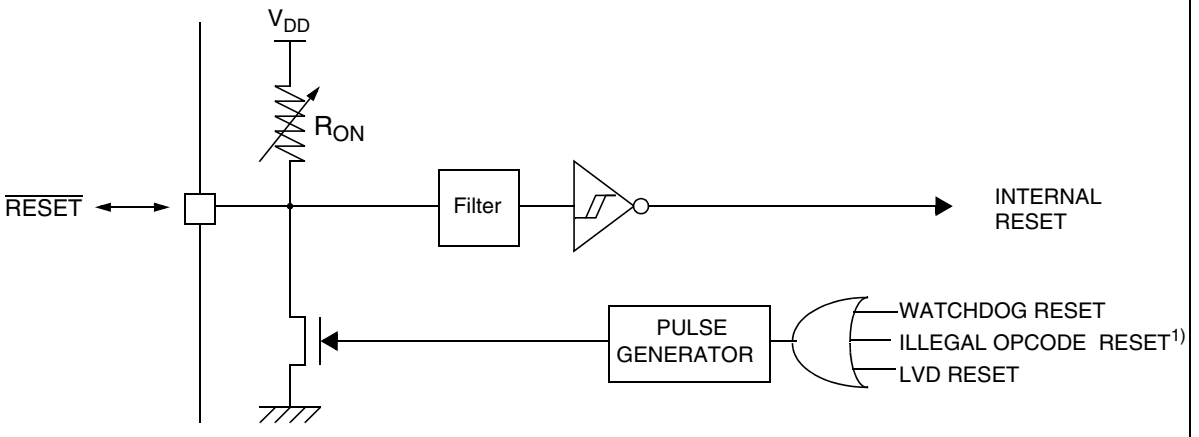


Figure 15. Reset Block Diagram



Note 1: See “Illegal Opcode Reset” on page 128. for more details on illegal opcode reset conditions.

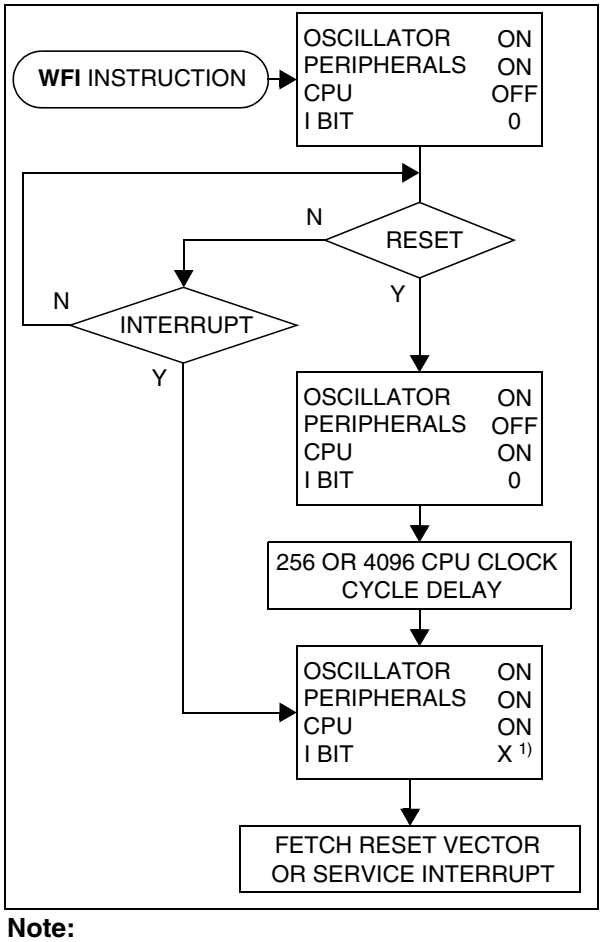
POWER SAVING MODES (Cont'd)

9.3 WAIT MODE

WAIT mode places the MCU in a low power consumption mode by stopping the CPU.
This power saving mode is selected by calling the 'WFI' instruction.
All peripherals remain active. During WAIT mode, the I bit of the CC register is cleared, to enable all interrupts. All other registers and memory remain unchanged. The MCU remains in WAIT mode until an interrupt or RESET occurs, whereupon the Program Counter branches to the starting address of the interrupt or Reset service routine.
The MCU will remain in WAIT mode until a Reset or an Interrupt occurs, causing it to wake up.

Refer to Figure 23.

Figure 23. WAIT Mode Flow-chart



Note:

1. Before servicing an interrupt, the CC register is pushed on the stack. The I bit of the CC register is set during the interrupt routine and cleared when the CC register is popped.

WATCHDOG TIMER (Cont'd)

11.1.5 Interrupts

None.

11.1.6 Register Description

CONTROL REGISTER (CR)

Read/Write

Reset Value: 0111 1111 (7Fh)

7							0
WDGA	T6	T5	T4	T3	T2	T1	T0

Bit 7 = **WDGA** *Activation bit*.
This bit is set by software and only cleared by hardware after a reset. When WDGA = 1, the watchdog can generate a reset.
0: Watchdog disabled
1: Watchdog enabled

Note: This bit is not used if the hardware watchdog option is enabled by option byte.

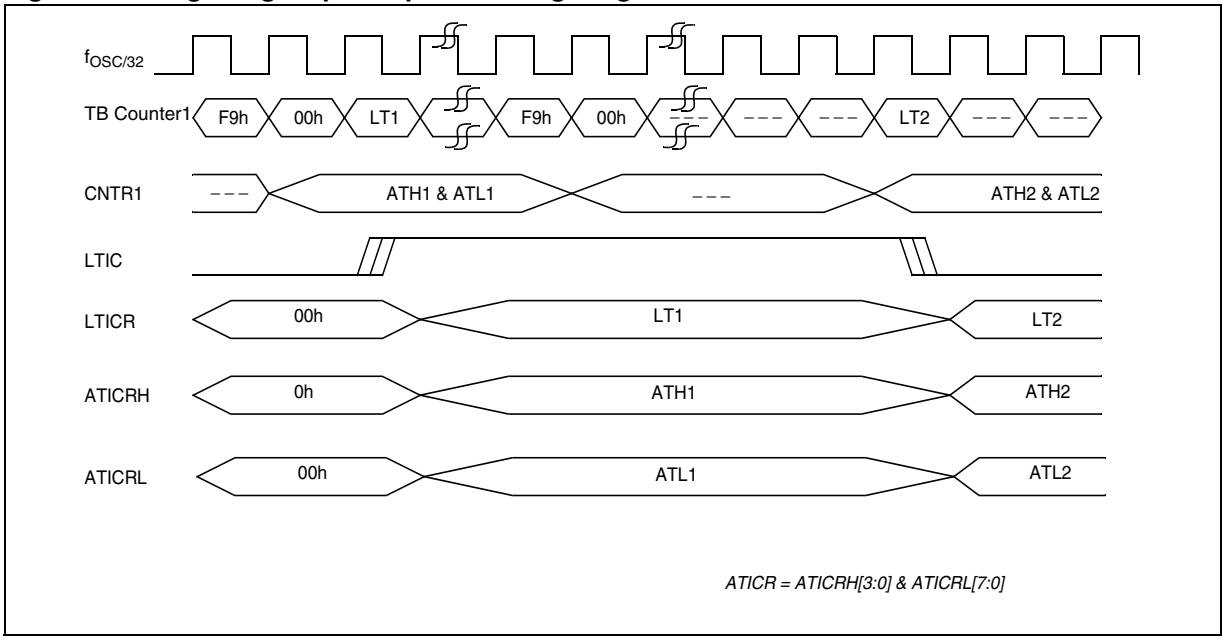
Bit 6:0 = **T[6:0]** *7-bit timer (MSB to LSB).*
These bits contain the decremented value. A reset is produced when it rolls over from 40h to 3Fh (T6 becomes cleared).

DUAL 12-BIT AUTORELOAD TIMER 3 (Cont'd)

– At the second input capture on the falling edge of the pulse, we assume that the values in the registers are as follows:
LTICR = LT2
ATICRH = ATH2
ATICRL = ATL2
Hence ATICR2 [11:0] = ATH2 & ATL2

Now pulse width P between first capture and second capture will be:
P = decimal (F9 – LT1 + LT2 + 1) * 0.004ms + decimal (ATICR2 - ATICR1 – 1) * 1ms

Figure 45. Long Range Input Capture Timing Diagram



11.2.4 Low Power Modes

Mode	Description
SLOW	The input frequency is divided by 32
WAIT	No effect on AT timer
ACTIVE-HALT	AT timer halted except if CK0=1, CK1=0 and OVFIE=1
HALT	AT timer halted.

DUAL 12-BIT AUTORELOAD TIMER 3 (Cont'd)

AUTORELOAD REGISTER (ATR1H)
Read / Write
Reset Value: 0000 0000 (00h)

15							8
0	0	0	0	ATR11	ATR10	ATR9	ATR8

AUTORELOAD REGISTER (ATR1L)
Read / Write
Reset Value: 0000 0000 (00h)

7							0
ATR7	ATR6	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0

Bits 11:0 = **ATR1[11:0]** *Autoreload Register 1.*
This is a 12-bit register which is written by software. The ATR1 register value is automatically loaded into the upcounter CNTR1 when an overflow occurs. The register value is used to set the PWM frequency.

PWM OUTPUT CONTROL REGISTER (PWMCR)
Read/Write
Reset Value: 0000 0000 (00h)

7							0
0	OE3	0	OE2	0	OE1	0	OE0

Bits 7:0 = **OE[3:0]** *PWMx output enable.*
These bits are set and cleared by software and cleared by hardware after a reset.
0: PWM mode disabled. PWMx Output Alternate Function disabled (I/O pin free for general purpose I/O)
1: PWM mode enabled

PWMx CONTROL STATUS REGISTER (PWMxCSR)
Read / Write
Reset Value: 0000 0000 (00h)

7	6						0
0	0	0	0	0	0	OPx	CMPFx

Bits 7:2= Reserved, must be kept cleared.

Bit 1 = **OPx** *PWMx Output Polarity.*
This bit is read/write by software and cleared by hardware after a reset. This bit selects the polarity of the PWM signal.
0: The PWM signal is not inverted.
1: The PWM signal is inverted.

Bit 0 = **CMPFx** PWMx *Compare Flag.*
This bit is set by hardware and cleared by software by reading the PWMxCSR register. It indicates that the upcounter value matches the Active DCRx register value.
0: Upcounter value does not match DCRx value.
1: Upcounter value matches DCRx value.

BREAK CONTROL REGISTER (BREAKCR)
Read/Write
Reset Value: 0000 0000 (00h)

7							0
0	0	BA	BPEN	PWM3	PWM2	PWM1	PWM0

Bits 7:6 = Reserved. Forced by hardware to 0.

Bit 5 = **BA** *Break Active.*
This bit is read/write by software, cleared by hardware after reset and set by hardware when the BREAK pin is low. It activates/deactivates the Break function.
0: Break not active
1: Break active

LITE TIMER (Cont'd)

11.3.4 Low Power Modes

Mode	Description
SLOW	No effect on Lite timer (this peripheral is driven directly by $f_{OSC}/32$)
WAIT	No effect on Lite timer
ACTIVE-HALT	No effect on Lite timer
HALT	Lite timer stops counting

11.3.5 Interrupts

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Active Halt	Exit from Halt
Timebase 1 Event	TB1F	TB1IE	Yes	Yes	No
Timebase 2 Event	TB2F	TB2IE	Yes	No	No
IC Event	ICF	ICIE	Yes	No	No

Note: The TBxF and ICF interrupt events are connected to separate interrupt vectors (see Interrupts chapter).

They generate an interrupt if the enable bit is set in the LTCSR1 or LTCSR2 register and the interrupt mask in the CC register is reset (RIM instruction).

11.3.6 Register Description

LITE TIMER CONTROL/STATUS REGISTER 2 (LTCSR2)
Read / Write
Reset Value: 0x00 0000 (x0h)

7							0
0	0	0	0	0	0	TB2IE	TB2F

Bits 7:2 = Reserved, must be kept cleared.

Bit 1 = **TB2IE** *Timebase 2 Interrupt enable*.
This bit is set and cleared by software.
0: Timebase (TB2) interrupt disabled
1: Timebase (TB2) interrupt enabled

Bit 0 = **TB2F** *Timebase 2 Interrupt Flag*.
This bit is set by hardware and cleared by software reading the LTCSR2 register. Writing to this bit has no effect.
0: No Counter 2 overflow
1: A Counter 2 overflow has occurred

LITE TIMER AUTORELOAD REGISTER (LTARR)
Read / Write
Reset Value: 0000 0000 (00h)

7							0
AR7	AR7	AR7	AR7	AR3	AR2	AR1	AR0

Bits 7:0 = **AR[7:0]** *Counter 2 Reload Value.*
These bits register is read/write by software. The LTARR value is automatically loaded into Counter 2 (LTCNTR) when an overflow occurs.

11.5 LINSCI SERIAL COMMUNICATION INTERFACE (LIN MASTER/SLAVE)

11.5.1 Introduction

The Serial Communications Interface (SCI) offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The SCI offers a very wide range of baud rates using two baud rate generator systems.

The LIN-dedicated features support the LIN (Local Interconnect Network) protocol for both master and slave nodes.

This chapter is divided into SCI Mode and LIN mode sections. For information on general SCI communications, refer to the SCI mode section. For LIN applications, refer to both the SCI mode and LIN mode sections.

11.5.2 SCI Features

- Full duplex, asynchronous communications
- NRZ standard format (Mark/Space)
- Independently programmable transmit and receive baud rates up to 500K baud
- Programmable data word length (8 or 9 bits)
- Receive buffer full, Transmit buffer empty and End of Transmission flags
- 2 receiver wake-up modes:
  - Address bit (MSB)
  - Idle line
- Muting function for multiprocessor configurations
- Separate enable bits for Transmitter and Receiver
- Overrun, Noise and Frame error detection
- 6 interrupt sources
  - Transmit data register empty
  - Transmission complete
  - Receive data register full
  - Idle line received
  - Overrun error
  - Parity interrupt
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Reduced power consumption mode

11.5.3 LIN Features

– LIN Master
  – 13-bit LIN Synch Break generation
– LIN Slave
  – Automatic Header Handling
  – Automatic baud rate resynchronization based on recognition and measurement of the LIN Synch Field (for LIN slave nodes)
  – Automatic baud rate adjustment (at CPU frequency precision)
  – 11-bit LIN Synch Break detection capability
  – LIN Parity check on the LIN Identifier Field (only in reception)
  – LIN Error management
  – LIN Header Timeout
  – Hot plugging support

LINSCI™ SERIAL COMMUNICATION INTERFACE (LIN Mode) (cont'd)

11.5.9.3 LIN Reception

In LIN mode the reception of a byte is the same as in SCI mode but the LINSCI has features for handling the LIN Header automatically (identifier detection) or semiautomatically (Synch Break detection) depending on the LIN Header detection mode. The detection mode is selected by the LHDM bit in the SCICR3.

Additionally, an automatic resynchronization feature can be activated to compensate for any clock deviation, for more details please refer to Section 11.5.9.5 LIN Baud Rate.

LIN Header Handling by a Slave

Depending on the LIN Header detection method the LINSCI will signal the detection of a LIN Header after the LIN Synch Break or after the Identifier has been successfully received.

Note:

It is recommended to combine the Header detection function with Mute mode. Putting the LINSCI in Mute mode allows the detection of Headers only and prevents the reception of any other characters.

This mode can be used to wait for the next Header without being interrupted by the data bytes of the current message in case this message is not relevant for the application.

Synch Break Detection (LHDM = 0):

When a LIN Synch Break is received:

– The RDRF bit in the SCISR register is set. It indicates that the content of the shift register is transferred to the SCIDR register, a value of 0x00 is expected for a Break.

– The LHDF flag in the SCICR3 register indicates that a LIN Synch Break Field has been detected.

– An interrupt is generated if the LHIE bit in the SCICR3 register is set and the I[1:0] bits are cleared in the CCR register.

– Then the LIN Synch Field is received and measured.

  – If automatic resynchronization is enabled (LASE bit = 1), the LIN Synch Field is not transferred to the shift register: There is no need to clear the RDRF bit.

  – If automatic resynchronization is disabled (LASE bit = 0), the LIN Synch Field is received as a normal character and transferred to the SCIDR register and RDRF is set.

Note:

In LIN slave mode, the FE bit detects all frame error which does not correspond to a break.

Identifier Detection (LHDM = 1):

This case is the same as the previous one except that the LHDF and the RDRF flags are set only after the entire header has been received (this is true whether automatic resynchronization is enabled or not). This indicates that the LIN Identifier is available in the SCIDR register.

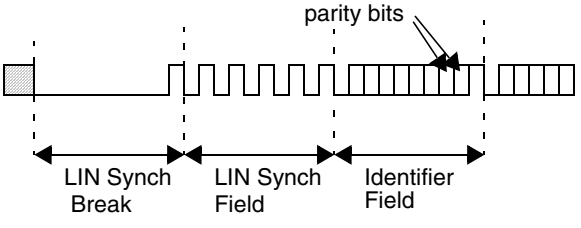
Notes:

During LIN Synch Field measurement, the SCI state machine is switched off: No characters are transferred to the data register.

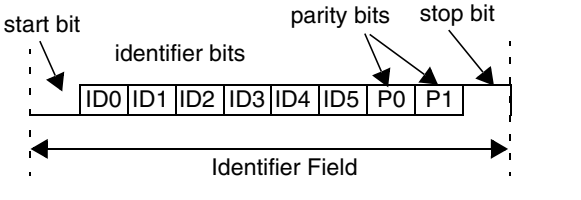
LIN Slave parity

In LIN Slave mode (LINE and LSLV bits are set) LIN parity checking can be enabled by setting the PCE bit.

In this case, the parity bits of the LIN Identifier Field are checked. The identifier character is recognized as the third received character after a break character (included):



The bits involved are the two MSB positions (7th and 8th bits if M = 0; 8th and 9th bits if M = 0) of the identifier character. The check is performed as specified by the LIN specification:



$P0 = ID0 \oplus ID1 \oplus ID2 \oplus ID4$

$P1 = \overline{ID1 \oplus ID3 \oplus ID4 \oplus ID5}$

M = 0

LINSCI™ SERIAL COMMUNICATION INTERFACE (LIN Mode) (cont'd)

SCICR2 register is set, the LHDM bit selects the Wake-Up method (replacing the WAKE bit).
0: LIN Synch Break Detection Method
1: LIN Identifier Field Detection Method

Bit 2 = **LHIE** *LIN Header Interrupt Enable*
This bit is set and cleared by software. It is only usable in LIN Slave mode.
0: LIN Header Interrupt is inhibited.
1: An SCI interrupt is generated whenever LHDF = 1.

Bit 1 = **LHDF** *LIN Header Detection Flag*
This bit is set by hardware when a LIN Header is detected and cleared by a software sequence (an access to the SCISR register followed by a read of the SCICR3 register). It is only usable in LIN Slave mode.
0: No LIN Header detected.
1: LIN Header detected.

Notes: The header detection method depends on the LHDM bit:

– If LHDM = 0, a header is detected as a LIN Synch Break.

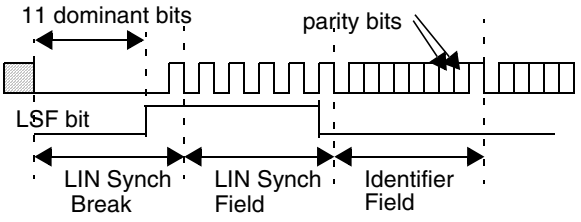
– If LHDM = 1, a header is detected as a LIN Identifier, meaning that a LIN Synch Break Field + a LIN Synch Field + a LIN Identifier Field have been consecutively received.

Bit 0 = **LSF** *LIN Synch Field State*

This bit indicates that the LIN Synch Field is being analyzed. It is only used in LIN Slave mode. In Auto Synchronization Mode (LASE bit = 1), when the SCI is in the LIN Synch Field State it waits or counts the falling edges on the RDI line.

It is set by hardware as soon as a LIN Synch Break is detected and cleared by hardware when the LIN Synch Field analysis is finished (see Figure 65). This bit can also be cleared by software to exit LIN Synch State and return to idle mode.
0: The current character is not the LIN Synch Field
1: LIN Synch Field State (LIN Synch Field undergoing analysis)

Figure 65. LSF Bit Set and Clear



LIN DIVIDER REGISTERS

LDIV is coded using the two registers LPR and LPFR. In LIN Slave mode, the LPR register is accessible at the address of the SCIBRR register and the LPFR register is accessible at the address of the SCIETPR register.

LIN PRESCALER REGISTER (LPR)

Read/Write
Reset Value: 0000 0000 (00h)

7							0
LPR7	LPR6	LPR5	LPR4	LPR3	LPR2	LPR1	LPR0

LPR[7:0] *LIN Prescaler (mantissa of LDIV)*

These 8 bits define the value of the mantissa of the LIN Divider (LDIV):

LPR[7:0]	Rounded Mantissa (LDIV)
00h	SCI clock disabled
01h	1
...	...
FEh	254
FFh	255

Caution: LPR and LPFR registers have different meanings when reading or writing to them. Consequently bit manipulation instructions (BRES or BSET) should never be used to modify the LPR[7:0] bits, or the LPFR[3:0] bits.

Table 22. ADC Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0034h	**ADCCSR**	EOC	SPEED	ADON	0	0	CH2	CH1	CH0
	Reset Value	0	0	0	0	0	0	0	0
0035h	**ADCDRH**	D9	D8	D7	D6	D5	D4	D3	D2
	Reset Value	0	0	0	0	0	0	0	0
0036h	**ADCDRL**	0	0	0	0	SLOW	0	D1	D0
	Reset Value	0	0	0	0	0	0	0	0

OPERATING CONDITIONS (Cont'd)

Figure 70. Typical accuracy with RCCR=RCCR0 vs V_{DD}= 4.5 to 5.5V and Temperature

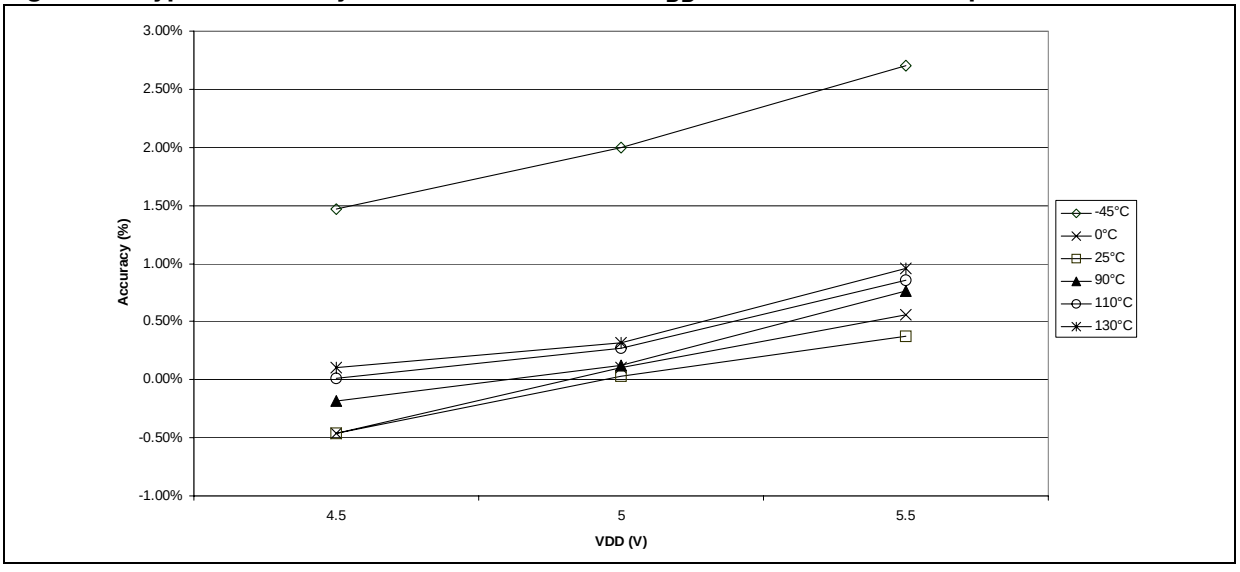
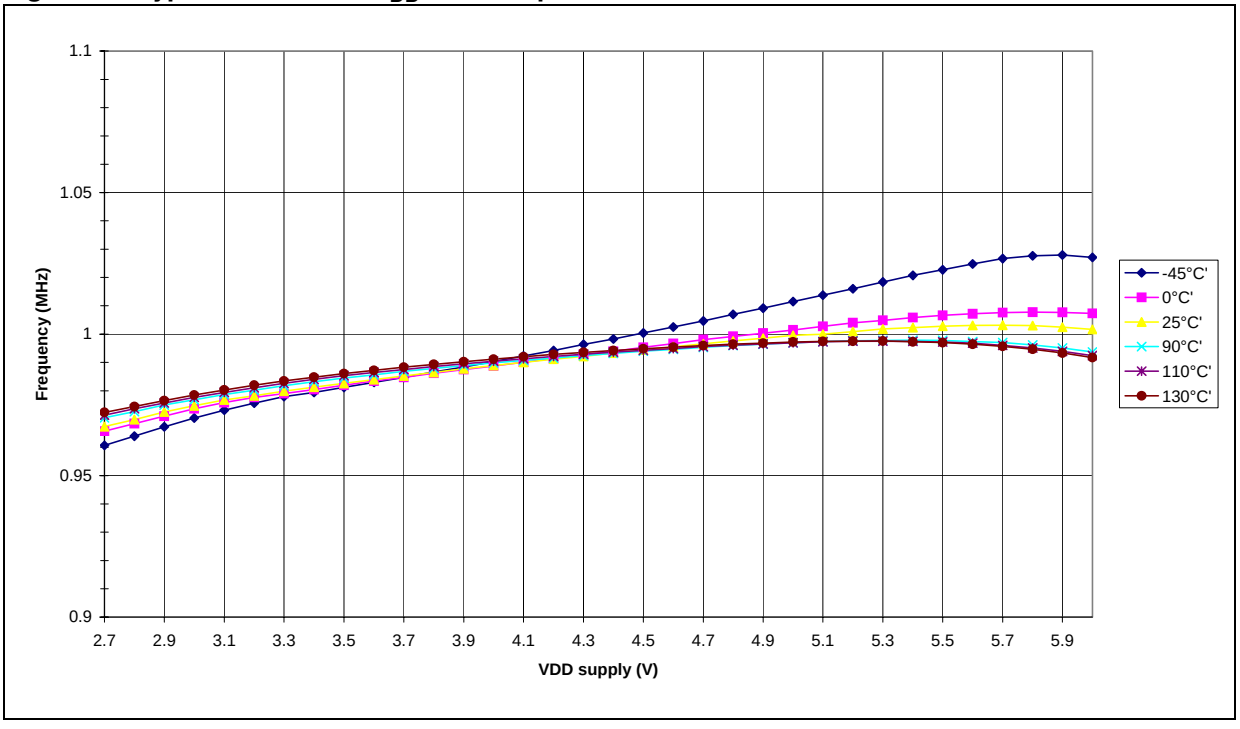


Figure 71. Typical RCCR0 vs V_{DD} and Temperature



driven by external square wave, LVD disabled.

3. SLOW mode selected with f_{CPU} based on f_{OSC} divided by 32. All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load), all peripherals in reset state; clock input (CLKIN) driven by external square wave, LVD disabled.

4. SLOW-WAIT mode selected with f_{CPU} based on f_{OSC} divided by 32. All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load), all peripherals in reset state; clock input (CLKIN) driven by external square wave, LVD disabled.

5. All I/O pins in output mode with a static value at V_{SS} (no load), LVD disabled. Data based on characterization results, tested in production at V_{DD} max and f_{CPU} max.

6. All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load). Data tested in production at V_{DD} max. and f_{CPU} max.

7. This consumption refers to the Halt period only and not the associated run period which is software dependent.

Figure 77. Typical I_{DD} in RUN vs. f_{CPU}

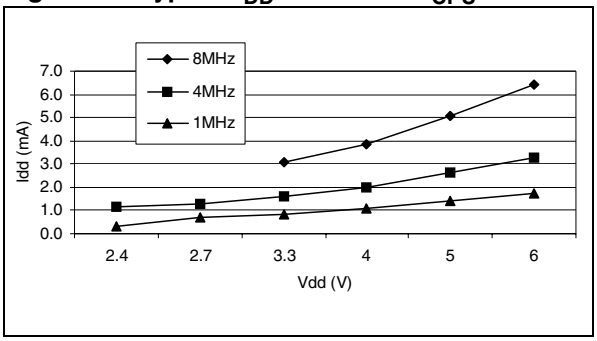
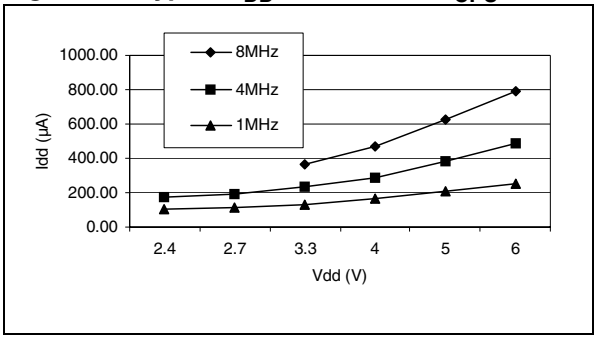


Figure 78. Typical I_{DD} in SLOW vs. f_{CPU}



SUPPLY CURRENT CHARACTERISTICS (Cont'd)

Figure 79. Typical I_{DD} in WAIT vs. f_{CPU}

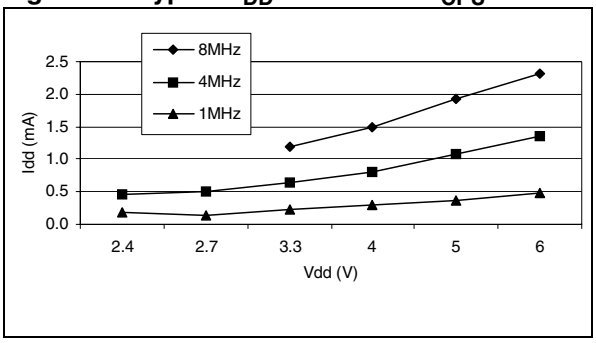


Figure 80. Typical I_{DD} in SLOW-WAIT vs. f_{CPU}

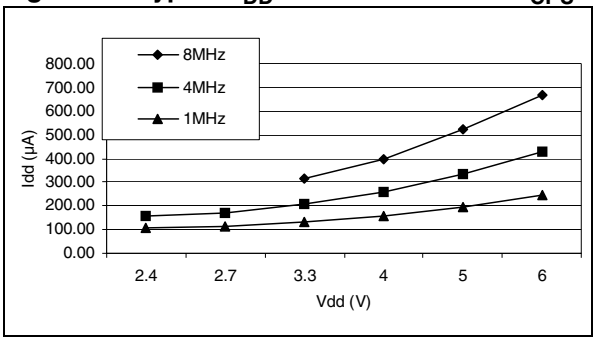


Figure 81. Typical I_{DD} vs. Temperature at V_{DD} = 5V and f_{OSC} = 16MHz

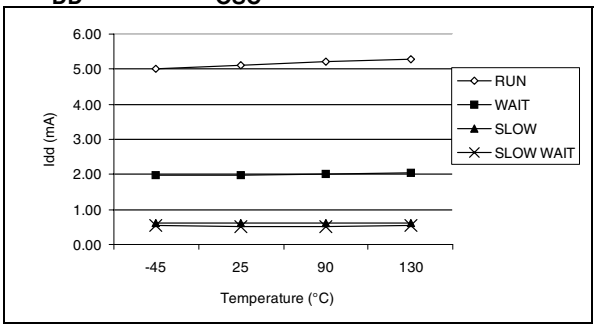
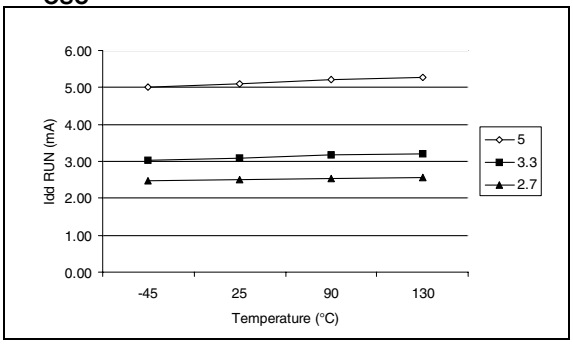


Figure 82. Typical I_{DD} vs. Temperature and V_{DD} at f_{OSC} = 16MHz



13.4.2 On-chip peripherals

Symbol	Parameter	Conditions		Typ	Unit
$I_{DD(AT)}$	12-bit Auto-Reload Timer supply current [1]	f_{CPU}=4MHz	V_{DD}=3.0V	150	µA
		f_{CPU}=8MHz	V_{DD}=5.0V	1000	
$I_{DD(SPI)}$	SPI supply current [2]	f_{CPU}=4MHz	V_{DD}=3.0V	50	
		f_{CPU}=8MHz	V_{DD}=5.0V	200	
$I_{DD(ADC)}$	ADC supply current when converting [3]	f_{ADC}=4MHz	V_{DD}=3.0V	250	
			V_{DD}=5.0V	1100	
$I_{DD(LINSCI)}$	LINSCI supply current when transmitting [4]	f_{CPU}=8MHz	V_{DD}=5.0V	650	

1. Data based on a differential I_{DD} measurement between reset configuration (timer stopped) and a timer running in PWM mode at f_{cpu}=8MHz.

2. Data based on a differential I_{DD} measurement between reset configuration and a permanent SPI master communication (data sent equal to 55h).

3. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

4. Data based on a differential I_{DD} measurement between LINSCI running at maximum speed configuration (500 kbaud, continuous transmission of AA +RE enabled and LINSCI off. This measurement includes the pad toggling consumption.

13.5 CLOCK AND TIMING CHARACTERISTICS

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A.

13.5.1 General Timings

Symbol	Parameter [1]	Conditions	Min	Typ [2]	Max	Unit
$t_{c(INST)}$	Instruction cycle time	f_{CPU}=8MHz	2	3	12	t_{CPU}
			250	375	1500	ns
$t_{v(IT)}$	Interrupt reaction time [3] $t_{v(IT)} = \Delta t_{c(INST)} + 10$	f_{CPU}=8MHz	10		22	t_{CPU}
			1.25		2.75	µs

13.5.2 External Clock Source

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OSC1H} or V_{CLKIN_H}	OSC1/CLKIN input pin high level voltage	see Figure 83	0.7xV_{DD}		V_{DD}	V
V_{OSC1L} or V_{CLKIN_L}	OSC1/CLKIN input pin low level voltage		V_{SS}		0.3xV_{DD}	
$t_{w(OSC1H)}$ or $t_{w(CLKINH)}$ $t_{w(OSC1L)}$ or $t_{w(CLKINL)}$	OSC1/CLKIN high or low time [4]		15			ns
$t_{r(OSC1)}$ or $t_{r(CLKIN)}$ $t_{f(OSC1)}$ or $t_{f(CLKIN)}$	OSC1/CLKIN rise or fall time [4]				15	
I_L	OSCx/CLKIN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA

Notes:

1. Guaranteed by Design. Not tested in production.

2. Data based on typical application software.

3. Time measured between interrupt event and interrupt vector fetch. $\Delta t_{c(INST)}$ is the number of t_{CPU} cycles needed to finish the current instruction execution.

4. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 83. Typical Application with an External Clock Source

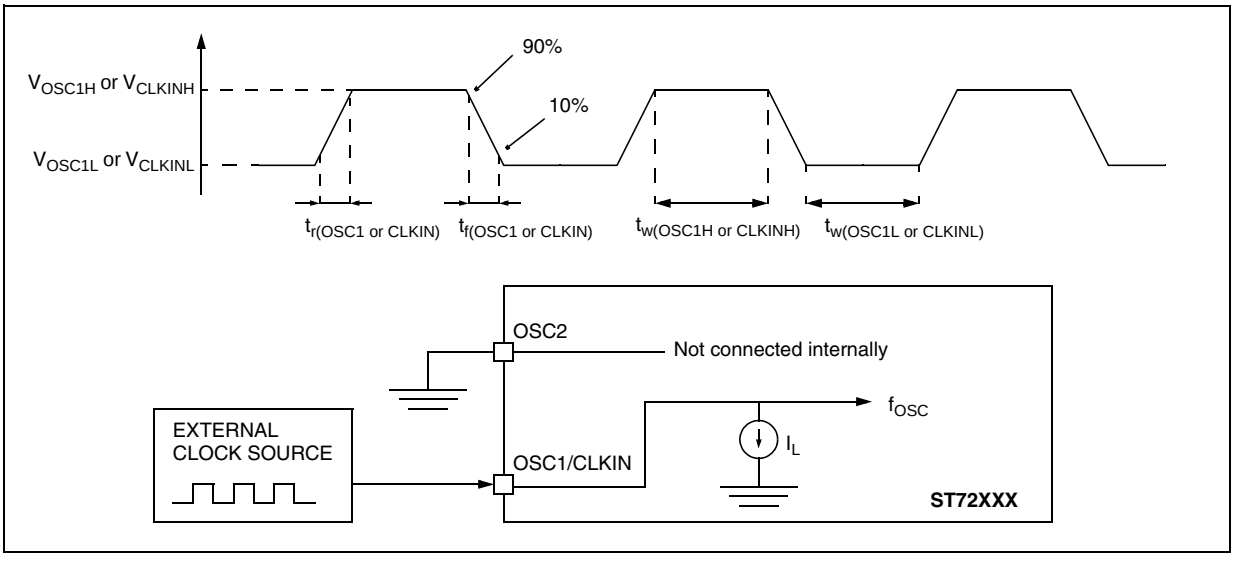
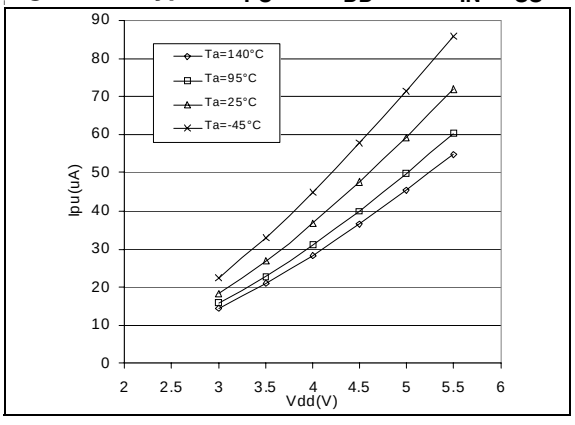


Figure 85. Typical I_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$



15 DEVICE CONFIGURATION

Each device is available for production in user programmable versions (FLASH) as well as in factory coded versions (ROM/FASTROM).

ST7PLITE3 devices are Factory Advanced Service Technique ROM (FASTROM) versions: they are factory programmed FLASH devices.

ST7FLITE3 devices are shipped to customers with a default program memory content (FFh), while FASTROM factory coded parts contain the code supplied by the customer. This implies that FLASH devices have to be configured by the customer using the Option Bytes.

15.1 FLASH OPTION BYTES

The two option bytes allow the hardware configuration of the microcontroller to be selected.

OPTION BYTE 0

OPT7 = **AWUCK** *Auto Wake Up Clock Selection*

0: 32-KHz Oscillator (VLP) selected as AWU clock

.

1: AWU RC Oscillator selected as AWU clock.

Note: If this bit is reset, internal RC oscillator must be selected (Option OSC=0).

OPT6:4 = **OSCRANGE[2:0]** *Oscillator Range*
When the internal RC oscillator is not selected (Option OSC=1), these option bits select the range of the resonator oscillator current source or the external clock source.

			OSCRANGE		
			2	**1**	**0**
Typ. frequency range with Resonator	LP	1~2MHz	0	0	0
	MP	2~4MHz	0	0	1
	MS	4~8MHz	0	1	0
	HS	8~16MHz	0	1	1
	VLP	32.768kHz	1	0	0
External Clock on OSC1			1	0	1
Reserved			1	1	0
External Clock on PB4			1	1	1

Notes:

1. OSCRANGE[2:0] has no effect when AWUCK option is set to 0. In this case, the VLP oscillator range is automatically selected as AWU clock.

2. When the internal RC oscillator is selected, the OSCRANGE option bits must be kept at their default value to select the 256 clock cycle delay (see section 7.5 on page 27)

OPT 3:2 = **SEC[1:0]** *Sector 0 size definition*
These option bits indicate the size of sector 0 according to the following table.

Sector 0 Size	SEC1	SEC0
0.5k	0	0
1k	0	1
2	1	0
4k	1	1

OPT1 = **FMP_R** *Read-out protection*
Readout protection, when selected provides a protection against program memory content extraction and against write access to Flash memory. Erasing the option bytes when the FMP_R option is selected will cause the whole memory to be erased first and the device can be reprogrammed. Refer to the ST7 Flash Programming Reference Manual and section 4.5 on page 14 for more details
0: Read-out protection off
1: Read-out protection on

OPT 0 = **FMP_W** *FLASH write protection*
This option indicates if the FLASH program memory is write protected.
Warning: When this option is selected, the program memory (and the option bit itself) can never be erased or programmed again.
0: Write protection off
1: Write protection on
The option bytes have no address in the memory map and can be accessed only in programming mode (for example using a standard ST7 programming tool). The default content of the FLASH is fixed to FFh.

ST7LITE3xF2 FASTROM MICROCONTROLLER OPTION LIST
(Last update: November 2007)

Customer . . . . . .
Address . . . . . .
. . . . . .
Contact . . . . . .
Phone No . . . . . .
Reference FASTROM Code*: . . . . . .
*FASTROM code name is assigned by STMicroelectronics.
FASTROM code must be sent in .S19 format. .Hex extension cannot be processed.

Device type: [ ] ST7PLITE30F2 [ ] ST7PLITE35F2 [ ] ST7PLITE39F2

Conditioning (check only one option):
PDIP20: [ ] Tube
SO20: [ ] Tape & Reel [ ] Tube
QFN20: [ ] Tape & Reel [ ] Tray

Special Marking: [ ] No [ ] Yes "_ _ _ _ _ _ _ _ "
Authorized characters are letters, digits, '.', '-', '/' and spaces only.
Maximum character count: 8 char. max

Temperature range [ ] - 40°C to + 85°C [ ] - 40°C to + 125°C

AWUCK Selection [ ] 32-kHz Oscillator [ ] AWU RC Oscillator

Clock Source Selection:
[ ] Resonator:
[ ] VLP: Very Low power resonator (32 to 100 kHz)
[ ] LP: Low power resonator (1 to 2 MHz)
[ ] MP: Medium power resonator (2 to 4 MHz)
[ ] MS: Medium speed resonator (4 to 8 MHz)
[ ] HS: High speed resonator (8 to 16 MHz)
[ ] External Clock
[ ] on PB4
[ ] on OSC1
[ ] Internal RC Oscillator

Sector 0 size: [ ] 0.5K [ ] 1K [ ] 2K [ ] 4K

Readout Protection: [ ] Disabled [ ] Enabled

FLASH Write Protection [ ] Disabled [ ] Enabled

PLL [ ] Disabled [ ] PLLx4 [ ] PLLx8

LVD Reset [ ] Disabled [ ] Highest threshold
[ ] Medium threshold
[ ] Lowest threshold

Watchdog Selection: [ ] Software Activation [ ] Hardware Activation

Watchdog Reset on Halt: [ ] Disabled [ ] Enabled

Comments : . . . . . .
Supply Operating Range in the application: . . . . . .
Notes . . . . . .
Date: . . . . . .
Signature: . . . . . .

Important note: Not all configurations are available.
Refer to Figure 108.Ordering information scheme.
Please contact the ST Sales Office nearest to you for any further information.

Please download the latest version of this option list from:
www.st.com