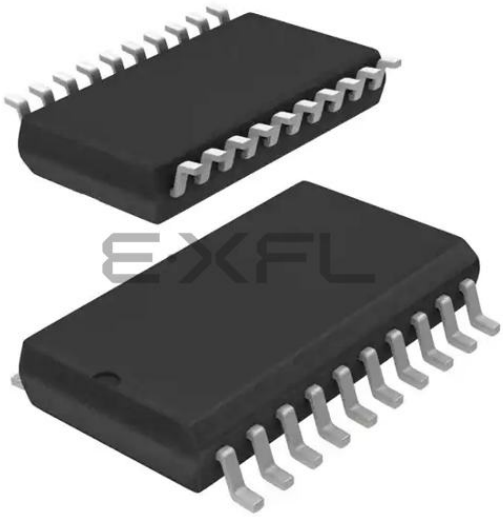

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ST7 |
| Core Size | 8-Bit |
| Speed | 16MHz |
| Connectivity | LINbusSCI, SPI |
| Peripherals | LVD, POR, PWM, WDT |
| Number of I/O | 15 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 384 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 7x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 20-SO |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/st7flite35f2m3 |

**PIN DESCRIPTION** (Cont'd)

**Legend / Abbreviations for Table 2:**

Type: I = input, O = output, S = supply

In/Output level: $C_T$= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Output level: HS = 20mA high sink (on N-buffer only)

Port and control configuration:

- Input: float = floating, wpu = weak pull-up, int = interrupt, ana = analog
- Output: OD = open drain, PP = push-pull

The RESET configuration of each pin is shown in bold which is valid as long as the device is in reset state.

**Table 2. Device Pin Description**

| | | | | Level | | Port / Control | | | | | | Main Function (after reset) | Alternate Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Input | | | | Output | | | |
| QFN20 | SO20/DIP20 | Pin Name | Type | Input | Output | float | wpu | int | ana | OD | PP | | |
| 19 | 1 | $V_{SS}$ [1] | S | | | | | | | | | Ground | |
| 20 | 2 | $V_{DD}$ [1] | S | | | | | | | | | Main power supply | |
| 1 | 3 | $\overline{\text{RESET}}$ | I/O | $C_T$ | | | X | | | X | | Top priority non maskable interrupt (active low) | |
| 2 | 4 | PB0/AIN0/$\overline{\text{SS}}$ | I/O | $C_T$ | | **X** | ei3 | | X | X | X | **Port B0** | ADC Analog Input 0 or SPI Slave Select (active low) **Caution:** No negative current injection allowed on this pin. For details, refer to section 13.2.2 on page 132 |
| 3 | 5 | PB1/AIN1/SCK | I/O | $C_T$ | | **X** | | | X | X | X | **Port B1** | ADC Analog Input 1 or SPI Serial Clock **Caution:** No negative current injection allowed on this pin. For details, refer to section 13.2.2 on page 132 |
| 4 | 6 | PB2/AIN2/ MISO | I/O | $C_T$ | | **X** | | | X | X | X | **Port B2** | ADC Analog Input 2 or SPI Master In/ Slave Out Data |
| 5 | 7 | PB3/AIN3/ MOSI | I/O | $C_T$ | | **X** | ei2 | | X | X | X | **Port B3** | ADC Analog Input 3 or SPI Master Out / Slave In Data |
| 6 | 8 | PB4/AIN4/ CLKIN** | I/O | $C_T$ | | **X** | X | | X | X | X | **Port B4** | ADC Analog Input 4 or External clock input |
| 7 | 9 | PB5/AIN5 | I/O | $C_T$ | | **X** | ei2 | | X | X | X | **Port B5** | ADC Analog Input 5 |
| 8 | 10 | PB6/AIN6/RDI | I/O | $C_T$ | | **X** | | | X | X | X | **Port B6** | ADC Analog Input 6 or LINSCI Input |
| 9 | 11 | PA7/TDO | I/O | $C_T$ | HS | **X** | X | | | X | X | **Port A7** | LINSCI Output |

# 3 REGISTER & MEMORY MAP

As shown in Figure 4, the MCU is capable of addressing 64K bytes of memories and I/O registers.

The available memory locations consist of 128 bytes of register locations, 384 bytes of RAM, 256 bytes of data EEPROM and 8 Kbytes of user program memory. The RAM space includes up to 128 bytes for the stack from 180h to 1FFh.

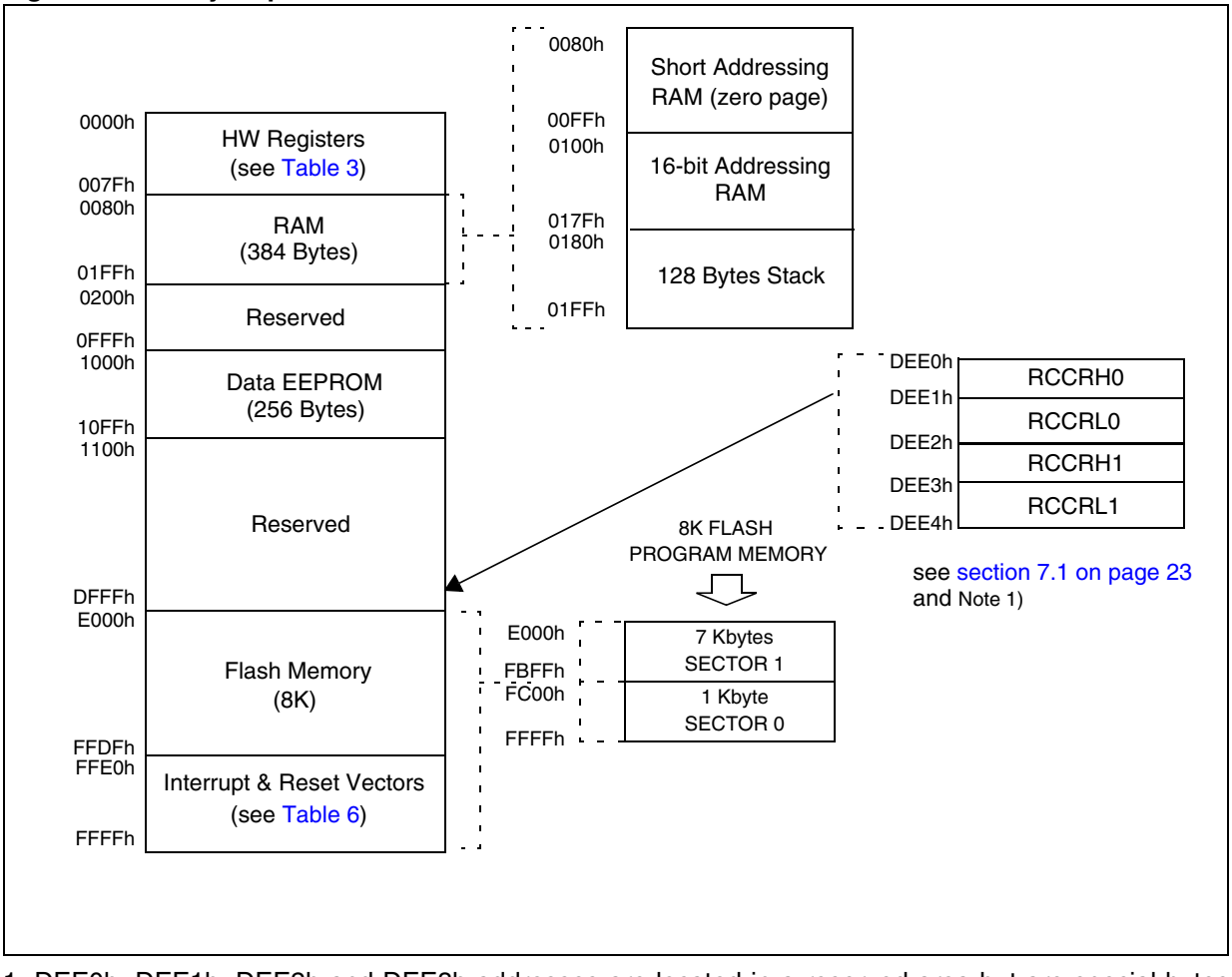
The highest address bytes contain the user reset and interrupt vectors.

The Flash memory contains two sectors (see Figure 4) mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (F000h-FFFFh).

The size of Flash Sector 0 and other device options are configurable by Option byte.

**IMPORTANT:** Memory locations marked as "Reserved" must never be accessed. Accessing a reseved area can have unpredictable effects on the device.

**Figure 4. Memory Map**




1. DEE0h, DEE1h, DEE2h and DEE3h addresses are located in a reserved area but are special bytes containing also the RC calibration values which are read-accessible only in user mode. If all the EEPROM data or Flash space (including the RC calibration values locations) has been erased (after the read out protection removal), then the RC calibration values can still be obtained through these addresses.

# 4 FLASH PROGRAM MEMORY

## 4.1 Introduction

The ST7 single voltage extended Flash (XFlash) is a non-volatile memory that can be electrically erased and programmed either on a byte-by-byte basis or up to 32 bytes in parallel.

The XFlash devices can be programmed off-board (plugged in a programming tool) or on-board using In-Circuit Programming or In-Application Programming.

The array matrix organisation allows each sector to be erased and reprogrammed without affecting other sectors.

## 4.2 Main Features

- ICP (In-Circuit Programming)
- IAP (In-Application Programming)
- ICT (In-Circuit Testing) for downloading and executing user application test patterns in RAM
- Sector 0 size configurable by option byte
- Read-out and write protection

## 4.3 PROGRAMMING MODES

The ST7 can be programmed in three different ways:

– Insertion in a programming tool. In this mode, FLASH sectors 0 and 1, option byte row and data EEPROM (if present) can be programmed or erased.

– In-Circuit Programming. In this mode, FLASH sectors 0 and 1, option byte row and data EEPROM (if present) can be programmed or erased without removing the device from the application board.

– In-Application Programming. In this mode, sector 1 and data EEPROM (if present) can be programmed or erased without removing the device from the application board and while the application is running.

### 4.3.1 In-Circuit Programming (ICP)

ICP uses a protocol called ICC (In-Circuit Communication) which allows an ST7 plugged on a printed circuit board (PCB) to communicate with an external programming device connected via cable. ICP is performed in three steps:

Switch the ST7 to ICC mode (In-Circuit Communications). This is done by driving a specific signal sequence on the ICCCLK/DATA pins while the RESET pin is pulled low. When the ST7 enters ICC mode, it fetches a specific RESET vector which points to the ST7 System Memory containing the ICC protocol routine. This routine enables the ST7 to receive bytes from the ICC interface.

– Download ICP Driver code in RAM from the ICCDATA pin

– Execute ICP Driver code in RAM to program the FLASH memory

Depending on the ICP Driver code downloaded in RAM, FLASH memory programming can be fully customized (number of bytes to program, program locations, or selection of the serial communication interface for downloading).

### 4.3.2 In Application Programming (IAP)

This mode uses an IAP Driver program previously programmed in Sector 0 by the user (in ICP mode).

This mode is fully controlled by user software. This allows it to be adapted to the user application, (user-defined strategy for entering programming mode, choice of communications protocol used to fetch the data to be stored etc.)
IAP mode can be used to program any memory areas except Sector 0, which is write/erase protected to allow recovery in case errors occur during the programming operation.

**DATA EEPROM** (Cont'd)

### 5.4 POWER SAVING MODES

#### Wait mode

The DATA EEPROM can enter WAIT mode on execution of the WFI instruction of the microcontroller or when the microcontroller enters Active-HALT mode.The DATA EEPROM will immediately enter this mode if there is no programming in progress, otherwise the DATA EEPROM will finish the cycle and then enter WAIT mode.

#### Active-Halt mode

Refer to Wait mode.

#### Halt mode

The DATA EEPROM immediately enters HALT mode if the microcontroller executes the HALT instruction. Therefore the EEPROM will stop the function in progress, and data may be corrupted.

### 5.5 ACCESS ERROR HANDLING

If a read access occurs while E2LAT=1, then the data bus will not be driven.

If a write access occurs while E2LAT=0, then the data on the bus will not be latched.

If a programming cycle is interrupted (by RESET action), the integrity of the data in memory is not guaranteed.

### 5.6 Data EEPROM Read-out Protection

The read-out protection is enabled through an option bit (see section 15.1 on page 161).

When this option is selected, the programs and data stored in the EEPROM memory are protected against read-out (including a re-write protection). In Flash devices, when this protection is removed by reprogramming the Option Byte, the entire Program memory and EEPROM is first automatically erased.

**Note:** Both Program Memory and data EEPROM are protected using the same option bit.

**Figure 9. Data EEPROM Programming Cycle**

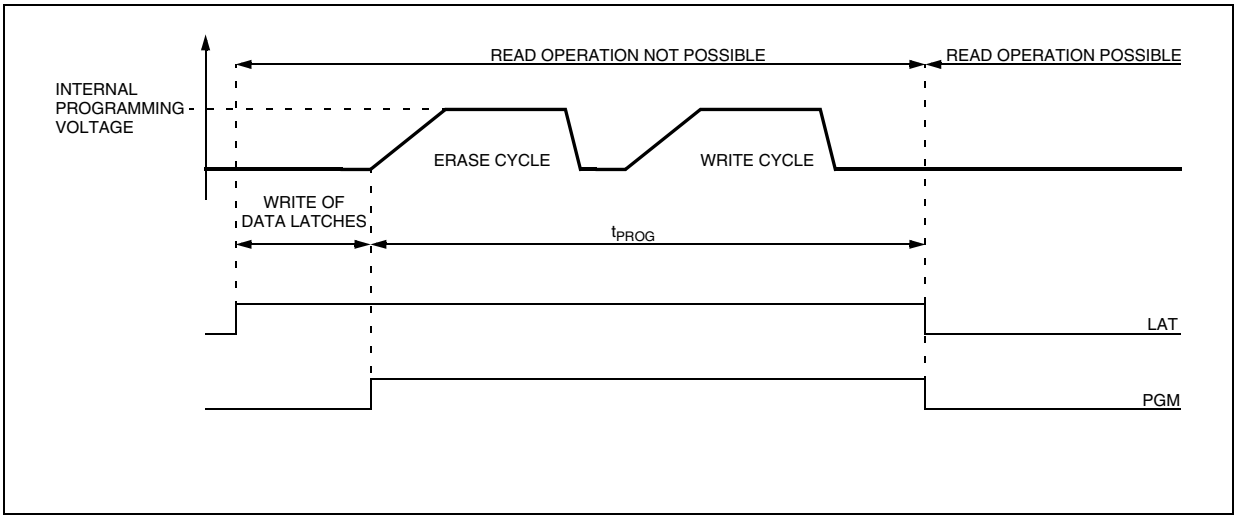
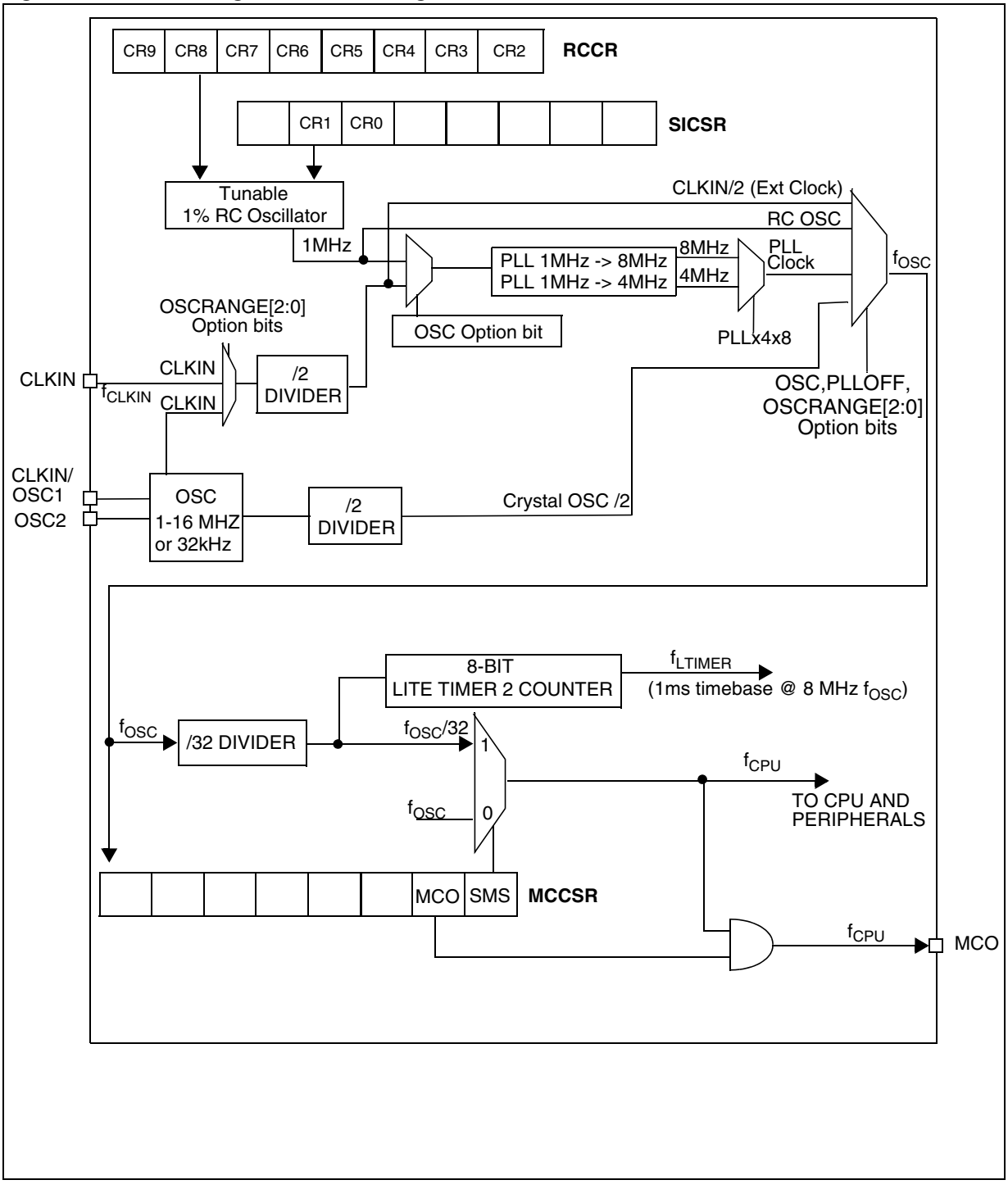


**Figure 13. Clock Management Block Diagram**



**INTERRUPTS** (Cont'd)

### EXTERNAL INTERRUPT CONTROL REGISTER (EICR)

Read/Write

Reset Value: 0000 0000 (00h)

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| IS31 | IS30 | IS21 | IS20 | IS11 | IS10 | IS01 | IS00 |

Bit 7:6 = **IS3[1:0]** *ei3 sensitivity*
These bits define the interrupt sensitivity for ei3 (Port B0) according to Table 7.

Bit 5:4 = **IS2[1:0]** *ei2 sensitivity*
These bits define the interrupt sensitivity for ei2 (Port B3) according to Table 7.

Bit 3:2 = **IS1[1:0]** *ei1 sensitivity*
These bits define the interrupt sensitivity for ei1 (Port A7) according to Table 7.

Bit 1:0 = **IS0[1:0]** *ei0 sensitivity*
These bits define the interrupt sensitivity for ei0 (Port A0) according to Table 7.

**Note:** These 8 bits can be written only when the I bit in the CC register is set.

**Table 7. Interrupt Sensitivity Bits**

| ISx1 | ISx0 | External Interrupt Sensitivity |
|---|---|---|
| 0 | 0 | Falling edge & low level |
| 0 | 1 | Rising edge only |
| 1 | 0 | Falling edge only |
| 1 | 1 | Rising and falling edge |

.

### EXTERNAL INTERRUPT SELECTION REGISTER (EISR)

Read/Write

Reset Value: 0000 0000 (00h)

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| ei31 | ei30 | ei21 | ei20 | ei11 | ei10 | ei01 | ei00 |

Bit 7:6 = **ei3[1:0]** *ei3 pin selection*
These bits are written by software. They select the Port B I/O pin used for the ei3 external interrupt according to the table below.

**External Interrupt I/O pin selection**

| ei31 | ei30 | I/O Pin |
|---|---|---|
| 0 | 0 | No interrupt * |
| 0 | 1 | PB0 |
| 1 | 0 | PB1 |
| 1 | 1 | PB2 |

* Reset State

Bit 5:4 = **ei2[1:0]** *ei2 pin selection*
These bits are written by software. They select the Port B I/O pin used for the ei2 external interrupt according to the table below.

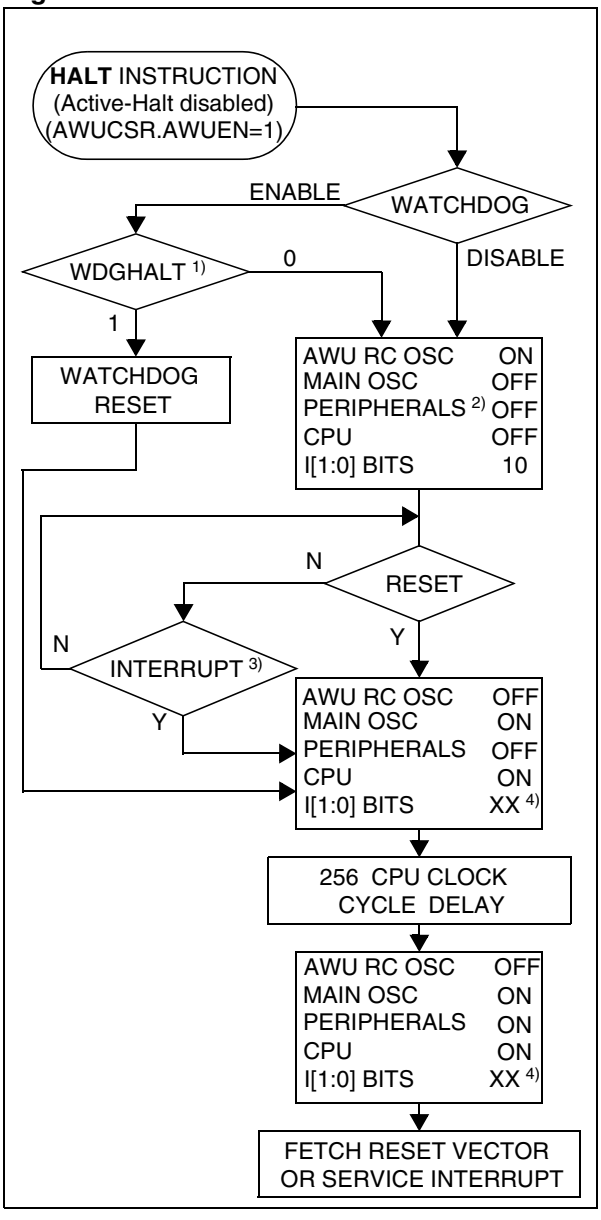
**External Interrupt I/O pin selection**

| ei21 | ei20 | I/O Pin |
|---|---|---|
| 0 | 0 | No interrupt * |
| 0 | 1 | PB3 |
| 1 | 0 | PB5 |
| 1 | 1 | PB6 |

* Reset State

**POWER SAVING MODES** (Cont'd)

**Figure 30. AWUFH Mode Flow-chart**




**Notes:**

**1.** WDGHALT is an option bit. See option byte section for more details.

**2.** Peripheral clocked with an external clock source can still be active.

**3.** Only an AWUFH interrupt and some specific interrupts can exit the MCU from HALT mode (such as external interrupt). Refer to Table 6, "Interrupt Mapping," on page 36 for more details.

**4.** Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.

## 11.3 LITE TIMER 2 (LT2)

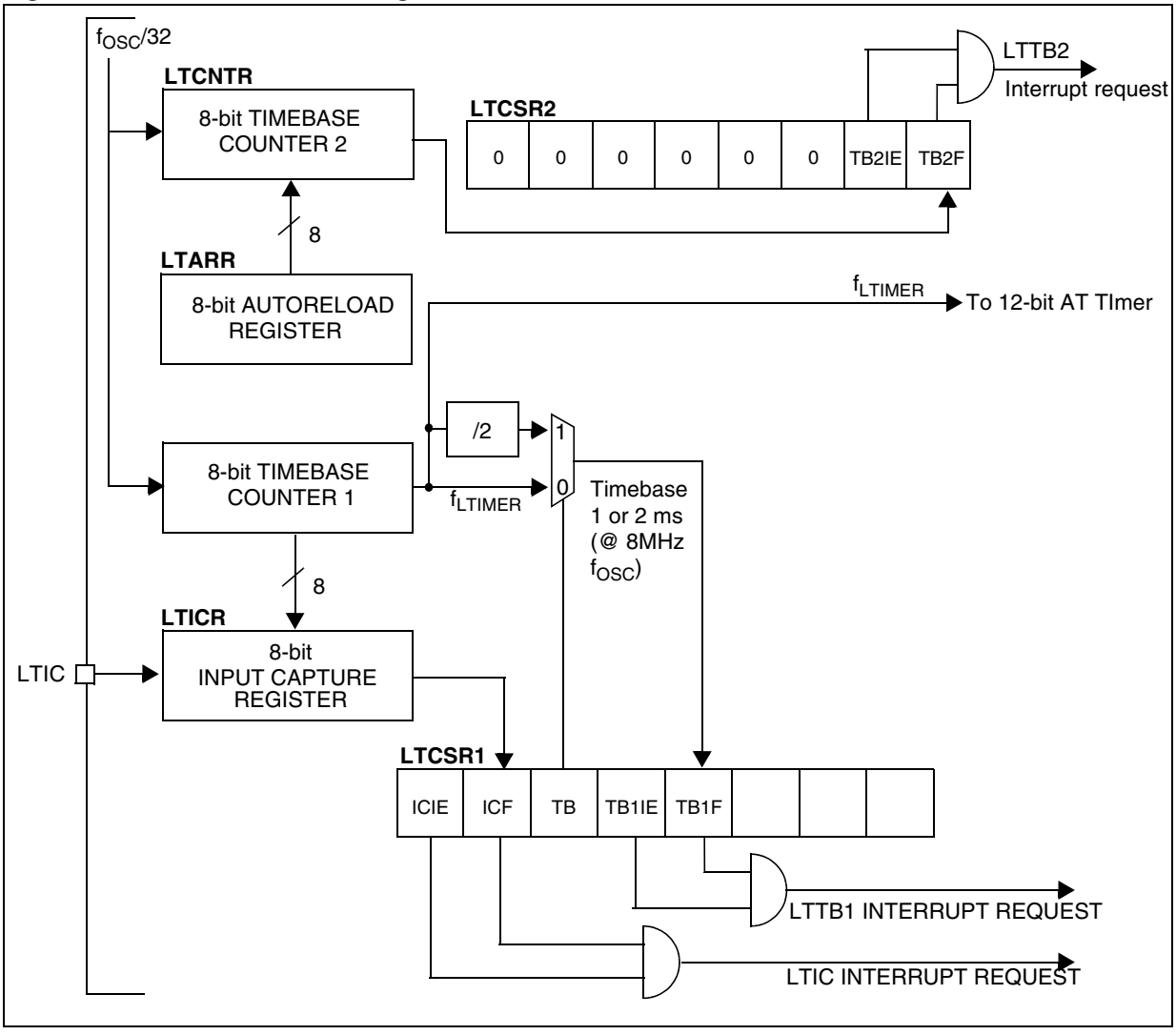
### 11.3.1 Introduction

The Lite Timer can be used for general-purpose timing functions. It is based on two free-running 8-bit upcounters and an 8-bit input capture register.

### 11.3.2 Main Features

- Realtime Clock (RTC)
  - One 8-bit upcounter 1 ms or 2 ms timebase period (@ 8 MHz $f_{OSC}$)
  - One 8-bit upcounter with autoreload and programmable timebase period from 4µs to 1.024ms in 4µs increments (@ 8 MHz $f_{OSC}$)
  - 2 Maskable timebase interrupts
- Input Capture
  - 8-bit input capture register (LTICR)
  - Maskable interrupt with wakeup from Halt Mode capability

**Figure 46. Lite Timer 2 Block Diagram**



**LITE TIMER** (Cont'd)

**Table 17. Lite Timer Register Map and Reset Values**

| Address (Hex.) | Register Label | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| 08 | **LTCSR2** Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | TB2IE 0 | TB2F 0 |
| 09 | **LTARR** Reset Value | AR7 0 | AR6 0 | AR5 0 | AR4 0 | AR3 0 | AR2 0 | AR1 0 | AR0 0 |
| 0A | **LTCNTR** Reset Value | CNT7 0 | CNT6 0 | CNT5 0 | CNT4 0 | CNT3 0 | CNT2 0 | CNT1 0 | CNT0 0 |
| 0B | **LTCSR1** Reset Value | ICIE 0 | ICF x | TB 0 | TB1IE 0 | TB1F 0 | 0 | x | 0 |
| 0C | **LTICR** Reset Value | ICR7 0 | ICR6 0 | ICR5 0 | ICR4 0 | ICR3 0 | ICR2 0 | ICR1 0 | ICR0 0 |

**SERIAL PERIPHERAL INTERFACE** (cont'd)

### 11.4.3.1 Functional Description

A basic example of interconnections between a single master and a single slave is illustrated in Figure 49.

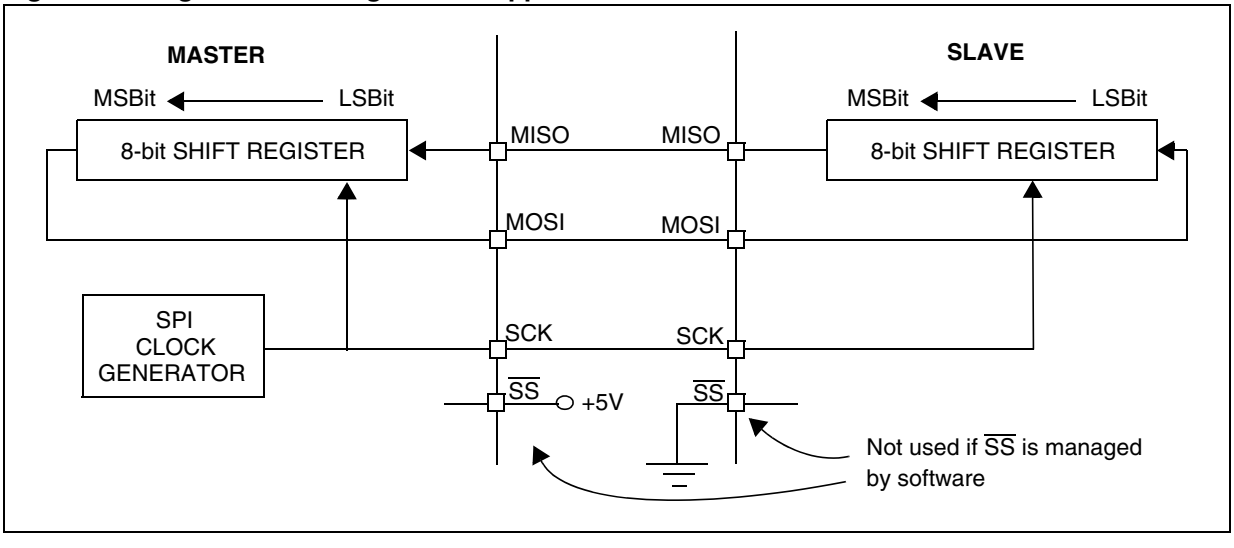
The MOSI pins are connected together and the MISO pins are connected together. In this way data is transferred serially between master and slave (most significant bit first).

The communication is always initiated by the master. When the master device transmits data to a slave device via MOSI pin, the slave device responds by sending data to the master device via the MISO pin. This implies full duplex communication with both data out and data in synchronized with the same clock signal (which is provided by the master device via the SCK pin).

To use a single data line, the MISO and MOSI pins must be connected at each node (in this case only simplex communication is possible).

Four possible data/clock timing relationships may be chosen (see Figure 52 on page 83) but master and slave must be programmed with the same timing mode.

**Figure 49. Single Master/ Single Slave Application**



**LINSCI™ SERIAL COMMUNICATION INTERFACE (SCI Mode)** (cont'd)

#### 11.5.5.3 Receiver

The SCI can receive data words of either 8 or 9 bits. When the M bit is set, word length is 9 bits and the MSB is stored in the R8 bit in the SCICR1 register.

**Character reception**

During a SCI reception, data shifts in least significant bit first through the RDI pin. In this mode, the SCIDR register consists or a buffer (RDR) between the internal bus and the received shift register (see Figure 55).

**Procedure**

– Select the M bit to define the word length.

– Select the desired baud rate using the SCIBRR and the SCIERPR registers.

– Set the RE bit, this enables the receiver which begins searching for a start bit.

When a character is received:

– The RDRF bit is set. It indicates that the content of the shift register is transferred to the RDR.

– An interrupt is generated if the RIE bit is set and the I[1:0] bits are cleared in the CCR register.

– The error flags can be set if a frame error, noise or an overrun error has been detected during reception.

Clearing the RDRF bit is performed by the following software sequence done by:

1. An access to the SCISR register

2. A read to the SCIDR register.

The RDRF bit must be cleared before the end of the reception of the next character to avoid an overrun error.

**Idle Line**

When an idle line is detected, there is the same procedure as a data received character plus an interrupt if the ILIE bit is set and the I[1:0] bits are cleared in the CCR register.

**Overrun Error**

An overrun error occurs when a character is received when RDRF has not been reset. Data can not be transferred from the shift register to the TDR register as long as the RDRF bit is not cleared.

When an overrun error occurs:

– The OR bit is set.

– The RDR content will not be lost.

– The shift register will be overwritten.

– An interrupt is generated if the RIE bit is set and the I[1:0] bits are cleared in the CCR register.

The OR bit is reset by an access to the SCISR register followed by a SCIDR register read operation.

**Noise Error**

Oversampling techniques are used for data recovery by discriminating between valid incoming data and noise.

When noise is detected in a character:

– The NF bit is set at the rising edge of the RDRF bit.

– Data is transferred from the Shift register to the SCIDR register.

– No interrupt is generated. However this bit rises at the same time as the RDRF bit which itself generates an interrupt.

The NF bit is reset by a SCISR register read operation followed by a SCIDR register read operation.

**Framing Error**

A framing error is detected when:

– The stop bit is not recognized on reception at the expected time, following either a desynchronization or excessive noise.

– A break is received.

When the framing error is detected:

– the FE bit is set by hardware

– Data is transferred from the Shift register to the SCIDR register.

– No interrupt is generated. However this bit rises at the same time as the RDRF bit which itself generates an interrupt.

The FE bit is reset by a SCISR register read operation followed by a SCIDR register read operation.

**Break Character**

– When a break character is received, the SCI handles it as a framing error. To differentiate a break character from a framing error, it is necessary to read the SCIDR. If the received value is 00h, it is a break character. Otherwise it is a framing error.

## LINSCI™ SERIAL COMMUNICATION INTERFACE (SCI Mode) (cont'd)

### 11.5.6 Low Power Modes

| Mode | Description |
|---|---|
| WAIT | No effect on SCI.<br>SCI interrupts cause the device to exit from Wait mode. |
| HALT | SCI registers are frozen.<br>In Halt mode, the SCI stops transmitting/receiving until Halt mode is exited. |

### 11.5.7 Interrupts

| Interrupt Event | Event Flag | Enable Control Bit | Exit from Wait | Exit from Halt |
|---|---|---|---|---|
| Transmit Data Register Empty | TDRE | TIE | Yes | No |
| Transmission Complete | TC | TCIE | | |
| Received Data Ready to be Read | RDRF | RIE | | |
| Overrun Error or LIN Synch Error Detected | OR/ LHE | | | |
| Idle Line Detected | IDLE | ILIE | | |
| Parity Error | PE | PIE | | |
| LIN Header Detection | LHDF | LHIE | | |

The SCI interrupt events are connected to the same interrupt vector (see Interrupts chapter).

These events generate an interrupt if the corresponding Enable Control Bit is set and the interrupt mask in the CC register is reset (RIM instruction).

**LINSCI™ SERIAL COMMUNICATION INTERFACE (LIN Mode)** (cont'd)

### 11.5.9.4 LIN Error Detection

#### LIN Header Error Flag

The LIN Header Error Flag indicates that an invalid LIN Header has been detected.

When a LIN Header Error occurs:

– The LHE flag is set

– An interrupt is generated if the RIE bit is set and the I[1:0] bits are cleared in the CCR register.

If autosynchronization is enabled (LASE bit = 1), this can mean that the LIN Synch Field is corrupted, and that the SCI is in a blocked state (LSF bit is set). The only way to recover is to reset the LSF bit and then to clear the LHE bit.

– The LHE bit is reset by an access to the SCISR register followed by a read of the SCIDR register.

#### LHE/OVR Error Conditions

When Auto Resynchronization is disabled (LASE bit = 0), the LHE flag detects:

– That the received LIN Synch Field is not equal to 55h.

– That an overrun occurred (as in standard SCI mode)

– Furthermore, if LHDM is set it also detects that a LIN Header Reception Timeout occurred (only if LHDM is set).

When the LIN auto-resynchronization is enabled (LASE bit = 1), the LHE flag detects:

– That the deviation error on the Synch Field is outside the LIN specification which allows up to +/-15.5% of period deviation between the slave and master oscillators.

– A LIN Header Reception Timeout occurred. If $T_{HEADER} > T_{HEADER\_MAX}$ then the LHE flag is set. Refer to Figure 60. (only if LHDM is set to 1)

– An overflow during the Synch Field Measurement, which leads to an overflow of the divider registers. If LHE is set due to this error then the SCI goes into a blocked state (LSF bit is set).

– That an overrun occurred on Fields other than the Synch Field (as in standard SCI mode)

#### Deviation Error on the Synch Field

The deviation error is checking by comparing the current baud rate (relative to the slave oscillator) with the received LIN Synch Field (relative to the master oscillator). Two checks are performed in parallel:

– The first check is based on a measurement between the first falling edge and the last falling edge of the Synch Field. Let us refer to this period deviation as D:

If the LHE flag is set, it means that:

D > 15.625%

If LHE flag is not set, it means that:

D < 16.40625%

If 15.625% ≤ D < 16.40625%, then the flag can be either set or reset depending on the dephasing between the signal on the RDI line and the CPU clock.

– The second check is based on the measurement of each bit time between both edges of the Synch Field: this checks that each of these bit times is large enough compared to the bit time of the current baud rate.

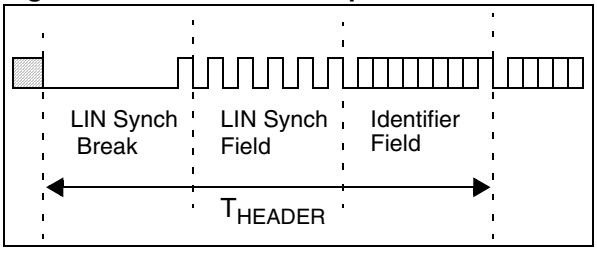
When LHE is set due to this error then the SCI goes into a blocked state (LSF bit is set).

#### LIN Header Time-out Error

When the LIN Identifier Field Detection Method is used (by configuring LHDM to 1) or when LIN auto-resynchronization is enabled (LASE bit = 1), the LINSCI automatically monitors the $T_{HEADER\_MAX}$ condition given by the LIN protocol.

If the entire Header (up to and including the STOP bit of the LIN Identifier Field) is not received within the maximum time limit of 57 bit times then a LIN Header Error is signalled and the LHE bit is set in the SCISR register.

**Figure 60. LIN Header Reception Timeout**




The time-out counter is enabled at each break detection. It is stopped in the following conditions:
- A LIN Identifier Field has been received
- An LHE error occurred (other than a timeout error).
- A software reset of LSF bit (transition from high to low) occurred during the analysis of the LIN Synch Field or

If LHE bit is set due to this error during the LIN Synchr Field (if LASE bit = 1) then the SCI goes into a blocked state (LSF bit is set).

**OPERATING CONDITIONS** (Cont'd)

**Figure 70. Typical accuracy with RCCR=RCCR0 vs $V_{DD}$= 4.5 to 5.5V and Temperature**

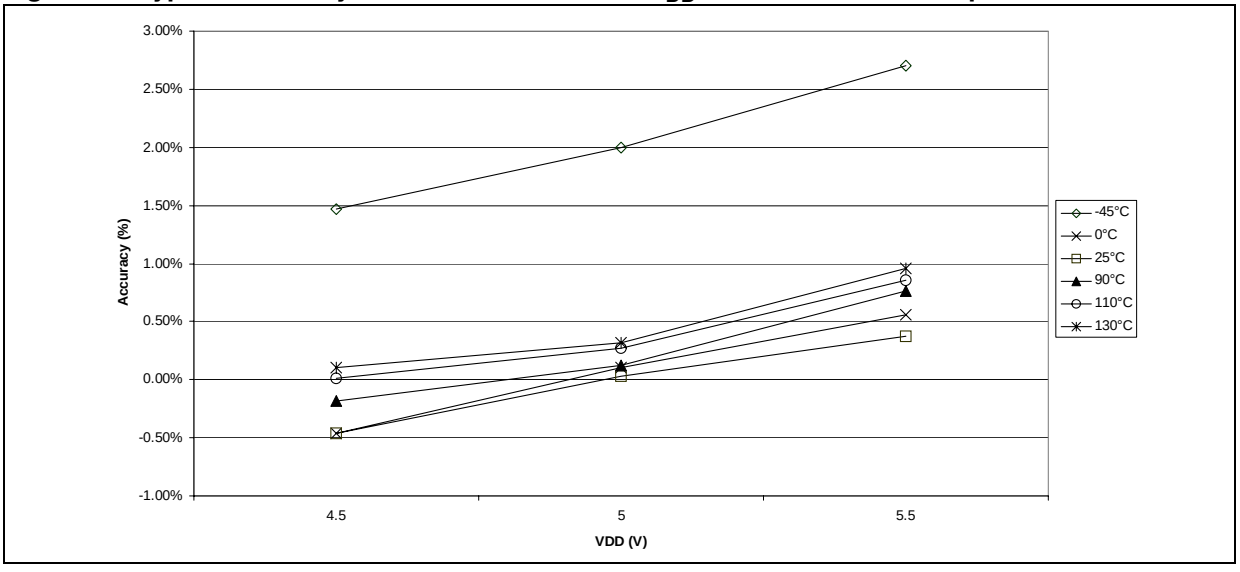
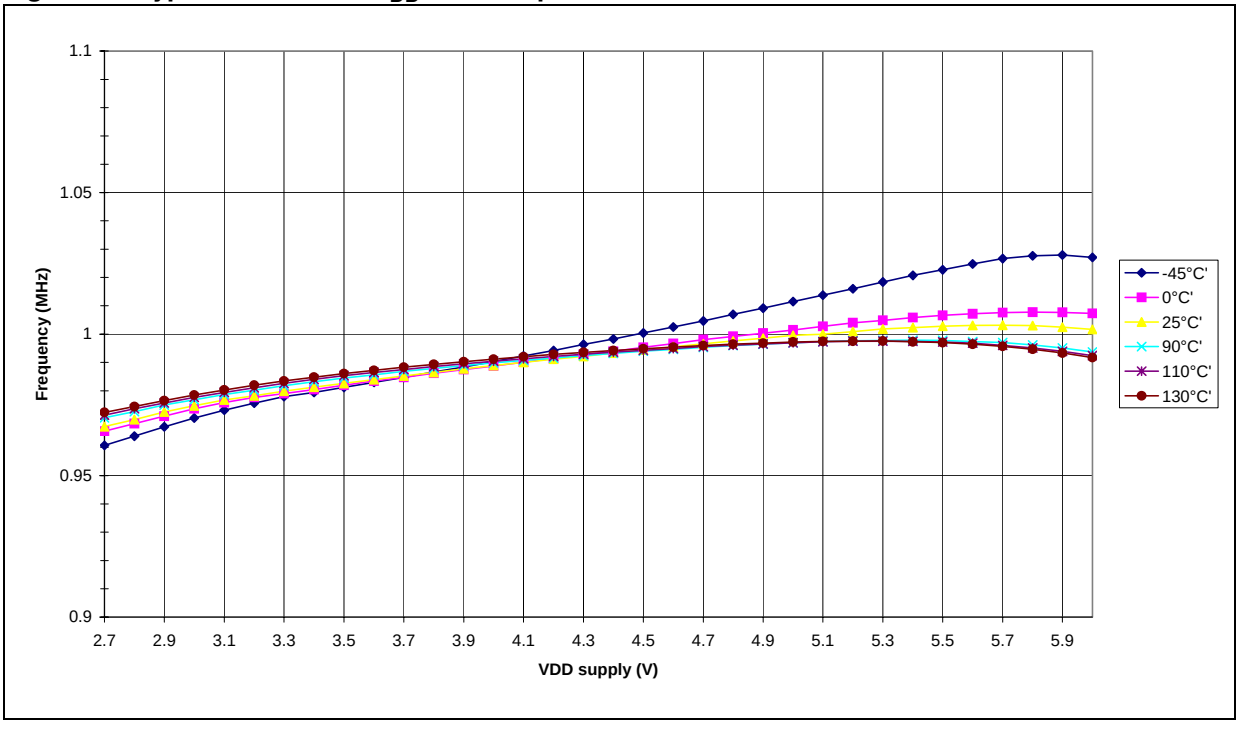



**Figure 71. Typical RCCR0 vs $V_{DD}$ and Temperature**



**OPERATING CONDITIONS** (Cont'd)

**Figure 74. PLL $\Delta f_{CPU}/f_{CPU}$ versus time**

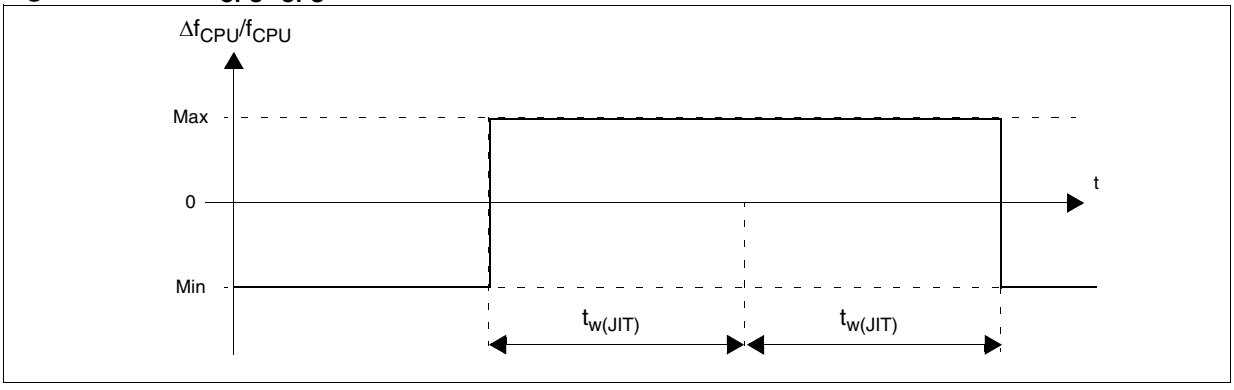
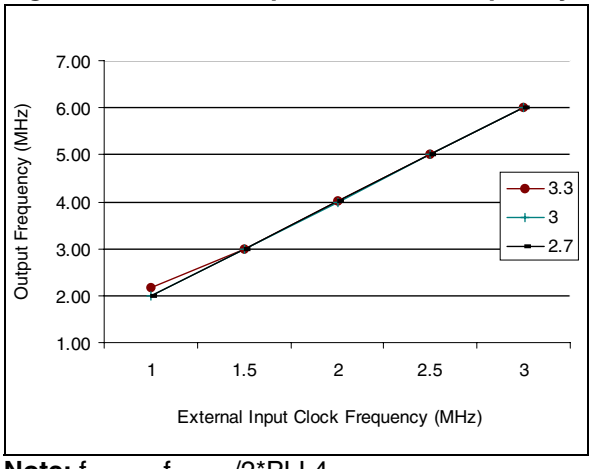
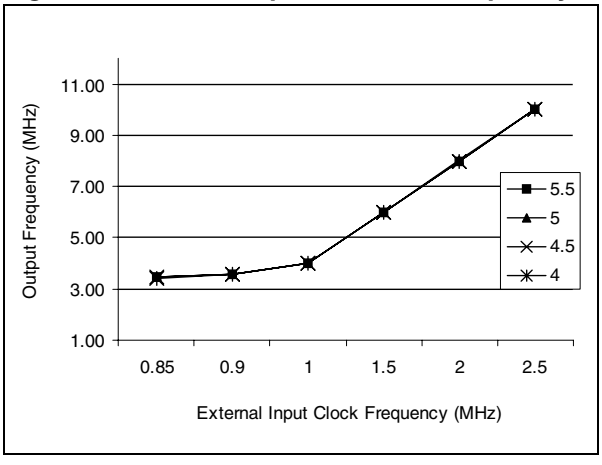



**Figure 75. PLLx4 Output vs CLKIN frequency**




**Note:** $f_{OSC} = f_{CLKIN}/2*PLL4$

**Figure 76. PLLx8 Output vs CLKIN frequency**




**Note:** $f_{OSC} = f_{CLKIN}/2*PLL8$

## 13.4 SUPPLY CURRENT CHARACTERISTICS

The following current consumption specified for the ST7 functional operating modes over temperature range does not take into account the clock source current consumption. To get the total device consumption, the two current values must be added (except for HALT mode for which the clock is stopped).

### 13.4.1 Supply Current

$T_A$ = -40 to +125°C unless otherwise specified

| Symbol | Parameter | Conditions | | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in RUN mode | $V_{DD}$=5.5V | $f_{CPU}$=8MHz [1], -40°C≤$T_A$≤+85°C | 6 | 9 | mA |
| | | | $f_{CPU}$=8MHz [1], -40°C≤$T_A$≤+125°C | | 10 | |
| | | | $f_{CPU}$=4MHz , -40°C≤$T_A$≤+85°C | 2.6 | 5.6 | |
| | | | $f_{CPU}$=4MHz , -40°C≤$T_A$≤+125°C | | | |
| | | | $f_{CPU}$=1MHz , -40°C≤$T_A$≤+85°C | 0.8 | 2.5 | |
| | | | $f_{CPU}$=1MHz , -40°C≤$T_A$≤+125°C | | | |
| | Supply current in WAIT mode | | $f_{CPU}$=8MHz [2] , -40°C≤$T_A$≤+85°C | 2.4 | 4 | |
| | | | $f_{CPU}$=8MHz [2] , -40°C≤$T_A$≤+125°C | | 4.5 | |
| | Supply current in SLOW mode | | $f_{CPU}$=250kHz [3] , -40°C≤$T_A$≤+85°C | 0.7 | 1.1 | |
| | | | $f_{CPU}$=250kHz [3] , -40°C≤$T_A$≤+125°C | | 1.5 | |
| | Supply current in SLOW WAIT mode | | $f_{CPU}$=250kHz [4], -40°C≤$T_A$≤+85°C | 0.6 | 1 | |
| | | | $f_{CPU}$=250kHz [4], -40°C≤$T_A$≤+125°C | | 1.4 | |
| | Supply current in HALT mode[5] | | -40°C≤$T_A$≤+85°C | 0.5 | 10 | µA |
| | | | -40°C≤$T_A$≤+125°C | | 20 | |
| | Supply current in AWUFH mode [6][7] | | -40°C≤$T_A$≤+85°C | 20 | 50 | |
| | | | -40°C≤$T_A$≤+125°C | | 300 | |
| | Supply current in ACTIVE HALT mode | | -40°C≤$T_A$≤+85°C | 0.7 | 1 | mA |
| | | | -40°C≤$T_A$≤+125°C | | | |
| | Supply current in RUN mode | $V_{DD}$=3.3V | $f_{CPU}$=8MHz [1], -40°C≤$T_A$≤+85°C | 4.0 | 7 | mA |
| | | | $f_{CPU}$=8MHz [1], -40°C≤$T_A$≤+125°C | 4.0 | 11 | |
| | | | $f_{CPU}$=4MHz | 1.7 | 4.7 | |
| | | | $f_{CPU}$=1MHz | 0.5 | 2.2 | |
| | Supply current in WAIT mode | | $f_{CPU}$=8MHz [2], -40°C≤$T_A$≤+85°C | 1.5 | 3.1 | |
| | | | $f_{CPU}$=8MHz [2], -40°C≤$T_A$≤+125°C | 1.5 | 4.5 | |
| | Supply current in SLOW mode | | $f_{CPU}$=250kHz [3], -40°C≤$T_A$≤+85°C | 0.2 | 0.6 | |
| | | | $f_{CPU}$=250kHz [3], -40°C≤$T_A$≤+125°C | 0.2 | 1.5 | |
| | Supply current in SLOW WAIT mode | | $f_{CPU}$=250kHz [4], -40°C≤$T_A$≤+85°C | 0.1 | 0.5 | |
| | | | $f_{CPU}$=250kHz [4], -40°C≤$T_A$≤+125°C | 0.1 | 1.4 | |
| | Supply current in HALT mode[5] | | -40°C≤$T_A$≤+85°C | 0.1 | 1 | µA |
| | | | -40°C≤$T_A$≤+125°C | 0.1 | 10 | |
| | Supply current in AWUFH mode [6][7] | | -40°C≤$T_A$≤+85°C | 9.6 | 11 | |
| | | | -40°C≤$T_A$≤+125°C | 9.6 | 300 | |
| | Supply current in ACTIVE HALT mode | | -40°C≤$T_A$≤+85°C | 0.5 | 50 | mA |
| | | | -40°C≤$T_A$≤+125°C | 0.5 | 100 | |

**Notes:**

**1.** CPU running with memory access, all I/O pins in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load), all peripherals in reset state; clock input (CLKIN) driven by external square wave, LVD disabled.

**2.** All I/O pins in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load), all peripherals in reset state; clock input (CLKIN)

**EMC CHARACTERISTICS** (Cont'd)

### 13.7.2 EMI (Electromagnetic Interference)

Based on a simple application running on the product (toggling two LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

| Symbol | Parameter | Conditions | Monitored Frequency Band | Max vs. [$f_{OSC}/f_{CPU}$] | | Unit |
|---|---|---|---|---|---|---|
| | | | | 8/4MHz | 16/8MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$=5V, $T_A$=+25°C, SO20 package, conforming to SAE J 1752/3 | 0.1MHz to 30MHz | 16 | 17 | dBµV |
| | | | 30MHz to 130MHz | 20 | 25 | |
| | | | 130MHz to 1GHz | 15 | 16 | |
| | | | SAE EMI Level | 3 | 3.5 | - |

**Note:**

**1.** Data based on characterization results, not tested in production.

### 13.7.3 Absolute Maximum Ratings (Electrical Sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

#### 13.7.3.1 Electrostatic Discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

**ESD Absolute Maximum Ratings**

| Symbol | Ratings | Conditions | Maximum value [1] | Unit |
|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electro-static discharge voltage (Human Body Model) | $T_A$=+25°C | 6000 | V |

**Notes:**

1. Data based on characterization results, not tested in production.

#### 13.7.3.2 Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. These tests are compliant with the EIA/JESD 78 IC latch-up standard.

**Electrical Sensitivities**

| Symbol | Parameter | Conditions | Class [1] |
|---|---|---|---|
| LU | Static latch-up class | $T_A$=+25°C | A |

**Note:**

**1.** Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

## I/O PORT PIN CHARACTERISTICS (Cont'd)

### 13.8.2 Output Driving Current

Subject to general operating conditions for $V_{DD}$, $f_{CPU}$, and $T_A$ unless otherwise specified.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ 1) | Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see Figure 88) | $V_{DD}$=5V | $I_{IO}$=+5mA $T_A \le 125°C$ | | 0.65 | 1.0 | V |
| | | | $I_{IO}$=+2mA $T_A \le 125°C$ | | 0.25 | 0.4 | |
| | Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time (see Figure 91) | | $I_{IO}$=+20mA, $T_A \le 125°C$ | | 1.05 | 1.3 | |
| | | | $I_{IO}$=+8mA $T_A \le 125°C$ | | 0.4 | 0.75 | |
| $V_{OH}$ 2) | Output high level voltage for an I/O pin when 4 pins are sourced at same time (see Figure 94) | | $I_{IO}$= -5mA, $T_A \le 125°C$ | $V_{DD}$-1.5 | 4.30 | | |
| | | | $I_{IO}$= -2mA $T_A \le 125°C$ | $V_{DD}$-0.8 | 4.70 | | |
| $V_{OL}$ 1)3) | Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see Figure 87) | $V_{DD}$=4V | $I_{IO}$=+2mA $T_A \le 125°C$ | | 0.25 | | |
| | Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time (see Figure 90) | | $I_{IO}$=+8mA $T_A \le 125°C$ | | 0.35 | | |
| $V_{OH}$ 2)3) | Output high level voltage for an I/O pin when 4 pins are sourced at same time (see Figure 93) | | $I_{IO}$= -2mA $T_A \le 125°C$ | | 3.70 | | |
| $V_{OL}$ 1)3) | Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see Figure 86) | $V_{DD}$=3V | $I_{IO}$=+2mA $T_A \le 125°C$ | | 0.30 | | |
| | Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time (see Figure 89) | | $I_{IO}$=+8mA $T_A \le 125°C$ | | 0.40 | | |
| $V_{OH}$ 2)3) | Output high level voltage for an I/O pin when 4 pins are sourced at same time (see Figure 92) | | $I_{IO}$= -2mA $T_A \le 125°C$ | | 2.60 | | |

**Notes:**

**1.** The $I_{IO}$ current sunk must always respect the absolute maximum rating specified in Section 13.2.2 and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.

**2.** The $I_{IO}$ current sourced must always respect the absolute maximum rating specified in Section 13.2.2 and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.

**3.** Not tested in production, based on characterization results.

**OPTION BYTES** (Cont'd)

| | OPTION BYTE 0 | | | | | | | | OPTION BYTE 1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 7 | | | | | | | 0 | 7 | | | | | | | 0 |
| | AWU CK | OSCRANGE 2:0 | | | SEC1 | SEC0 | FMPR | FMPW | PLL x4x8 | PLL OFF | Res. | OSC | LVD 1:0 | | WDG SW | WDG HALT |
| Default Value | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

**OPTION BYTE 1**

OPT 7 = **PLLx4x8** *PLL Factor Selection*.
0: PLLx4
1: PLLx8

OPT 6 = **PLLOFF** *PLL Disable*
This option bit enables or disables the PLL.
0: PLL enabled
1: PLL disabled (bypassed)

OPT 5 = Reserved. Must always be set to 1.

OPT 4 = **OSC** *RC Oscillator Selection*
This option bit enables to select the internal RC Oscillator.
0: RC Oscillator on
1: RC Oscillator off

**Notes:**

– RC oscillator available on ST7LITE35 and ST7LITE39 devices only

– If the RC oscillator is selected, then to improve clock stability and frequency accuracy, it is recommended to place a decoupling capacitor, typically 100nF, between the $V_{DD}$ and $V_{SS}$ pins as close as possible to the ST7 device.

OPT 3:2 = **LVD[1:0]** *Low Voltage Selection*
These option bits enable the voltage detection block (LVD and AVD) with a selected threshold to the LVD and AVD.

| Configuration | VD1 | VD0 |
|---|---|---|
| LVD Off | 1 | 1 |
| Highest Voltage Threshold | 1 | 0 |
| Medium Voltage Threshold | 0 | 1 |
| Lowest Voltage Threshold | 0 | 0 |

OPT 1 = **WDGSW** *Hardware or Software Watchdog*
0: Hardware (watchdog always enabled)
1: Software (watchdog to be enabled by software)

OPT 0 = **WDG HALT** *Watchdog Reset on Halt*
0: No reset generation when entering HALT mode
1: Reset generation when entering HALT mode

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