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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	32-Bit Single-Core
Speed	76.2MHz
Connectivity	EBI/EMI, Ethernet, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lh79525n0q100a1-55

SIGNAL DESCRIPTIONS

Table 2. LH79524 Pin Descriptions

LFBGA PIN	SIGNAL NAME	TYPE	DESCRIPTION
T12	A0	O	External Address Bus
R11	A1		
T11	A2		
P10	A3		
R10	A4		
T10	A5		
P9	A6		
R9	A7		
T9	A8		
T8	A9		
R8	A10		
P8	A11		
T7	A12		
R7	A13		
P7	A14		
T6	A15		
M15	D0	I/O	External Data Bus
N16	D1		
L13	D2		
M14	D3		
N15	D4		
P16	D5		
M13	D6		
N14	D7		
F14	SDCLK	O	SDRAM Clock
G15	SDCKE	O	SDRAM Clock Enable
D13	DQM0	O	Data Mask Output to SDRAMs
E13	DQM1		
E14	DQM2		
G14	DQM3		
G16	nDCS0	O	SDRAM Chip Select
H14	nDCS1	O	SDRAM Chip Select
H15	nRAS	O	Row Address Strobe
H16	nCAS	O	Column Address Strobe
L16	nCS0/PM0	O	Static Memory Chip Select; multiplexed with GPIO Port M[3:0] (output only)
L15	nCS1/PM1		
M16	nCS2/PM2		
L14	nCS3/PM3		
J15	nBLE0/PM4	O	Static Memory Byte Lane Enable / Byte Write Enable; multiplexed with GPIO Port M[7:4] (output only)
J14	nBLE1/PM5		
K16	nBLE2/PM6		
K15	nBLE3/PM7		

Table 2. LH79524 Pin Descriptions (Cont'd)

LFBGA PIN	SIGNAL NAME	TYPE	DESCRIPTION
K14	nOE	O	Static Memory Output Enable
J16	nWE	O	Static Memory Write Enable
A16	USBDN	I/O	USB Data Negative (Differential Pair output, single ended and Differential pair input)
A15	USBDP	I/O	USB Data Positive (Differential Pair output, single ended and Differential pair input)
E2	AN0/UL/X+	I	ADC Input 0, 4-wire touch screen Upper Left, 5-wire touch screen X+
F2	AN1/UR/X–	I	ADC Input 1, 4-wire touch screen Upper Right, 5-wire touch screen X–
G2	AN2/LL/Y+/PJ3	I	ADC Input 2, 4-wire touch screen Lower Left, 5-wire touch screen Y+; multiplexed with GPIO Port J3 (input only)
H2	AN3/LR/Y–/PJ0	I	ADC Input 3, 4-wire touch screen Upper Right, 5-wire touch screen Y–; multiplexed with GPIO Port J0 (input only)
H3	AN4/WIPER/PJ1	I	ADC Input 4, 5-wire touch screen Wiper input; multiplexed with GPIO Port J1 (input only)
F1	AN5/PJ5/INT5	I	ADC Input 5; multiplexed with GPIO Port J5 (input only) and External Interrupt 5
F3	AN6/PJ7/INT7	I	ADC Input 6; multiplexed with GPIO Port J7 (input only) and External Interrupt 7
E1	AN7/PJ6/INT6	I	ADC Input 7; multiplexed with GPIO Port J6 (input only) and External Interrupt 6
G3	AN8/PJ4	I	ADC Input 8; multiplexed with GPIO Port J4 (input only)
G1	AN9/PJ2	I	ADC Input 9; multiplexed with GPIO Port J2 (input only)
J3	CTCLK/INT4/BATCNTL	I/O	Timer[2:0] External Clock input; muxed with External Int 4 and Battery Control
N1	PA0/INT2/UARTRX2/ UARTIRRX2	I/O	General Purpose I/O Signal — Port A0; multiplexed with UART2 Received Serial Data Input, UART2 Infrared Received Serial Data In, and External Interrupt 2
M2	PA1/INT3/UARTTX2/ UARTIRTX2	I/O	General Purpose I/O Signal — Port A1; multiplexed with UART2 Transmitted Serial Data Output, UART2 Serial Transmit Data Out, and External Interrupt 3
L3	PA2/CTCAP0A/ CTCMP0A	I/O	General Purpose I/O Signal — Port A2; multiplexed with Counter/Timer 0 Capture A input and Counter/Timer 0 Compare A output
M1	PA3/CTCAP0B/ CTCMP0B	I/O	General Purpose I/O Signal — Port A3; multiplexed with Counter/Timer 0 Capture B input and Counter/Timer 0 Compare B output
L2	PA4/CTCAP1A/ CTCMP1A	I/O	General Purpose I/O Signal — Port A4; multiplexed with Counter/Timer 1 Capture A input and Counter/Timer 1 Compare A output
L1	PA5/CTCAP1B/ CTCMP1B	I/O	General Purpose I/O Signal — Port A5; multiplexed with Counter/Timer 1 Capture B input and Counter/Timer 1 Compare B output
K3	PA6/CTCAP2A/ CTCMP2A/SDA	I/O	General Purpose I/O Signal — Port A6; multiplexed with Counter/Timer 2 Capture A input, Counter/Timer 2 Compare A output, I^2C Bus Data (open drain)
K2	PA7/CTCAP2B/ CTCMP2B/SCL	I/O	General Purpose I/O Signal — Port A7; multiplexed with Counter/Timer 2 Capture B input, Counter/Timer 2 Compare B output, I^2C Bus Clock (open drain)
R2	PB0/nDACK/ nUARTCTS0	I/O	General Purpose I/O Signal — Port B0; multiplexed with DMA Acknowledge and UART0 CTS
R1	PB1/DREQ/ nUARTRTS0	I/O	General Purpose I/O Signal — Port B1; multiplexed with DMA Request and UART0 RTS
P2	PB2/SSPFRM/I2SWS	I/O	General Purpose I/O Signal — Port B2; multiplexed with SSP Serial Frame Output and I^2S Frame Output
N3	PB3/SSPCLK/I2SCLK	I/O	General Purpose I/O Signal — Port B3; multiplexed with SSP Clock and I^2S Clock
M4	PB4/SSPRX/I2SRXD/ UARTRX1/ UARTIRRX1	I/O	General Purpose I/O Signal — Port B4; multiplexed with SSP Data In, I^2S Data In, UART1 Serial Data In, and UART1 Infrared Data In
P1	PB5/SSPTX/I2STXD/ UARTTX1/UARTIRTX1	I/O	General Purpose I/O Signal — Port B5; multiplexed with SSP Data Out, I^2S Data Out, UART1 Data Out, and UART1 IR Data Out
N2	PB6/INT0/UARTRX0/ UARTIRRX0	I/O	General Purpose I/O Signal — Port B6; multiplexed with UART0 Infrared Received Serial Data Input, UART0 Received Serial Data In, and External Interrupt 0

Table 3. LH79524 Numerical Pin List (Cont'd)

LFBGA NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
P8	A11		8 mA	
P9	A6		8 mA	
P10	A3		8 mA	
P11	PN3	D25	8 mA	1
P12	PD6	D14	8 mA	1
P13	PK4	D20	8 mA	1
P14	PD1	D9	8 mA	1
P15	PD0	D8	8 mA	1
P16	D5		8 mA	1
R1	PB1	DREQ/ nUARTRTS0	8 mA	2
R2	PB0	nDACK/ nUARTCTS0	8 mA	2
R3	TEST2			2, 6
R4	PC7	A23/nFRE	8 mA	1
R5	PC4	A20	8 mA	1
R6	PC1	A17	8 mA	1
R7	A13		8 mA	
R8	A10		8 mA	
R9	A7		8 mA	
R10	A4		8 mA	
R11	A1		8 mA	
R12	PN2	D24	8 mA	1
R13	PK6	D22	8 mA	1
R14	PK5	D21	8 mA	1
R15	PK3	D19	8 mA	1
R16	PK0	D16	8 mA	1
T1	TDI			2, 6
T2	TEST1			2, 6
T3	TCK			2, 6

Table 3. LH79524 Numerical Pin List (Cont'd)

LFBGA NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
T4	PC5	A21	8 mA	1
T5	PC2	A18	8 mA	1
T6	A15		8 mA	
T7	A12		8 mA	
T8	A9		8 mA	
T9	A8		8 mA	
T10	A5		8 mA	
T11	A2		8 mA	
T12	A0		8 mA	
T13	PD7	D15	8 mA	1
T14	PD5	D13	8 mA	1
T15	PD3	D11	8 mA	1
T16	PK2	D18	8 mA	1

NOTES:
1. Internal pull-down. The internal pullup and pulldown resistance on all digital I/O pins is 50KΩ.
2. Internal pull-up. The internal pullup and pulldown resistance on all digital I/O pins is 50KΩ.
3. USB Inputs/outputs are tristated.
4. Output is for crystal oscillator only, no drive capability.
5. Crystal Oscillator Inputs should be driven to a maximum of 1.8 V ± 10%.
6. Input with Schmitt Trigger.
7. Output Drive Values are MAX. See 'DC Specifications'.
8. All unused analog pins, and XTAL32IN (if unused) should be tied to ground through a 33KΩ resistor.

Table 4. TESTx PIN FUNCTION

MODE	TEST1	TEST2	nBLE0
Embedded ICE	0	1	1
Normal	1	1	x

Table 5. LH79525 Pin Descriptions (Cont'd)

PIN NO.	SIGNAL NAME	TYPE	DESCRIPTION
163	PH7/ETHERTX3	I/O	General Purpose I/O Signals — Port H7; multiplexed with Ethernet Transmit Channel 3
4	PI0/ETHERMDC	I/O	General Purpose I/O Signals — Port I0; multiplexed with Ethernet Management Data Clock
2	PI1/ETHERMDIO	I/O	General Purpose I/O Signals — Port I1; multiplexed with Ethernet Management Data I/O
1	PI2/ETHERCOL	I/O	General Purpose I/O Signals — Port I2; multiplexed with Ethernet Collision Detect
176	PI3/ETHERCRS	I/O	General Purpose I/O Signals — Port I3; multiplexed with Ethernet Carrier Sense
175	PI4/ETHERRXER	I/O	General Purpose I/O Signals — Port I4; multiplexed with Ethernet Receive Error
174	PI5/ETHERRX0	I/O	General Purpose I/O Signals — Port I5; multiplexed with Ethernet Receive Channel 0
173	PI6/ETHERRX1	I/O	General Purpose I/O Signals — Port I6; multiplexed with Ethernet Receive Channel 1
172	PI7/ETHERRX2	I/O	General Purpose I/O Signals — Port I7; multiplexed with Ethernet Receive Channel 2
24	nRESETIN	I	Reset Input
22	nRESETOUT	O	Reset Output
127	XTALIN	I	Crystal Input, or external clock input
128	XTALOUT	O	Crystal Output
125	XTAL32IN	I	32.768 kHz Crystal Oscillator Input, or external clock input,
126	XTAL32OUT	O	32.768 kHz Crystal Oscillator Output
23	CLKOUT	O	Clock Out (selectable from the internal bus clock or 32.768 MHz)
8	nTRST	I	JTAG Test Reset Input
50	TMS	I	JTAG Test Mode Select Input
51	TCK	I	JTAG Test Clock Input
46	TDI	I	JTAG Test Serial Data Input
45	TDO	O	JTAG Test Data Serial Output
47	TEST1	I	Tie HIGH for Normal Operation; pull LOW to enable embedded ICE Debugging
48	TEST2	I	Tie HIGH for Normal Operation; pull HIGH to enable embedded ICE Debugging
9	LINREGEN	I	Linear Regulator Enable (Requires pull-up. See User's Guide)
6, 66, 107, 150	VDDC	Power	Core Power Supply
7, 64, 105,148	VSSC	Ground	Core GND
3, 26, 33, 57, 75, 86, 101, 129, 135, 144, 160	VDD	Power	Input/Output Power Supply
5, 27, 49, 68, 81, 92, 108, 132, 140, 152, 168	VSS	Ground	Input/Output GND
10	VDDA0	Power	Analog Power Supply for Analog-to-Digital Converter
122	VDDA1	Power	Analog Power Supply for the USB PLL
123	VDDA2	Power	Analog Power Supply for System PLL
21	VSSA0	Ground	Analog GND for Analog-to-Digital Converter
121	VSSA1	Ground	Analog GND for the USB PLL
124	VSSA2	Ground	Analog GND for System PLL

Table 6. LH79525 Numerical Pin List

PIN NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
1	PI2	ETHERCOL	8 mA	1

Table 6. LH79525 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
2	PI1	ETHERMDIO	8 mA	2

Table 6. LH79525 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
97	D2		8 mA	1
98	D1		8 mA	1
99	D0		8 mA	1
100	nCS3	PM3	8 mA	
101	VDD			
102	nCS2	PM2	8 mA	
103	nCS1	PM1	8 mA	
104	nCS0	PM0	8 mA	
105	VSSC			
106	nOE		8 mA	
107	VDDC			
108	VSS			
109	nBLE1	PM5	8 mA	
110	nBLE0	PM4	8 mA	
111	nWE		8 mA	
112	nCAS		8 mA	
113	nRAS		8 mA	
114	nDCS1		8 mA	
115	nDCS0		8 mA	
116	SDCKE		8 mA	
117	SDCLK		12 mA	
118	DQM1		8 mA	
119	DQM0		8 mA	
120	PE7	nWAIT/nDEOT	8 mA	2, 3
121	VSSA1			
122	VDDA1			
123	VDDA2			
124	VSSA2			
125	XTAL32IN			5
126	XTAL32OUT			6
127	XTALIN			5
128	XTALOUT			6
129	VDD			
130	USBDN			4
131	USBDP			4
132	VSS			
133	PE6	LCDVEEN/ LCDMOD	8 mA	1
134	PE5	LCDVDDEN	8 mA	1
135	VDD			
136	PE4	LCDDSPLEN/LCDREV	8 mA	1
137	PE3	LCDCLS	8 mA	1
138	PE2	LCDPS	8 mA	1
139	PE1	LCDDCLK	8 mA	1
140	VSS			
141	PE0	LCDLP/LCDHRLP	8 mA	1
142	PF7	LCDFP/LCDSPS	8 mA	1
143	PF6	LCDEN/LCDSPL	8 mA	1
144	VDD			
145	PF5	LCDVD11	8 mA	2

Table 6. LH79525 Numerical Pin List (Cont'd)

PIN NO.	FUNCTION AT RESET	MULTIPLEXED FUNCTION(S)	OUTPUT DRIVE	NOTES
146	PF4	LCDVD10	8 mA	2
147	PF3	LCDVD9	8 mA	2
148	VSSC			
149	PF2	LCDVD8	8 mA	2
150	VDDC			
151	PF1	LCDVD7	8 mA	1
152	VSS			
153	PF0	LCDVD6	8 mA	1
154	PG7	LCDVD5	8 mA	1
155	PG6	LCDVD4	8 mA	1
156	PG5	LCDVD3	8 mA	1
157	PG4	LCDVD2	8 mA	1
158	PG3	LCDVD1	8 mA	1
159	PG2	LCDVD0	8 mA	1
160	VDD			
161	PG1	ETHERTXCLK	8 mA	1
162	PG0	ETHERTXEN	8 mA	1
163	PH7	ETHERTX3	8 mA	1
164	PH6	ETHERTX2	8 mA	1
165	PH5	ETHERTX1	8 mA	1
166	PH4	ETHERTX0	8 mA	1
167	PH3	ETHERTXER	8 mA	1
168	VSS			
169	PH2	ETHERRXCLK	8 mA	1
170	PH1	ETHERRXDV	8 mA	1
171	PH0	ETHERRX3	8 mA	1
172	PI7	ETHERRX2	8 mA	1
173	PI6	ETHERRX1	8 mA	1
174	PI5	ETHERRX0	8 mA	1
175	PI4	ETHERRXER	8 mA	1
176	PI3	ETHERCRS	8 mA	1

NOTES:

1. Internal pull-down. The internal pullup and pulldown resistance on all digital I/O pins is 50KΩ.
2. Internal pull-up. The internal pullup and pulldown resistance on all digital I/O pins is 50KΩ.
3. Input with Schmitt Trigger.
4. USB Inputs/outputs are tristated.
5. Crystal Inputs should be driven to a maximum of 1.8 V ± 10%.
6. Output is for crystal oscillator only, no drive capability.
7. Output Drive Values shown are MAX. See 'DC Specifications'.
8. All unused analog pins, and XTAL32IN (if unused) should be tied to ground through a 33KΩ resistor.

Table 7. TESTx PIN FUNCTION

MODE	TEST1	TEST2	nBLE0
Embedded ICE	0	1	1
Normal	1	1	x

Table 8. LH79524 LCD Data Multiplexing

LFBGA BALL NO.	LFBGA BALL NAME	STN						TFT
		MONO 4-BIT		MONO 8-BIT		COLOR		COLOR
		SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL	SINGLE PANEL
C2	LCDVD15	MUSTN0	MUSTN0	MUSTN0	MUSTN0	CUSTN0	CUSTN0	INTENSITY
C1	LCDVD14	X	X	X	MLSTN4	X	CLSTN4	BLUE4
C10	LCDVD13	X	X	MUSTN6	MUSTN6	CUSTN6	CUSTN6	BLUE3
A10	LCDVD12	X	X	X	MLSTN7	X	CLSTN7	BLUE2
A11	LCDVD11	X	X	X	MLSTN6	X	CLSTN6	BLUE1
B10	LCDVD10	X	X	X	MLSTN5	X	CLSTN5	BLUE0
C9	LCDVD9	X	MLSTN3	X	MLSTN3	X	CLSTN3	GREEN4
B9	LCDVD8	X	MLSTN2	X	MLSTN2	X	CLSTN2	GREEN3
A9	LCDVD7	X	MLSTN1	X	MLSTN1	X	CLSTN1	GREEN2
A8	LCDVD6	X	MLSTN0	X	MLSTN0	X	CLSTN0	GREEN1
B8	LCDVD5	X	X	MUSTN7	MUSTN7	CUSTN7	CUSTN7	GREEN0
C8	LCDVD4	X	X	MUSTN5	MUSTN5	CUSTN5	CUSTN5	RED4
A7	LCDVD3	X	X	MUSTN4	MUSTN4	CUSTN4	CUSTN4	RED3
B7	LCDVD2	MUSTN3	MUSTN3	MUSTN3	MUSTN3	CUSTN3	CUSTN3	RED2
C7	LCDVD1	MUSTN2	MUSTN2	MUSTN2	MUSTN2	CUSTN2	CUSTN2	RED1
A6	LCDVD0	MUSTN1	MUSTN1	MUSTN1	MUSTN1	CUSTN1	CUSTN1	RED0

NOTES:
1. Recommended hookups for TFT 5:5:5 + Intensity and 5:6:5 are shown.
2. The Intensity bit is identically generated for all three colors.
3. Connect to the LSB of the Red, Green, and Blue inputs of a 6:6:6 panel.
4. CLSTN = Color Lower data bit for STN panel.
5. CUSTN = Color Upper data bit for STN panel.
6. MLSTN = Monochrome Lower data bit for STN panel.
7. MUSTN = Monochrome Upper data bit for STN panel.

Table 9. LH79525 LCD Data Multiplexing

PIN NO.	PIN NAME	STN MONO 4-BIT	
		SINGLE PANEL	DUAL PANEL
145	LCDVD11	MUSTN1	MUSTN1
146	LCDVD10	MUSTN0	MUSTN0
147	LCDVD9		
149	LCDVD8		
151	LCDVD7		MLSTN3
153	LCDVD6		MLSTN2
154	LCDVD5		MLSTN1
155	LCDVD4		MLSTN0
156	LCDVD3		

Watchdog Timer

The Watchdog Timer provides hardware protection against malfunctions. It is a programmable timer to be reset by software at regular intervals. Failure to reset the timer will cause a FIQ interrupt. Failure to service the FIQ interrupt will then generate a System Reset. The features of the Watchdog Timer are:

- Driven by the bus clock
- 16 programmable time-out periods: 2^{16} through 2^{31} clock cycles
- Generates a reset or an FIQ Interrupt whenever a time-out period is reached
- Software enable, lockout, and counter-reset mechanisms add security against inadvertent writes
- Protection mechanism guards against interrupt-service failure:
  - The first WDT time-out triggers FIQ and asserts nWDFIQ status flag
  - If FIQ service routine fails to clear nWDFIQ, then the next WDT time-out triggers a system reset.

Timers

The LH79524 and LH79525 incorporate three 16-bit independently programmable Timer modules. The timers are clocked by the system clock, but have an internal scaled-down system clock that is used for the Pulse Width Modulator (PWM) and compare functions.

All counters are incremented by an internal prescaled counter clock or external clock and can generate an overflow interrupt. All three timers have separate internal prescaled counter clocks, with either a common external clock or a prescaled version of the system clock.

- Timer 0 has five Capture Registers and two Compare Registers.
- Timer 1 and Timer 2 have two Capture and two Compare Registers each.

The Capture Registers have edge-selectable inputs and can generate an interrupt. The Compare Registers can force the compare output pin either HIGH or LOW upon a match.

The timers support a PWM Mode that uses the two Timer Compare Registers associated with a timer to create a PWM. Each timer can generate a separate interrupt. The interrupt becomes active if any enabled compare, capture, or overflow interrupt condition occurs. The interrupt remains active until all compare, capture, and overflow interrupts are cleared.

General Purpose Input/Output (GPIO)

The LH79524 provides up to 108 bits of programmable input/output, and the LH79525 provides 86 bits. Many of the GPIO pins are multiplexed with other signals. All GPIO feature:

- Individually programmable input/output pins
- All default to Input on power-up.
- LH79524
  - Ports A-I, K, L, and N: Bidirectional I/O (Port N is 4 bits wide)
  - Port J: Input only
  - Port M: Output only
- LH79525
  - Ports A-I: Bidirectional I/O
  - Port J: Input only
  - Port M: Output only (6 bits wide)

Boot Controller

The boot controller allows selection of the hardware device to be used for booting.

- Supports booting from 8-, 16-, or 32-bit devices, selectable via external pins at power-on reset
- Configures the byte lane boot state for nCS1, selectable via external pins at power-on reset.
- Supports booting from alternate external devices (e.g., NAND flash) via external pins on power-on reset
- Glueless interface to external NAND flash.

USB Device

The USB Device integrated into the LH79524/LH79525 is compliant with the USB 1.1 and 2.0 specification, and compatible with both the OpenHCI and Intel UHCI standards. The USB Device:

- Supports Full-Speed (12 Mbit/s) operation, and suspend and resume signaling
- Four Endpoints
- Bulk/Interrupt or Isochronous Transfers
- FIFO for each Endpoint direction (except EP0 which shares a FIFO between IN/OUT). FIFOs exist in 2464 × 8 RAM
- Supports DMA accesses to FIFO.

Power Supply Sequencing

When the linear regulator is *not* enabled, NXP recommends that the 1.8 V power supply be energized before the 3.3 V supply. If this is not possible, the 1.8 V supply may not lag the 3.3 V supply by more than 100 μs. If longer delay time is needed, it is recommended that the voltage difference between the two power supplies be within 1.5 V during power supply ramp up. To avoid a potential latchup condition, voltage should be applied to input pins only after the device is powered-on as described above.

DC/AC Specifications

Unless noted, all data provided are based on:

- -40°C to +85°C (Industrial temperature range)
- VDDC = 1.7 V to 1.9 V
- VDD = 3.0 V to 3.6 V, VDDA = 1.7 V to 1.9 V.

DC SPECIFICATIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
VIH	CMOS input HIGH voltage	2.0		5.5	V	CEN = 1
VIL	CMOS input LOW voltage			0.8	V	CEN = 1
VIT+	Positive Input threshold voltage (Schmitt pins)	2.0			V	CSEN = 1
VIT-	Negative Input threshold voltage (Schmitt pins)			0.8	V	CSEN = 1
VHYST	Schmitt trigger hysteresis		0.35		V	CSEN = 1
VOH[1]	Output drive (2 mA type)	2.6			V	IOH = -2 mA
	Output drive (4 mA type)	2.6			V	IOH = -4 mA
	Output drive (8 mA type)	2.6			V	IOH = -8 mA
	Output drive (12 mA type)	2.6			V	IOH = -12 mA
VOL[1]	Output drive (2 mA type)			0.4	V	IOL = 2 mA
	Output drive (4 mA type)			0.4	V	IOL = 4 mA
	Output drive (8 mA type)			0.4	V	IOL = 7 mA
	Output drive (12 mA type)	2.6			V	IOH = 12 mA
RIN	Input leakage pull-up/pull-down resistors		40		kΩ	VIN = VDD or GND (Calculate input leakage current at desired VDD)
IACTIVE	Active current		85		mA	Note 2
ISTANDBY	Standby current		50		mA	Notes 2, 3
ISLEEP	Sleep current		3.8		mA	
ISTOP1	Stop1 current		420		μA	
ISTOP2	Stop2 current		115		μA	RTC ON, Linear Regulator ON
ISTOP2	Stop2 current		95		μA	RTC OFF, Linear Regulator ON
ISTOP2	Stop2 current		45		μA	RTC ON, Linear Regulator OFF
ISTOP2	Stop2 current		25		μA	RTC OFF, Linear Regulator OFF

NOTES:

1. Table 2 details each pin's buffer type.
2. Running Typical Application over operating range.
3. Current measured with CPU stopped and all peripherals enabled

Linear Regulator DC Characteristics.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
IQUIESCENT	Quiescent Current		75		μA
ISLEEPLR	Current with Linear Regulator disabled		8		μA
IOLR	Output Current Range	0.0		200	mA
VOLR	Output Voltage, Linear Regulator		1.84		V

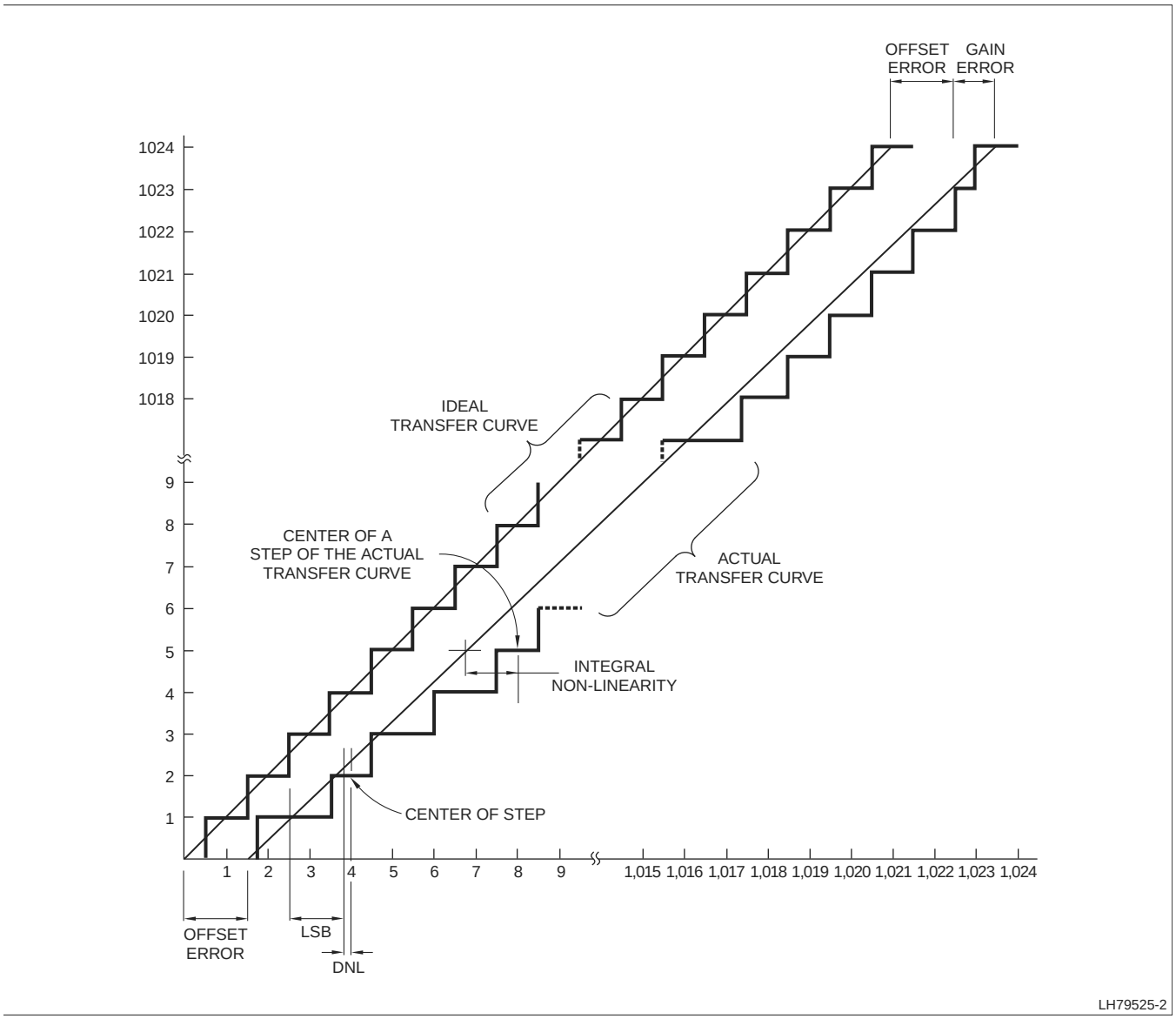


Figure 10. ADC Transfer Characteristics

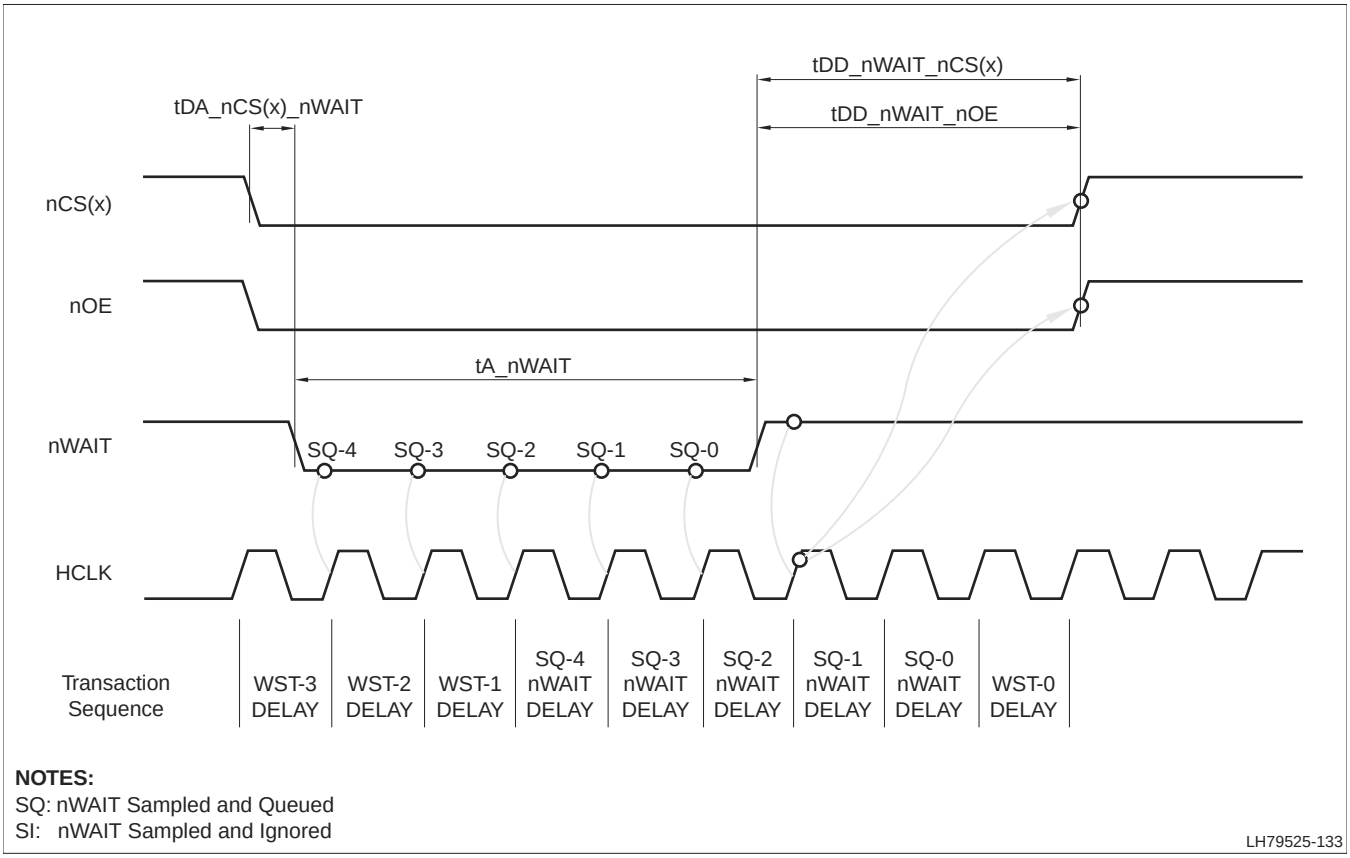


Figure 11. nWAIT Read Sequence (SWAITRDx = 3)

Table 16. nWAIT Read Sequence Parameter Definitions

PARAMETER	DESCRIPTION	MIN.	MAX.	UNIT [1]
tDA_nCS(x)_nWAIT	Delay from nCS(x) assertion to nWAIT assertion	0	16,365	HCLK periods
tDD_nWAIT_nCS(x)	Delay from nWAIT deassertion to nCS(x) deassertion		4	HCLK periods
tDD_nWAIT_nOE	Delay from nWAIT deassertion to nOE deassertion		4	HCLK periods
tA_nWAIT	Assertion time of nWAIT	2		HCLK periods

NOTES:
1. The timing relationship is specified as a cycle-based timing. Variations caused by clock jitter, power rail noise, and I/O conditioning will cause these timings to vary nominally. It is recommended that designers add a small margin to avoid possible corner-case conditions.
2. The Read Wait States register (SWAITRDx) must be set to a minimum value of 3.
3. For each rising clock edge (HCLK) that the assertion of nWAIT lags the assertion of nCSx, another read wait state (SWAITRDx) must be added to the minimum requirement.
4. nWAIT delay cycles are *not* added for all nWAIT assertions sampled prior to WST-3. These nWAIT assertions are ignored.
5. nWAIT delay cycles are added for all nWAIT assertions sampled from WST-3 until the de-assertion of nWAIT. nWAIT delay cycles are added once the wait state countdown has reached WST-1.
6. Once nWAIT is sampled high, the current memory transaction is queued to complete.
7. Since static and dynamic memory cannot be accessed at the same time, any prolonged access (either due to nWAIT or the Extended Wait Register) that causes an SDRAM refresh failure may cause SDRAM data to be lost.
8. Timing assumes Output Enable Delay register (SWAITOENx) is programmed to 0.

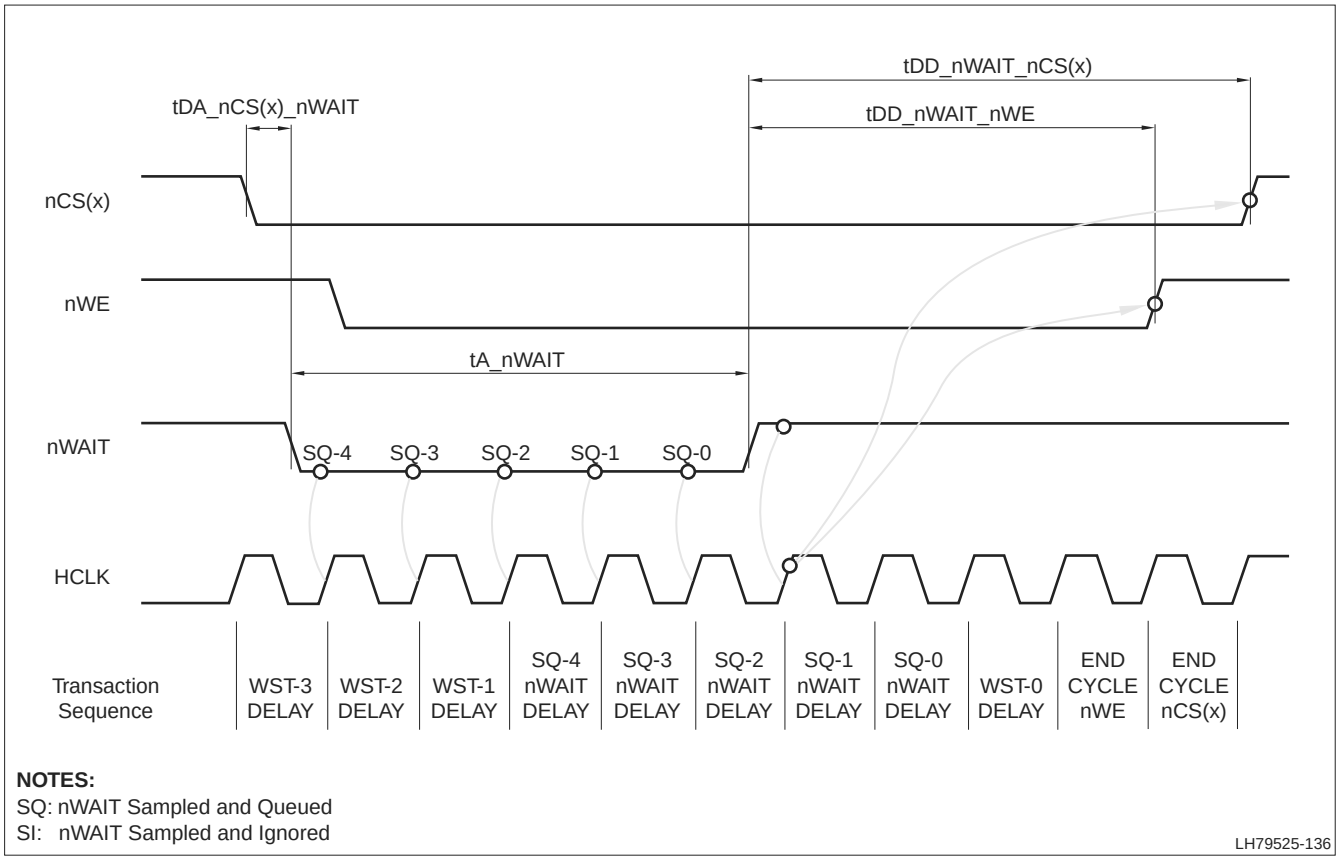


Figure 14. nWAIT Write Sequence (SWAITWRx = 3)

Table 17. nWAIT Write Sequence Parameter Definitions

PARAMETER	DESCRIPTION	MIN.	MAX.	UNIT[1]
tIDA_nCS(x)_nWAIT	Delay from nCS(x) assertion to nWAIT assertion	0	16,365	HCLK periods
tDD_nWAIT_nCS(x)	Delay from nWAIT deassertion to nCS(x) deassertion		6	HCLK periods
tDD_nWAIT_nWE	Delay from nWAIT deassertion to nWE deassertion		5	HCLK periods
tA_nWAIT	Assertion time of nWAIT	2		HCLK periods

NOTES:

1. The timing relationship is specified as a cycle-based timing. Variations caused by clock jitter, power rail noise, and I/O conditioning will cause these timings to vary nominally. It is recommended that designers add a small margin to avoid possible corner-case conditions.
2. The Write Wait States register (SWAITWRx) must be set to a minimum value of 3.
3. For each rising clock edge (HCLK) that the assertion of nWAIT lags the assertion of nCSx, another write wait state (SWAITRDx) must be added to the minimum requirement.
4. nWAIT delay cycles are *not* added for all nWAIT assertions sampled prior to WST-3. These nWAIT assertions are ignored.
5. nWAIT delay cycles are added for all nWAIT assertions sampled from WST-3 until the de-assertion of nWAIT. nWAIT delay cycles are added once the wait state countdown has reached WST-1.
6. Once nWAIT is sampled high, the current memory transaction is queued to complete.
7. Since static and dynamic memory cannot be accessed at the same time, any prolonged access (either due to nWAIT or the Extended Wait Register) that causes an SDRAM refresh failure may cause SDRAM data to be lost.
8. Timing assumes Write Enable Delay register (SWAITWENx) is programmed to 0.

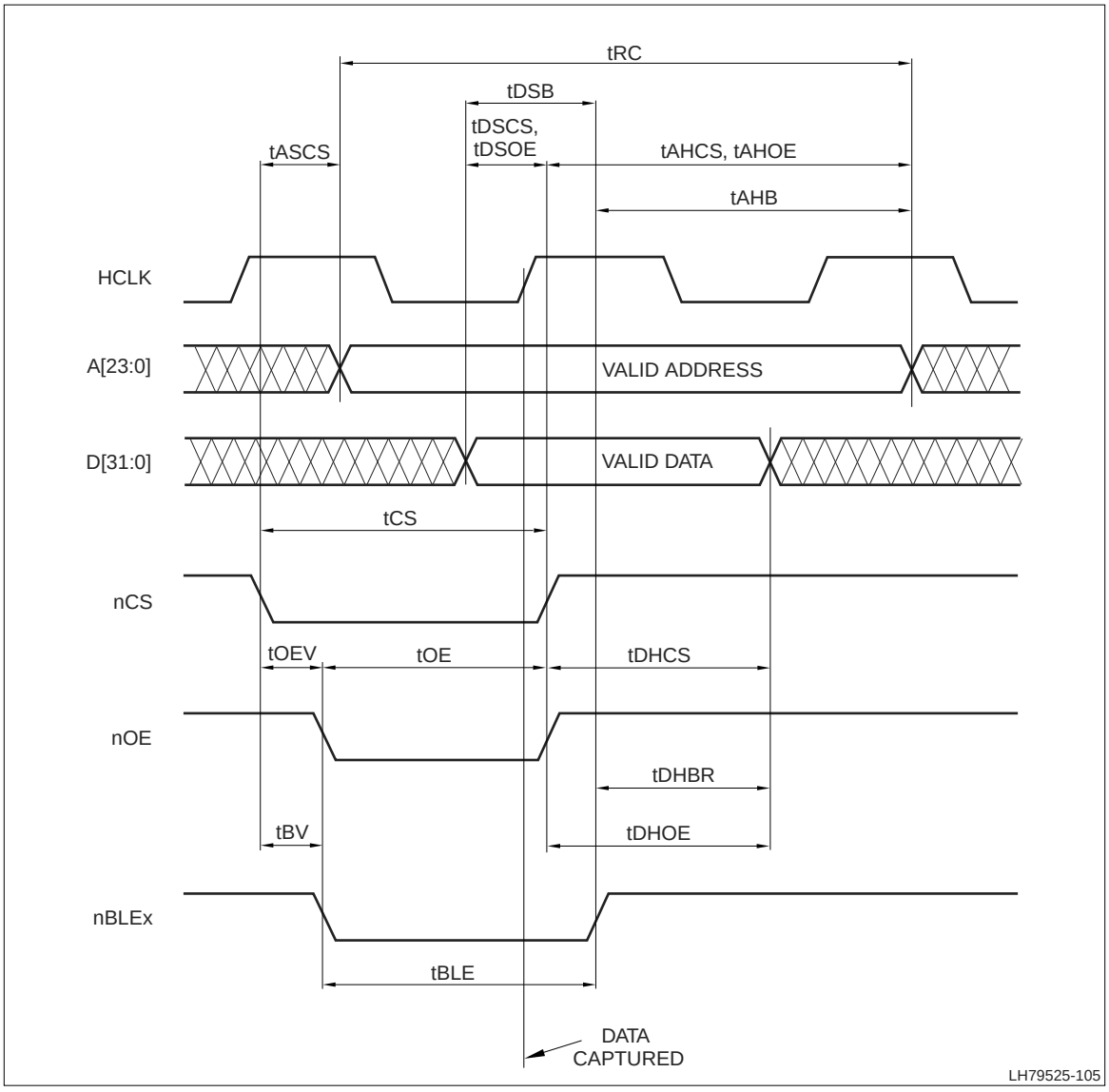


Figure 17. External Static Memory Read, Zero Wait States

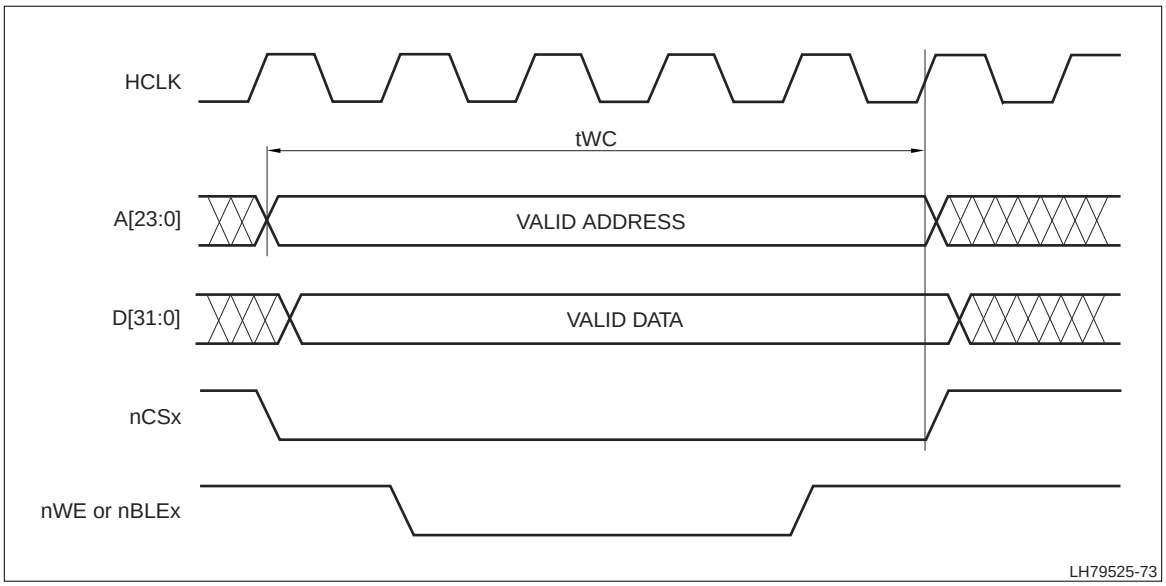
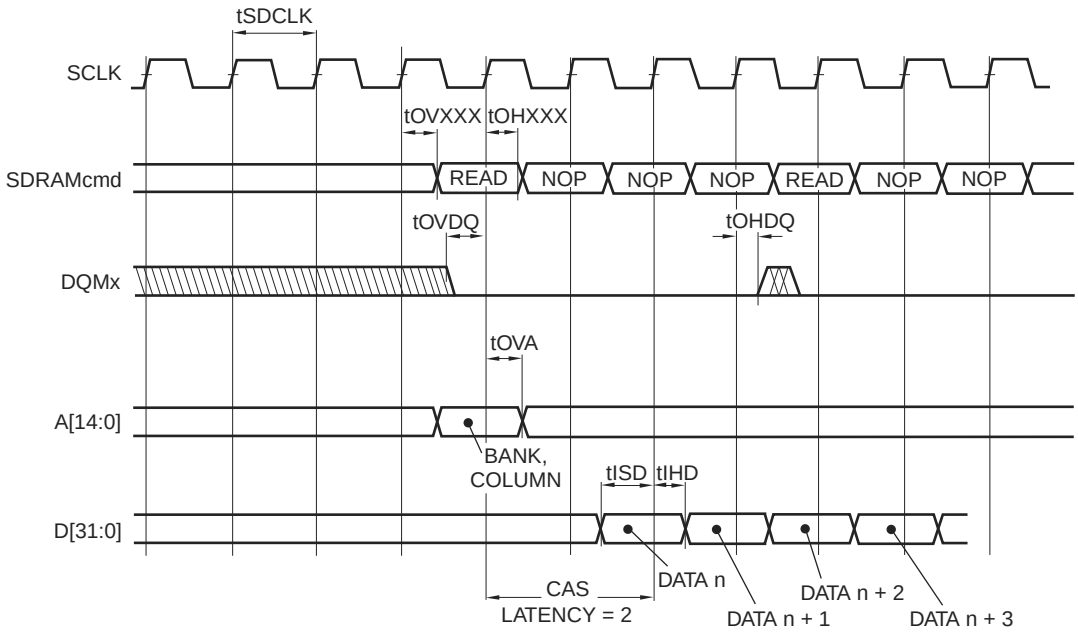


Figure 20. External Static Memory Write with Two Wait States

SDRAM MEMORY CONTROLLER WAVEFORMS

Figure 21 shows the waveform and timing for an SDRAM Burst Read (page already open). Figure 22 shows the waveform and timing for SDRAM to Activate a Bank and Write.



NOTES:
1. SDRAMcmd is the combination of nRAS, nCAS, nSDWE, and nSDCS(X).
2. tOVXXX represents tOVRA, tOVCA, tOVSDW, or tOVSC.
3. tOHXXX represents tOHRA, tOHCA, tOHSDW, or tOHSC.
4. SDCKE is HIGH.

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Figure 21. SDRAM Burst Read

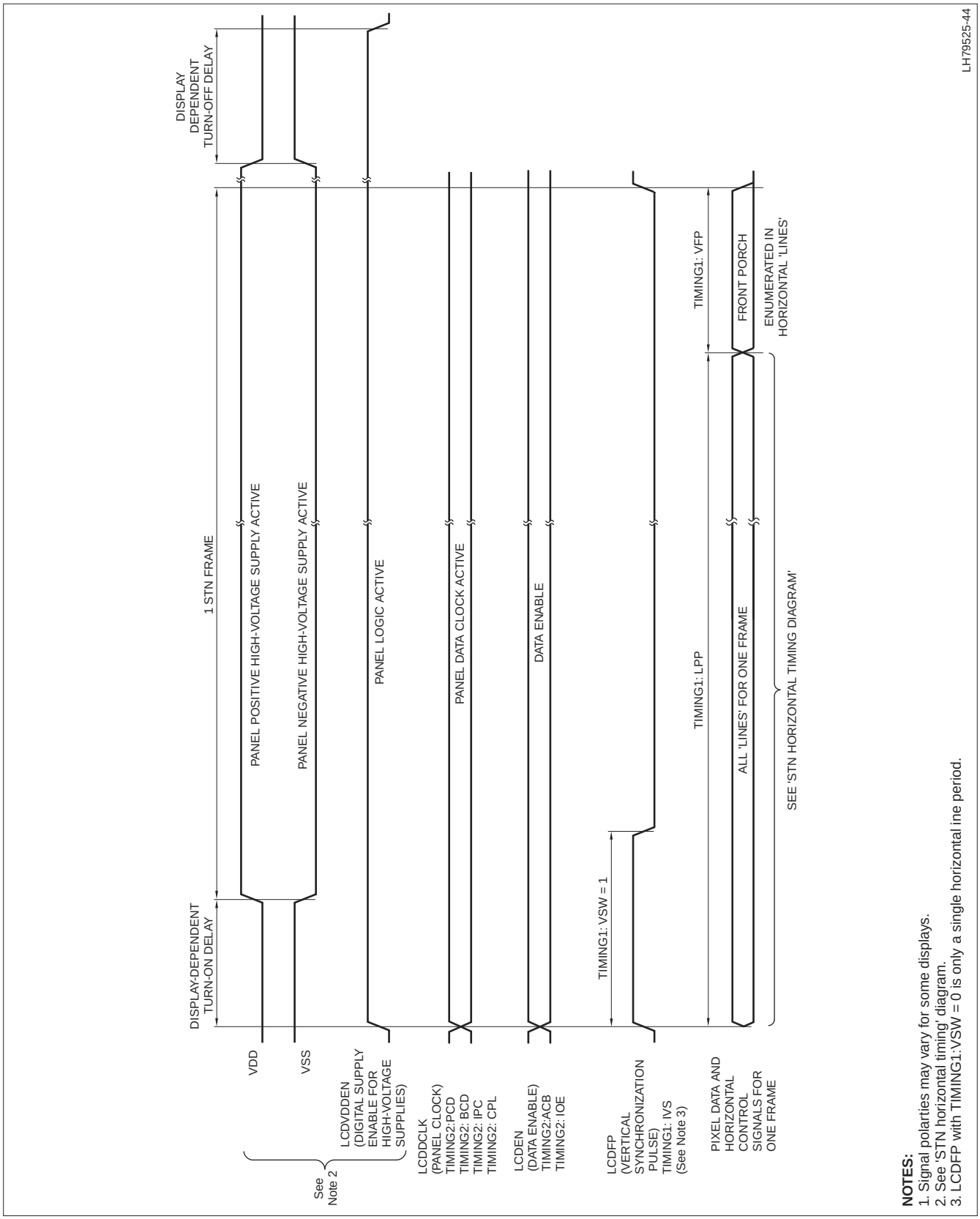

Figure 29. STN Vertical Timing

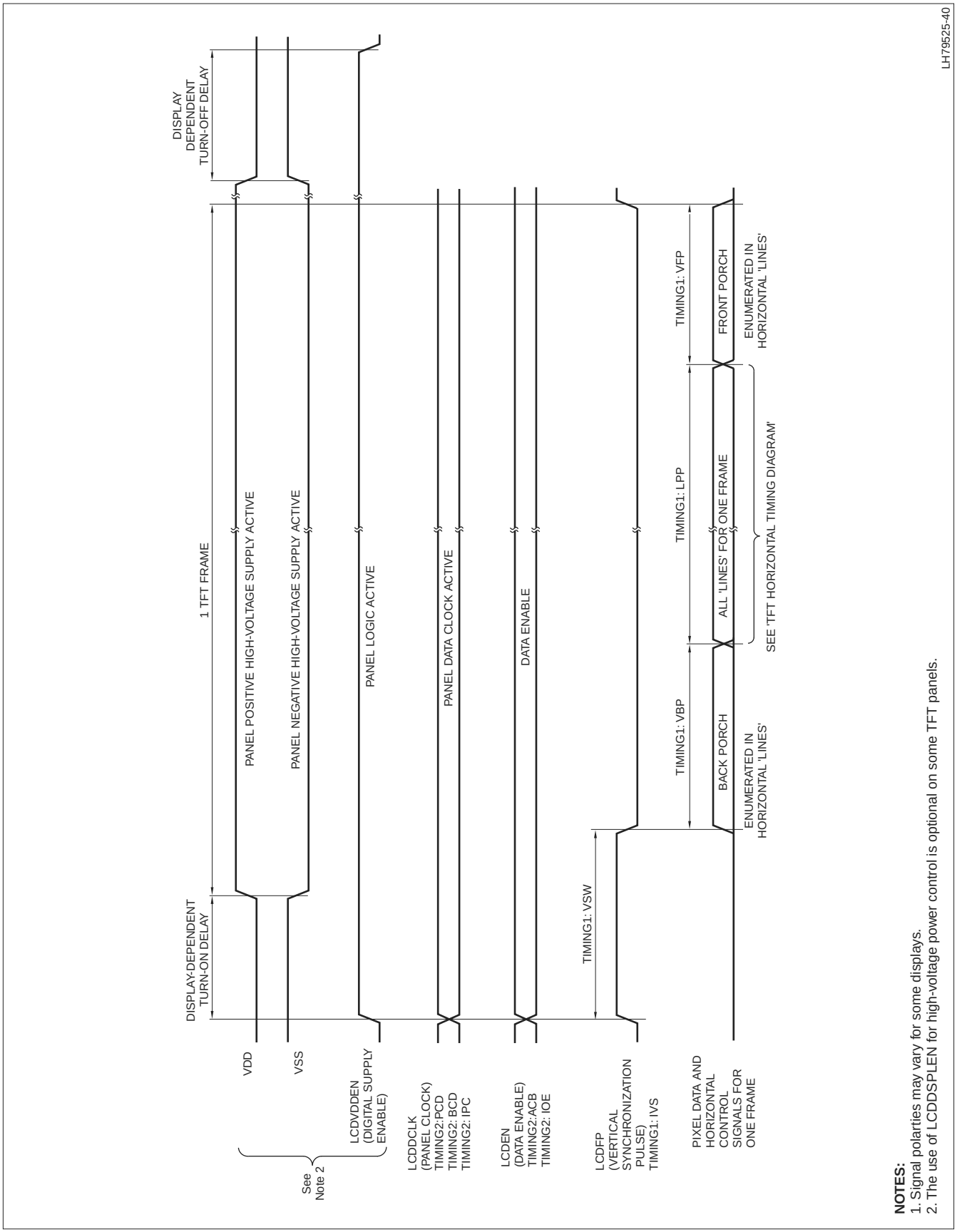

Figure 30. TFT Horizontal Timing

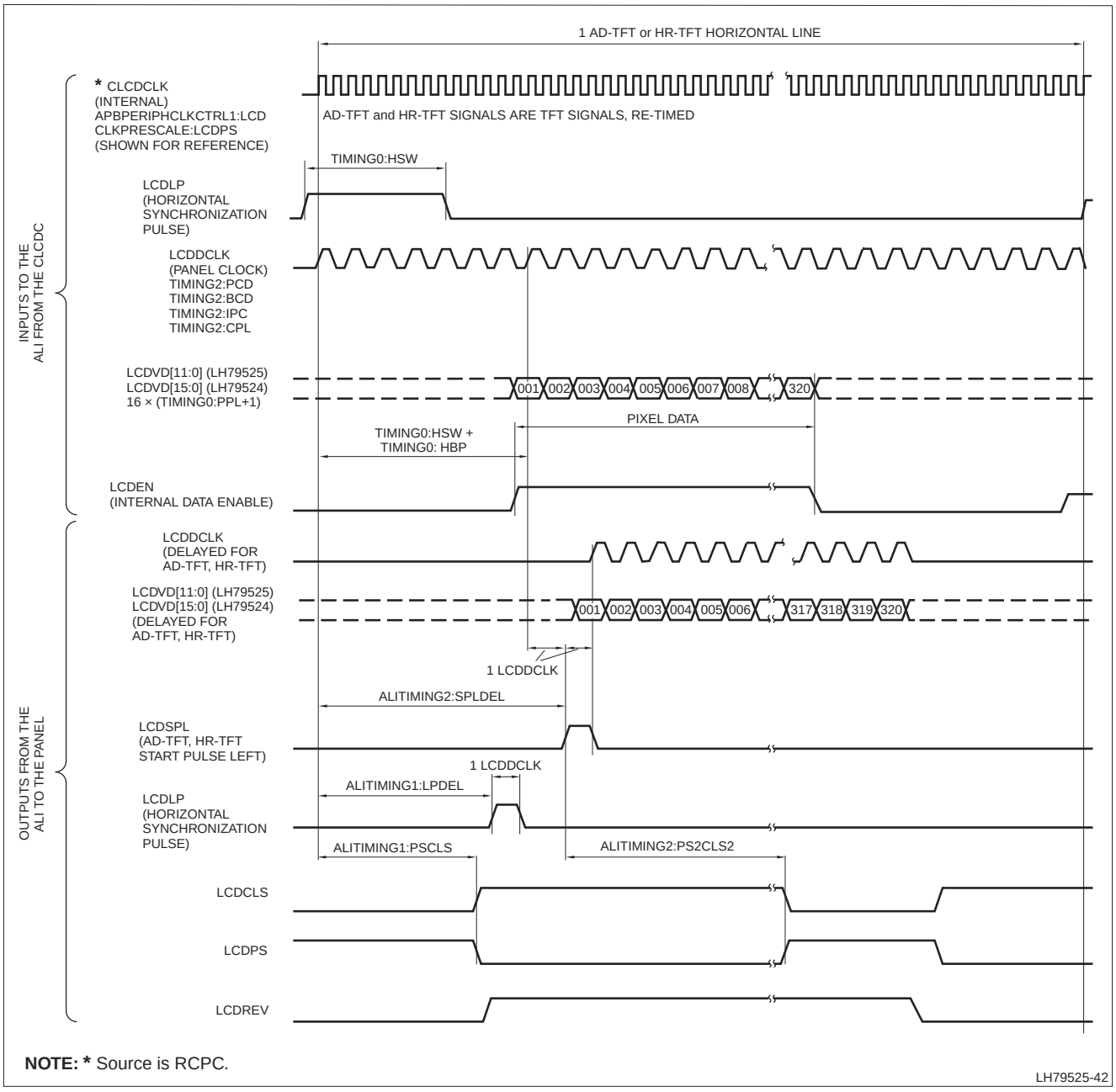

Figure 32. AD-TFT, HR-TFT Horizontal Timing

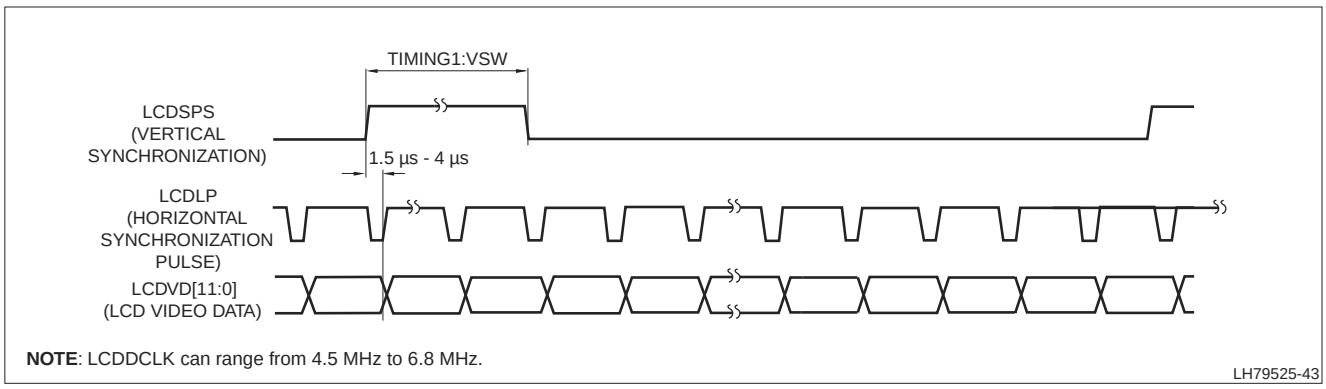

Figure 33. AD-TFT, HR-TFT Vertical Timing

Ethernet MAC Controller Waveforms

The timing for the EMC is presented in the following two illustrations. Figure 35 shows an Ethernet transmit and Figure 36 shows an Ethernet receive.

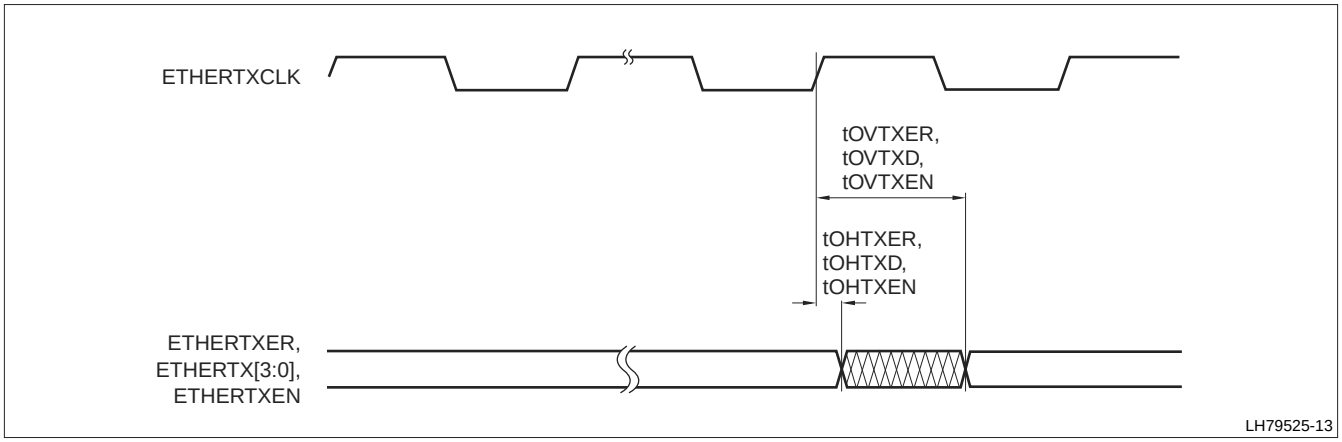

Figure 35. Ethernet Transmit Timing

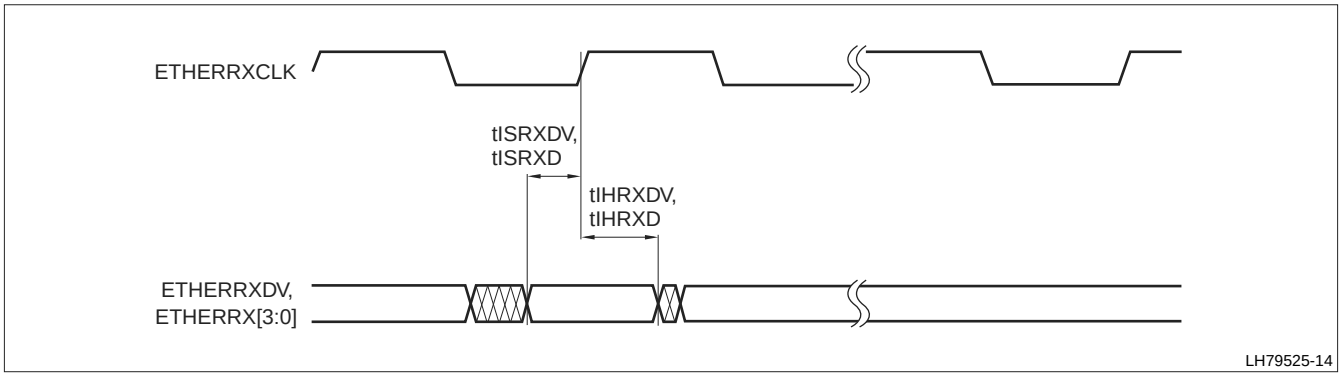

Figure 36. Ethernet Receive Timing

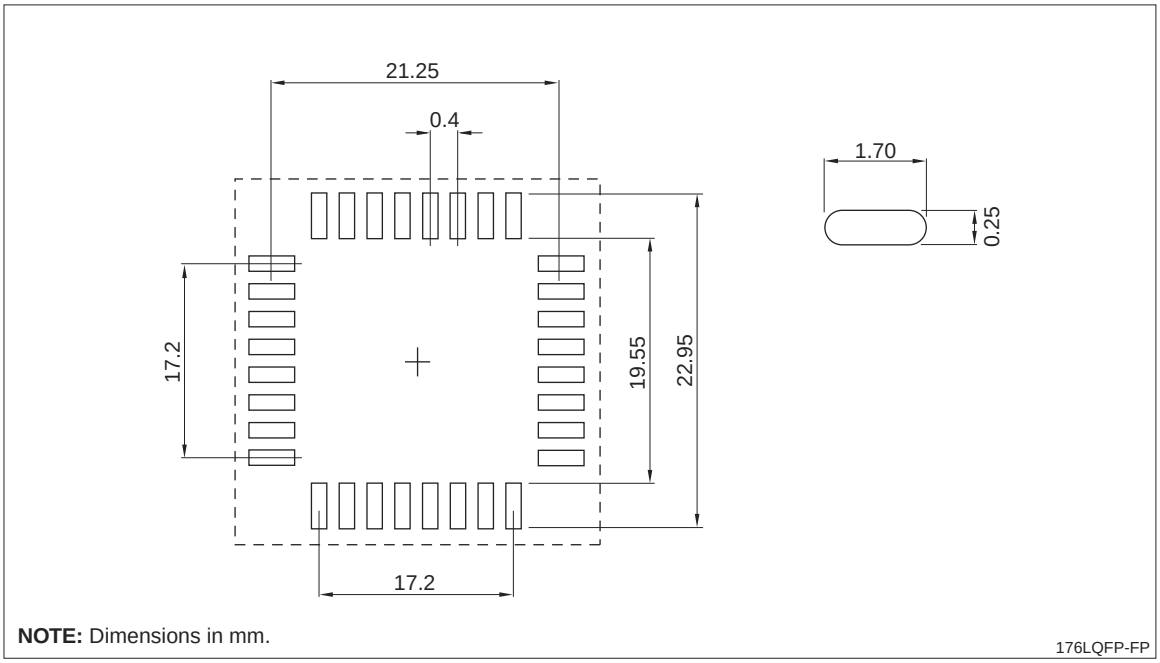

Figure 43. LH79525: LQFP176 PCB Footprint

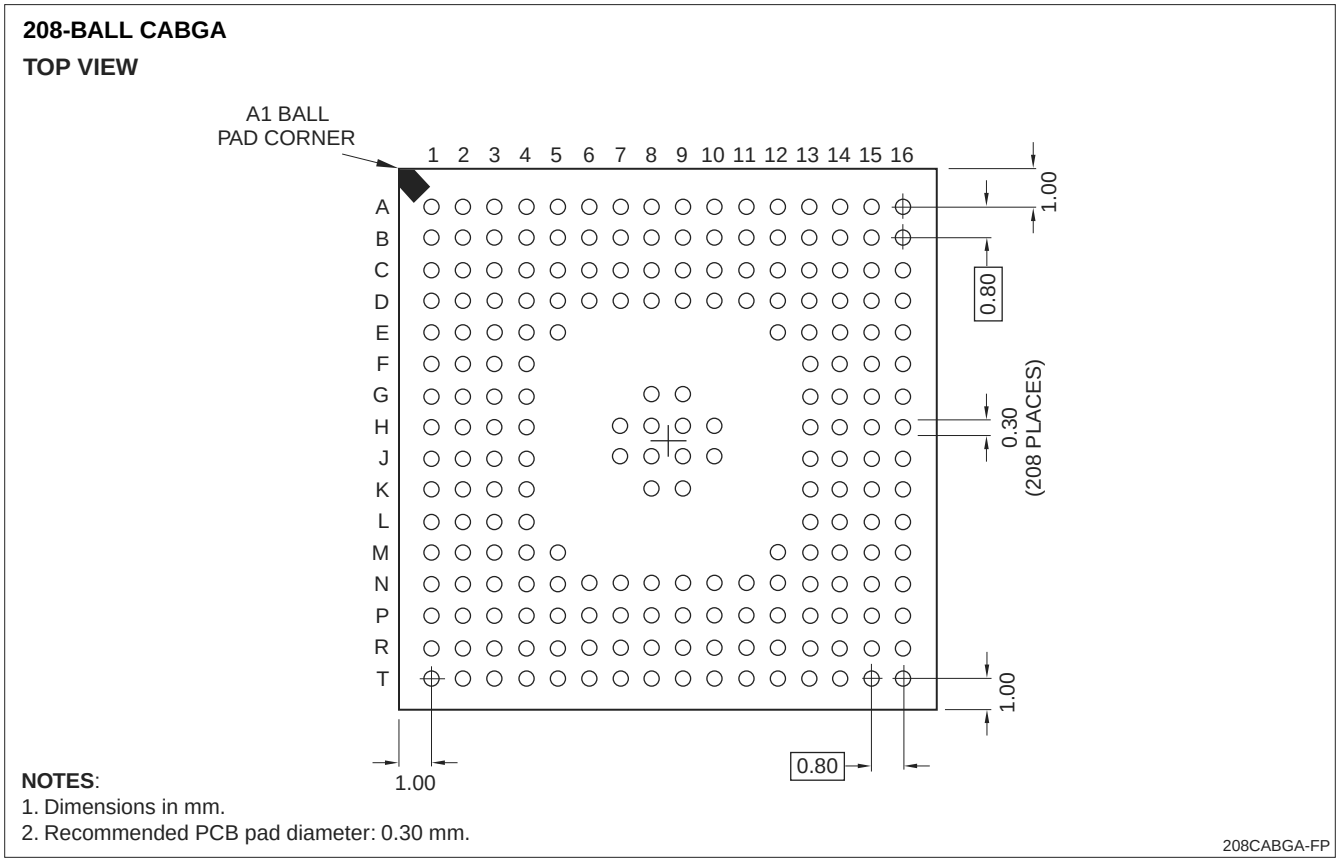

Figure 44. LH79524: LFBGA208 PCB Footprint

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