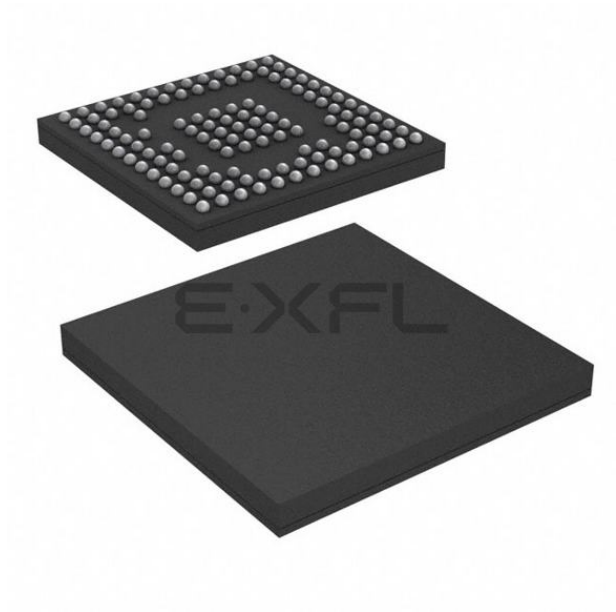

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	65
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D - 12b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	125-VFBGA
Supplier Device Package	125-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32pg12b500f1024gl125-b

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Con-verter	GPIO	Package	Temp Range
EFM32PG12B500F1024GL125-B	1024	256	Yes	65	BGA125	-40 to +85
EFM32PG12B500F1024IL125-B	1024	256	Yes	65	BGA125	-40 to +125
EFM32PG12B500F1024GM48-B	1024	256	Yes	33	QFN48	-40 to +85
EFM32PG12B500F1024IM48-B	1024	256	Yes	33	QFN48	-40 to +125

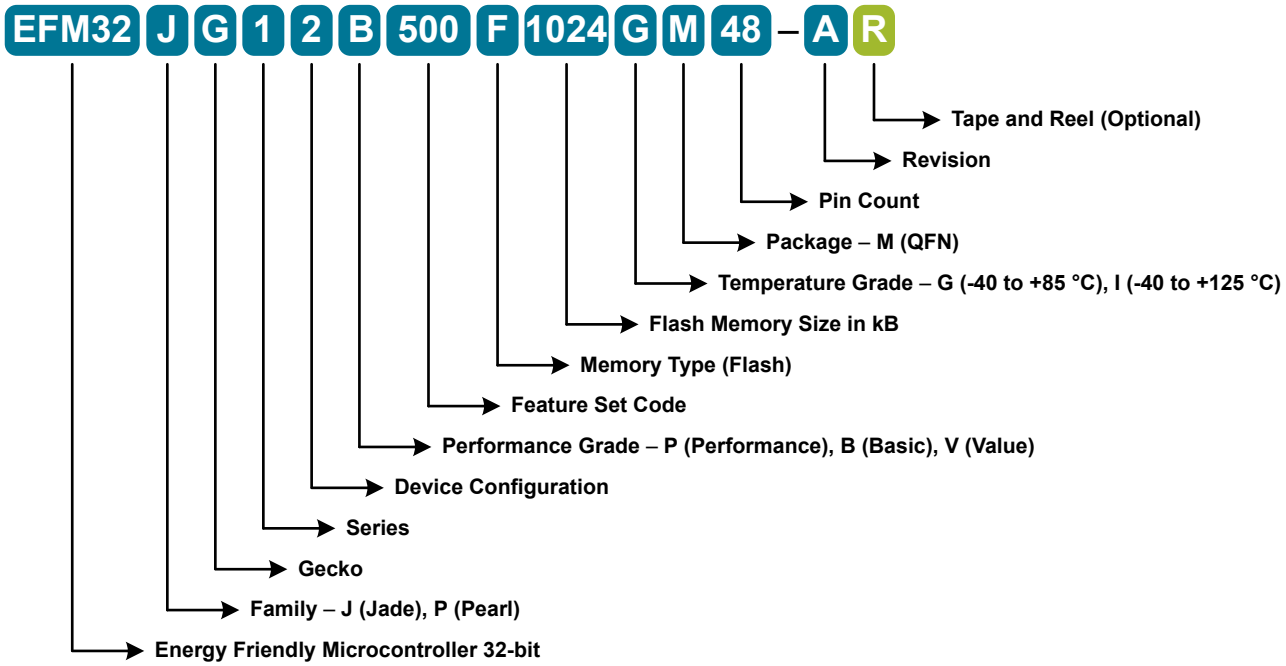

Figure 2.1. OPN Decoder

3. System Overview

3.1 Introduction

The EFM32PG12 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the EFM32PG12 Reference Manual.

A block diagram of the EFM32PG12 family is shown in Figure 3.1 Detailed EFM32PG12 Block Diagram on page 3. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

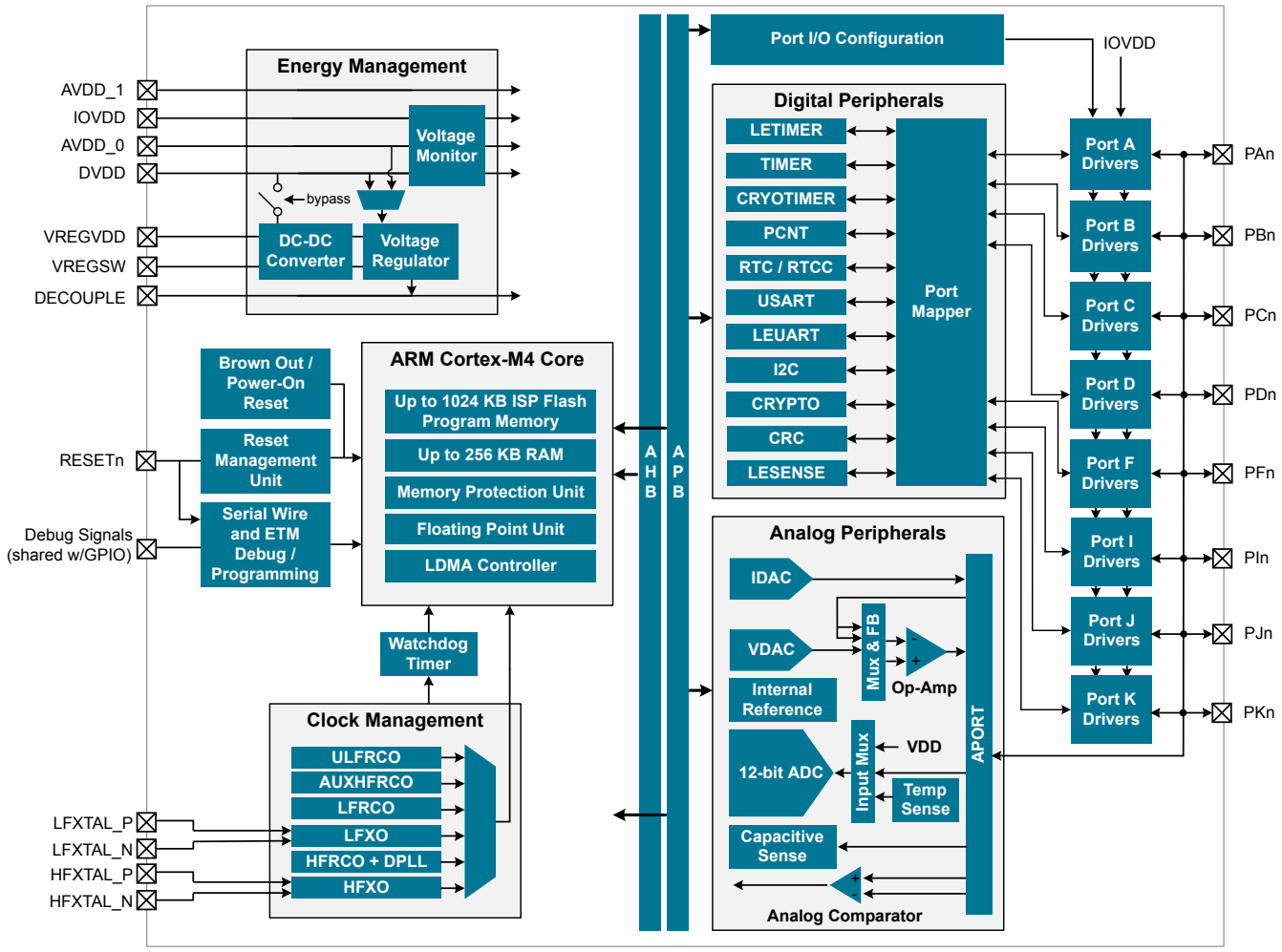

Figure 3.1. Detailed EFM32PG12 Block Diagram

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:
1. CMU_HFXOCTRL_LOWPOWER=1.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.6 Wake Up Times

Table 4.8. Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wakeup time from EM1	t_{EM1_WU}		—	3	—	AHB Clocks
Wake up from EM2	t_{EM2_WU}	Code execution from flash	—	10.1	—	µs
		Code execution from RAM	—	3.2	—	µs
Wake up from EM3	t_{EM3_WU}	Code execution from flash	—	10.1	—	µs
		Code execution from RAM	—	3.2	—	µs
Wake up from EM4H[1]	t_{EM4H_WU}	Executing from flash	—	80	—	µs
Wake up from EM4S[1]	t_{EM4S_WU}	Executing from flash	—	291	—	µs
Time from release of reset source to first instruction execution.	t_{RESET}	Soft Pin Reset released	—	43	—	µs
		Any other reset released	—	350	—	µs
Power mode scaling time	t_{SCALE}	VSCALE0 to VSCALE2, HFCLK = 19 MHz[3]	—	31.8	—	µs
		VSCALE2 to VSCALE0, HFCLK = 19 MHz[2]	—	4.3	—	µs

Note:
1. Time from wakeup request until first instruction is executed. Wakeup results in device reset.
2. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 µs + 29 HFCLKs.
3. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 µs + 28 HFCLKs.

4.1.8.2 High-Frequency Crystal Oscillator (HFXO)

Table 4.11. High-Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXO}		38	38.4	40	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO_38M4}	Crystal frequency 38.4 MHz	—	—	60	Ω
Supported range of crystal load capacitance [1]	C_{HFXO_CL}		6	—	12	pF
On-chip tuning cap range [2]	C_{HFXO_T}	On each of HFXTAL_N and HFXTAL_P pins	TBD	20	TBD	pF
On-chip tuning capacitance step	SS_{HFXO}		—	0.04	—	pF
Startup time	t_{HFXO}	38.4 MHz, ESR = 50 Ohm, C_L = 10 pF	—	300	—	µs
Frequency tolerance for the crystal	FT_{HFXO}	38.4 MHz, ESR = 50 Ohm, C_L = 10 pF	-40	—	40	ppm

Note:
1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be C_{HFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal. .

4.1.8.3 Low-Frequency RC Oscillator (LFRCO)

Table 4.12. Low-Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}	ENVREF[2] = 1	TBD	32.768	TBD	kHz
		ENVREF[2] = 1, T_{AMB} > 85 °C	TBD	32.768	TBD	kHz
		ENVREF[2] = 0	TBD	32.768	TBD	kHz
		ENVREF[2] = 0, T_{AMB} > 85 °C	TBD	32.768	TBD	kHz
Startup time	t_{LFRCO}		—	500	—	µs
Current consumption [1]	I_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	370	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	520	—	nA

Note:
1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
2. in CMU_LFRCOCTRL register.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output fall time, From 70% to 30% of V_{IO}	t_{IOOF}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE[1] = 0x6	—	1.8	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	4.5	—	ns
Output rise time, From 30% to 70% of V_{IO}	t_{IOOR}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE = 0x6[1]	—	2.2	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	7.4	—	ns

Note:
1. In GPIO_Pn_CTRL register.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC clock frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	$f_{ADCRATE}$		—	—	1	Msps
Conversion time[1]	$t_{ADCCONV}$	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	$t_{ADCSTART}$	WARMUPMODE[4] = NORMAL	—	—	5	µs
		WARMUPMODE[4] = KEEPIN-STANDBY	—	—	2	µs
		WARMUPMODE[4] = KEEPINSLO-WACC	—	—	1	µs
SNDR at 1Msps and f_{IN} = 10kHz	$SNDR_{ADC}$	Internal reference, 2.5 V full-scale, differential (-1.25, 1.25)	TBD	67	—	dB
		vrefp_in = 1.25 V direct mode with 2.5 V full-scale, differential	—	68	—	dB
Spurious-free dynamic range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution, No missing co-des	TBD	—	TBD	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	TBD	—	TBD	LSB
Offset error	$V_{ADCOFFSETERR}$		TBD	0	TBD	LSB
Gain error in ADC	$V_{ADCGAIN}$	Using internal reference	—	-0.2	TBD	%
		Using external reference	—	-1	—	%
Temperature sensor slope	V_{TS_SLOPE}		—	-1.84	—	mV/°C

Note:

1. Derived from ADCCLK.
2. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
3. In ADCn_BIASPROG register.
4. In ADCn_CNTL register.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slew rate[5]	SR	DRIVESTRENGTH = 3, INCBW=1[3]	—	4.7	—	V/µs
		DRIVESTRENGTH = 3, INCBW=0	—	1.5	—	V/µs
		DRIVESTRENGTH = 2, INCBW=1[3]	—	1.27	—	V/µs
		DRIVESTRENGTH = 2, INCBW=0	—	0.42	—	V/µs
		DRIVESTRENGTH = 1, INCBW=1[3]	—	0.17	—	V/µs
		DRIVESTRENGTH = 1, INCBW=0	—	0.058	—	V/µs
		DRIVESTRENGTH = 0, INCBW=1[3]	—	0.044	—	V/µs
		DRIVESTRENGTH = 0, INCBW=0	—	0.015	—	V/µs
Startup time[6]	T_{START}	DRIVESTRENGTH = 3	—	—	TBD	µs
		DRIVESTRENGTH = 2	—	—	TBD	µs
		DRIVESTRENGTH = 1	—	—	TBD	µs
		DRIVESTRENGTH = 0	—	—	TBD	µs
Input offset voltage	V_{OSI}	DRIVESTRENGTH = 2 or 3, T_J = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 1 or 0, T_J = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 2 or 3, across operating temperature range	TBD	—	TBD	mV
		DRIVESTRENGTH = 1 or 0, across operating temperature range	TBD	—	TBD	mV
DC power supply rejection ratio[9]	$PSRR_{DC}$	Input referred	—	70	—	dB
DC common-mode rejection ratio[9]	$CMRR_{DC}$	Input referred	—	70	—	dB
Total harmonic distortion	THD_{OPA}	DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	—	90	—	dB
		DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	—	90	—	dB

4.1.21 USART SPI

SPI Master Timing

Table 4.30. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [3] [2]	t_{SCLK}		2 * $t_{HFPERCLK}$	—	—	ns
CS to MOSI [1] [3]	t_{CS_MO}		0	—	13.3	ns
SCLK to MOSI [1] [3]	t_{SCLK_MO}		0	—	8	ns
MISO setup time [1] [3]	t_{SU_MI}	IOVDD = 1.62 V	90	—	—	ns
		IOVDD = 3.0 V	40	—	—	ns
MISO hold time [1] [3]	t_{H_MI}		10	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

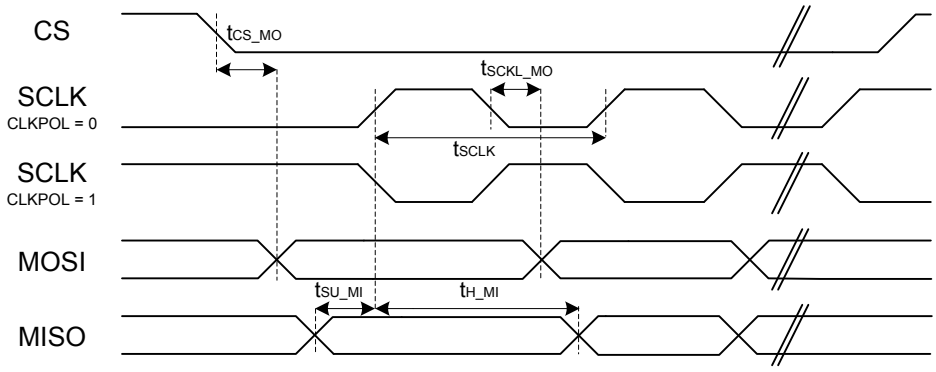

Figure 4.1. SPI Master Timing Diagram

SPI Slave Timing

Table 4.31. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [3] [2]	t_{SCLK}		8 * $t_{HFPERCLK}$	—	—	ns
SCLK high time [1] [3] [2]	t_{SCLK_HI}		3 * $t_{HFPERCLK}$	—	—	ns
SCLK low time [1] [3] [2]	t_{SCLK_LO}		3 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1] [3]	$t_{CS\_ACT\_MI}$		4	—	50	ns
CS disable to MISO [1] [3]	$t_{CS\_DIS\_MI}$		4	—	50	ns
MOSI setup time [1] [3]	t_{SU_MO}		4	—	—	ns
MOSI hold time [1] [3] [2]	t_{H_MO}		3 + 2 * $t_{HFPERCLK}$	—	—	ns
SCLK to MISO [1] [3] [2]	t_{SCLK_MI}		16 + $t_{HFPERCLK}$	—	66 + 2 * $t_{HFPERCLK}$	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

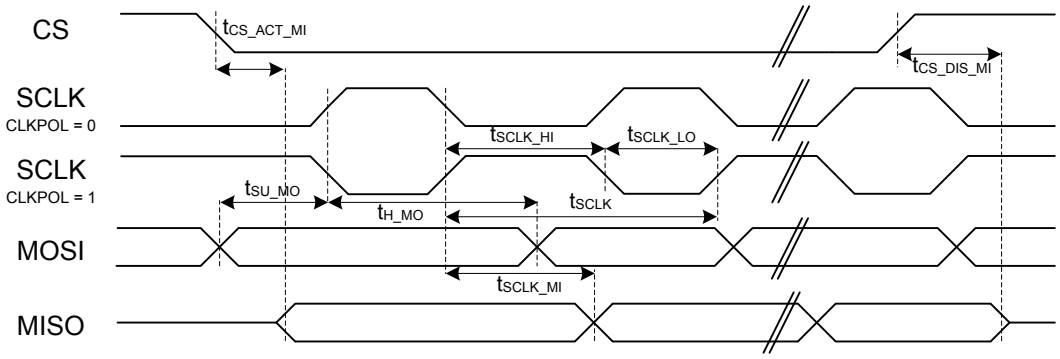

Figure 4.2. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

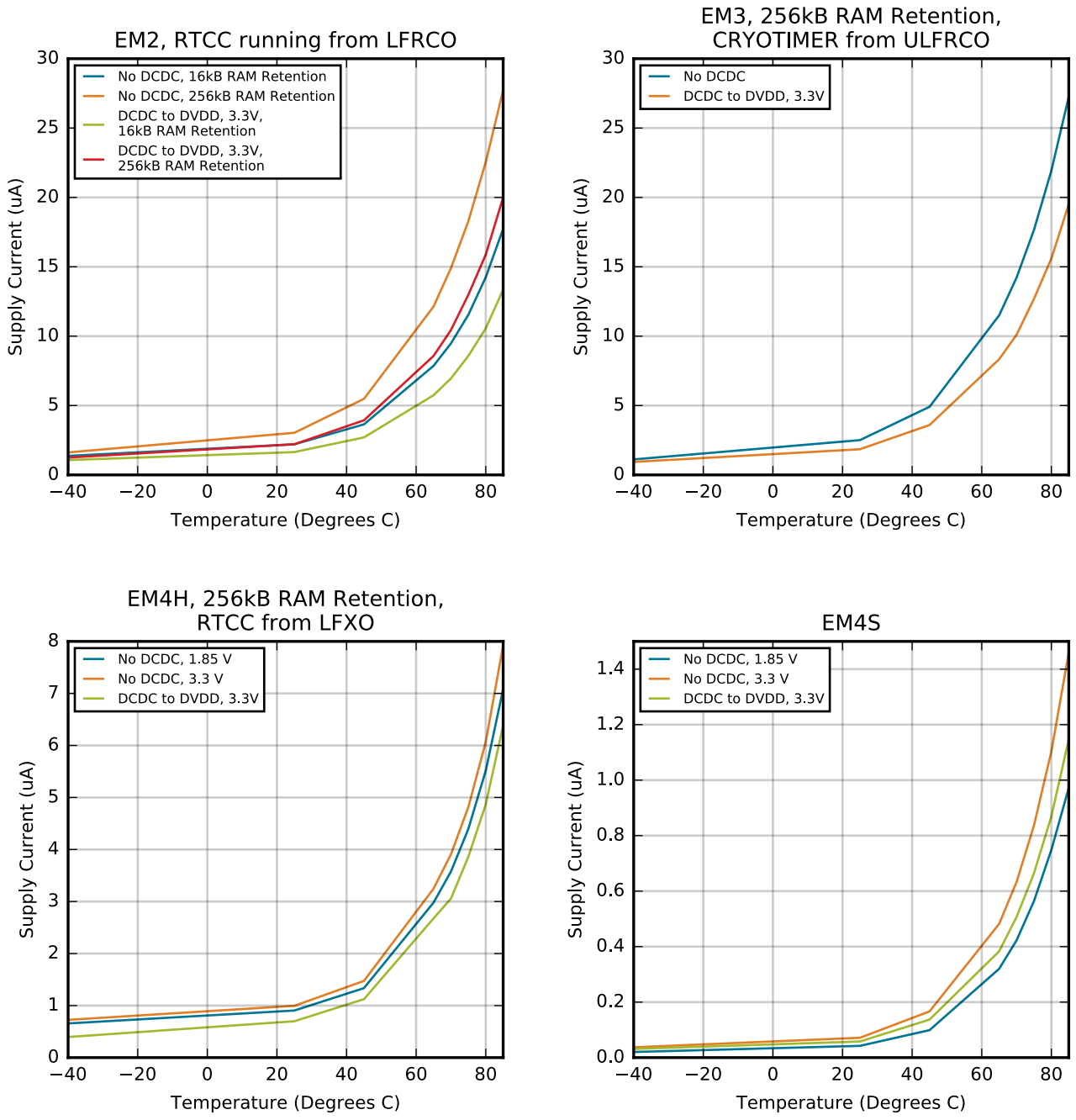

Figure 4.5. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Temperature

5. Typical Connection Diagrams

5.1 Power

Typical power supply connections for direct supply, without using the internal DC-DC converter, are shown in Figure 5.1 EFM32PG12 Typical Application Circuit, Direct Supply, No DC-DC Converter on page 59.

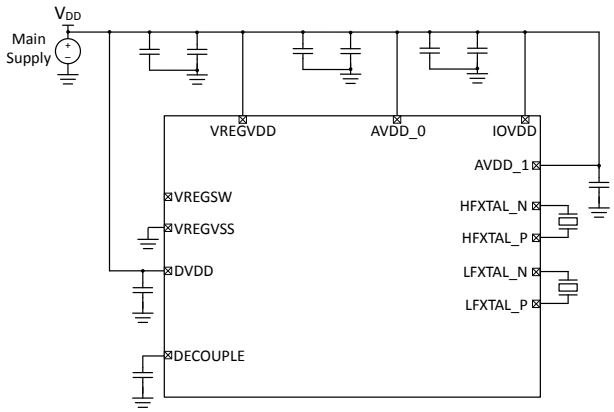

Figure 5.1. EFM32PG12 Typical Application Circuit, Direct Supply, No DC-DC Converter

A typical application circuit using the internal DC-DC converter is shown in Figure 5.2 EFM32PG12 Typical Application Circuit Using the DC-DC Converter on page 59. The MCU operates from the DC-DC converter supply.

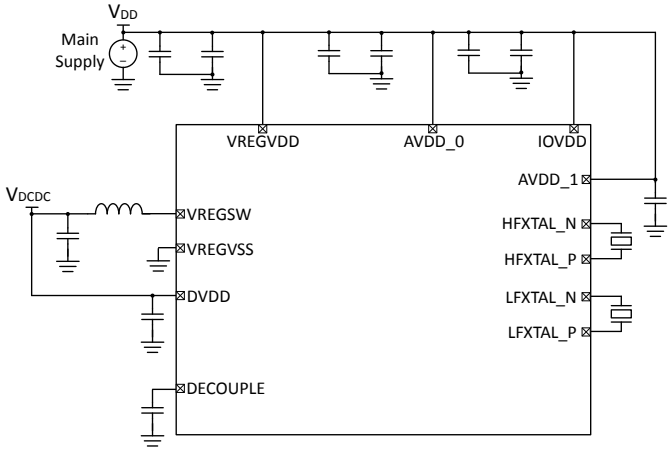

Figure 5.2. EFM32PG12 Typical Application Circuit Using the DC-DC Converter

5.2 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002: "Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
M9	PD9	BUSCY BUSDX	TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 WTIM0_CC1 #31 WTIM0_CC2 #29 WTIM0_CDTI0 #25 WTIM0_CDTI1 #23 WTIM0_CDTI2 #21 WTIM1_CC0 #17 WTIM1_CC1 #15 WTIM1_CC2 #13 WTIM1_CC3 #11 LE-TIM0_OUT0 #17 LE-TIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16	US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 US3_TX #1 US3_RX #0 US3_CLK #31 US3_CS #30 US3_CTS #29 US3_RTS #28 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16	CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17 LES_CH1
M10	PD11	BUSCY BUSDX	TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 WTIM0_CC2 #31 WTIM0_CDTI0 #27 WTIM0_CDTI1 #25 WTIM0_CDTI2 #23 WTIM1_CC0 #19 WTIM1_CC1 #17 WTIM1_CC2 #15 WTIM1_CC3 #13 LE-TIM0_OUT0 #19 LE-TIM0_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18	US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 US3_TX #3 US3_RX #2 US3_CLK #1 US3_CS #0 US3_CTS #31 US3_RTS #30 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18	PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19 LES_CH3

6.1.1 EFM32PG12B5xx in BGA125 GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters (A, B, C...), with individual pins on each port indicated by a number from 15 down to 0.

Table 6.2. EFM32PG12B5xx in BGA125 GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	PA9 (5V)	PA8 (5V)	PA7 (5V)	PA6 (5V)	PA5 (5V)	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10 (5V)	PB9 (5V)	PB8 (5V)	PB7 (5V)	PB6 (5V)	-	-	-	-	-	-
Port C	-	-	-	-	PC11 (5V)	PC10 (5V)	PC9 (5V)	PC8 (5V)	PC7 (5V)	PC6 (5V)	PC5 (5V)	PC4 (5V)	PC3 (5V)	PC2 (5V)	PC1 (5V)	PC0 (5V)
Port D	PD15	PD14	PD13	PD12 (5V)	PD11 (5V)	PD10 (5V)	PD9 (5V)	PD8 (5V)	-	-	-	-	-	-	-	-
Port F	PF15 (5V)	PF14 (5V)	PF13 (5V)	PF12 (5V)	PF11 (5V)	PF10 (5V)	PF9 (5V)	PF8 (5V)	PF7 (5V)	PF6 (5V)	PF5 (5V)	PF4 (5V)	PF3 (5V)	PF2 (5V)	PF1 (5V)	PF0 (5V)
Port I	-	-	-	-	-	-	-	-	-	-	-	-	PI3 (5V)	PI2 (5V)	PI1 (5V)	PI0 (5V)
Port J	PJ15 (5V)	PJ14 (5V)	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port K	-	-	-	-	-	-	-	-	-	-	-	-	-	PK2 (5V)	PK1 (5V)	PK0

Note:
1. GPIO with 5V tolerance are indicated by (5V).

Table 6.3. EFM32PG12B5xx in QFN48 Device Pinout

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground			
1	PF0	BUSBY BUSAX	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 WTIM0_CDTI1 #30 WTIM0_CDTI2 #28 WTIM1_CC0 #24 WTIM1_CC1 #22 WTIM1_CC2 #20 WTIM1_CC3 #18 LE-TIM0_OUT0 #24 LE-TIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 US2_TX #14 US2_RX #13 US2_CLK #12 US2_CS #11 US2_CTS #10 US2_RTS #9 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK BOOT_TX
2	PF1	BUSAY BUSBX	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 WTIM0_CDTI1 #31 WTIM0_CDTI2 #29 WTIM1_CC0 #25 WTIM1_CC1 #23 WTIM1_CC2 #21 WTIM1_CC3 #19 LE-TIM0_OUT0 #25 LE-TIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 US2_TX #15 US2_RX #14 US2_CLK #13 US2_CS #12 US2_CTS #11 US2_RTS #10 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS BOOT_RX

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
ETM_TD2	0: PF11 1: PA8 2: PB7 3: PC9								Embedded Trace Module ETM data 2.
ETM_TD3	0: PF12 1: PA9 2: PB8 3: PC10								Embedded Trace Module ETM data 3.
GPIO_EM4WU0	0: PF2								Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PF7								Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PD14								Pin can be used to wake the system up from EM4
GPIO_EM4WU8	0: PA3								Pin can be used to wake the system up from EM4
GPIO_EM4WU9	0: PB13								Pin can be used to wake the system up from EM4
GPIO_EM4WU12	0: PC10								Pin can be used to wake the system up from EM4
I2C0_SCL	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	I2C0 Serial Clock Line input / output.
I2C0_SDA	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	I2C0 Serial Data input / output.
I2C1_SCL	0: PA7 1: PA8 2: PA9 3: PI2	4: PI3 5: PB6 6: PB7 7: PB8	8: PB9 9: PB10 10: PJ14 11: PJ15	12: PC0 13: PC1 14: PC2 15: PC3	16: PC4 17: PC5 18: PC10 19: PC11	20: PF8 21: PF9 22: PF10 23: PF11	24: PF12 25: PF13 26: PF14 27: PF15	28: PK0 29: PK1 30: PK2 31: PA6	I2C1 Serial Clock Line input / output.
I2C1_SDA	0: PA6 1: PA7 2: PA8 3: PA9	4: PI2 5: PI3 6: PB6 7: PB7	8: PB8 9: PB9 10: PB10 11: PJ14	12: PJ15 13: PC0 14: PC1 15: PC2	16: PC3 17: PC4 18: PC5 19: PC10	20: PC11 21: PF8 22: PF9 23: PF10	24: PF11 25: PF12 26: PF13 27: PF14	28: PF15 29: PK0 30: PK1 31: PK2	I2C1 Serial Data input / output.
IDAC0_OUT	0: PK0								IDAC0 output.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
LES_CH5	0: PD13								LESENSE channel 5.
LES_CH6	0: PD14								LESENSE channel 6.
LES_CH7	0: PD15								LESENSE channel 7.
LES_CH8	0: PA0								LESENSE channel 8.
LES_CH9	0: PA1								LESENSE channel 9.
LES_CH10	0: PA2								LESENSE channel 10.
LES_CH11	0: PA3								LESENSE channel 11.
LES_CH12	0: PA4								LESENSE channel 12.
LES_CH13	0: PA5								LESENSE channel 13.
LES_CH14	0: PA6								LESENSE channel 14.
LES_CH15	0: PA7								LESENSE channel 15.
LETIM0_OUT0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Low Energy Timer LETIM0, output channel 1.

Table 6.9. CSEN Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
CEXT																																	
APORT1X	BUSAX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10		PC8		PC6		PC4		PC2		PC0
APORT1Y	BUSAY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT3X	BUSCX		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PA0		PD14		PD12		PD10		PD8
APORT3Y	BUSCY	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	
CEXT_SENSE																																	
APORT2X	BUSBX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT2Y	BUSBY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10		PC8		PC6		PC4		PC2		PC0
APORT4X	BUSDX	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PA0		PD14		PD12		PD10		PD8

Table 6.10. IDAC0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSCX		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PA0		PD14		PD12		PD10		PD8
APORT1Y	BUSCY	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	

7.2 BGA125 PCB Land Pattern

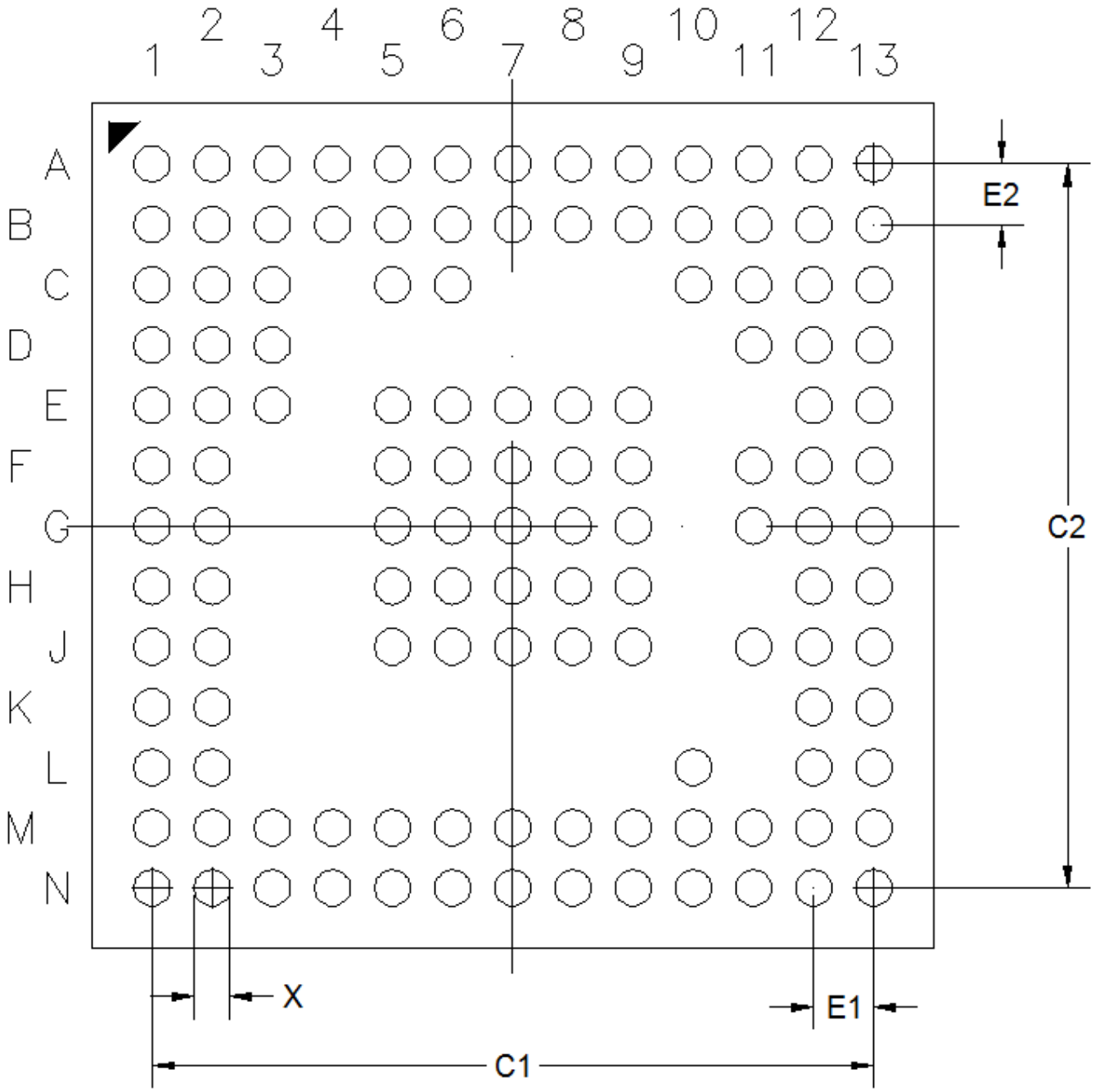

Figure 7.2. BGA125 PCB Land Pattern Drawing

Table 8.2. QFN48 PCB Land Pattern Dimensions

Dimension	Typ
S1	6.01
S	6.01
L1	4.70
W1	4.70
e	0.50
W	0.26
L	0.86

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 4x4 array of 0.75 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.