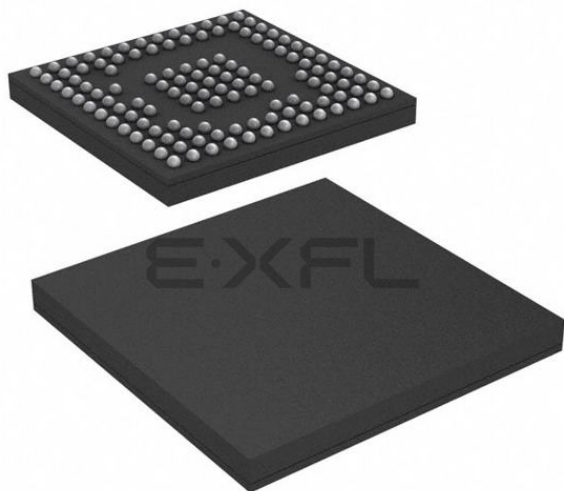




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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	65
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D - 12b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	125-VFBGA
Supplier Device Package	125-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32pg12b500f1024gl125-br

1. Feature List

The EFM32PG12 highlighted features are listed below.

- **ARM Cortex-M4 CPU platform**
 - High performance 32-bit processor @ up to 40 MHz
 - DSP instruction support and Floating Point Unit
 - Memory Protection Unit
 - Wake-up Interrupt Controller
- **Flexible Energy Management System**
 - 64 μ A/MHz in Active Mode (EM0)
 - 2.1 μ A EM2 Deep Sleep current (256 kB RAM retention and RTCC running from LFXO)
 - 1.5 μ A EM2 Deep Sleep current (16 kB RAM retention and RTCC running from LFRCO)
 - 1.81 μ A EM3 Stop current (State and 256 kB RAM retention, CRYOTIMER running from ULFRCO)
 - 0.39 μ A EM4H Hibernate Mode (128 byte RAM retention)
- **Up to 1024 kB flash program memory**
 - Dual-bank with read-while-write support
- **Up to 256 kB RAM data memory**
- **Up to 65 General Purpose I/O Pins**
 - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
 - Configurable peripheral I/O locations
 - Asynchronous external interrupts
 - Output state retention and wake-up from Shutoff Mode
- **Hardware Cryptography**
 - AES 128/256-bit keys
 - ECC B/K163, B/K233, P192, P224, P256
 - SHA-1 and SHA-2 (SHA-224 and SHA-256)
 - True random number generator (TRNG)
- **Security Management Unit (SMU)**
 - Fine-grained access control for on-chip peripherals
- **Timers/Counters**
 - 2 $\times$ 16-bit Timer/Counter
 - 3 + 4 Compare/Capture/PWM channels
 - 2 $\times$ 32-bit Timer/Counter
 - 3 + 4 Compare/Capture/PWM channels
 - 1 $\times$ 32-bit Real Time Counter and Calendar
 - 1 $\times$ 32-bit Ultra Low Energy CRYOTIMER for periodic wake-up from any Energy Mode
 - 16-bit Low Energy Timer for waveform generation
 - 3 $\times$ 16-bit Pulse Counter with asynchronous operation
 - 2 $\times$ Watchdog Timer with dedicated RC oscillator
- **8 Channel DMA Controller**
- **12 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Communication Interfaces**
 - 4 $\times$ Universal Synchronous/Asynchronous Receiver/ Transmitter
 - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
 - Triple buffered full/half-duplex operation with flow control
 - Low Energy UART
 - Autonomous operation with DMA in Deep Sleep Mode
 - 2 $\times$ I²C Interface with SMBus support
 - Address recognition in EM3 Stop Mode
- **Ultra Low-Power Precision Analog Peripherals**
 - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
 - 2 $\times$ Analog Comparator (ACMP)
 - 2 $\times$ 12-bit 500 ksps Digital to Analog Converter (VDAC)
 - 3 $\times$ Operational Amplifier (OPAMP)
 - Digital to Analog Current Converter (IDAC)
 - Multi-channel Capacitive Sense Interface (CSEN)
 - Up to 54 pins connected to analog channels (APORT) shared between analog peripherals
- **Low-Energy Sensor Interface (LESENSE)**
 - Autonomous sensor monitoring in deep sleep mode
 - Wide range of supported sensors, including LC sensors and capacitive touch switches
 - Up to 16 channels
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **Debug Interface**
 - 2-pin Serial Wire Debug interface
 - 1-pin Serial Wire Viewer
 - JTAG (programming only)
 - Embedded Trace Macrocell (ETM)
- **Wide Operating Range**
 - 1.8 V to 3.8 V single power supply
 - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
 - Standard (-40 °C to 85 °C T_{AMB}) and Extended (-40 °C to 125 °C T_J) temperature grades available
- **Packages**
 - 7 mm $\times$ 7 mm QFN48
 - 7 mm $\times$ 7 mm BGA125
- **Pre-Programmed UART Bootloader**
- **Full Software Support**
 - CMSIS register definitions
 - Low-power Hardware Abstraction Layer (HAL)
 - Portable software components
 - Third-party middleware
 - Free and available example code

3. System Overview

3.1 Introduction

The EFM32PG12 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the EFM32PG12 Reference Manual.

A block diagram of the EFM32PG12 family is shown in [Figure 3.1 Detailed EFM32PG12 Block Diagram on page 3](#). The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult [Ordering Information](#).

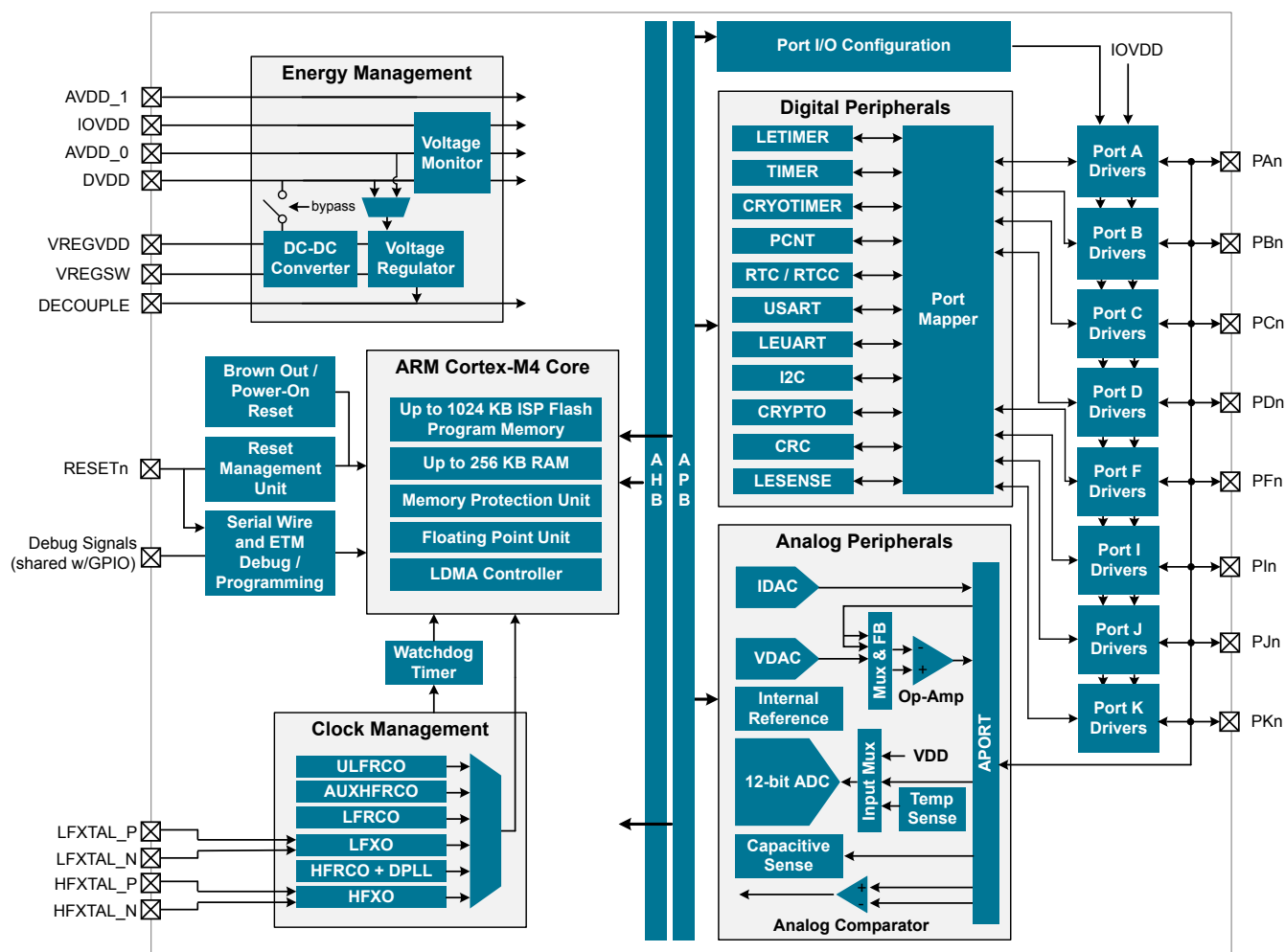


Figure 3.1. Detailed EFM32PG12 Block Diagram

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in LP mode ³ .	I _{ACTIVE_LPM_VS}	19 MHz HFRCO, CPU running while loop from flash	—	58	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	196	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode ² .	I _{EM1_DCM}	38.4 MHz crystal ⁴	—	56	—	μA/MHz
		38 MHz HFRCO	—	41	—	μA/MHz
		26 MHz HFRCO	—	48	—	μA/MHz
		1 MHz HFRCO	—	610	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Power mode ³ .	I _{EM1_LPM}	38.4 MHz crystal ⁴	—	49	—	μA/MHz
		38 MHz HFRCO	—	33	—	μA/MHz
		26 MHz HFRCO	—	35	—	μA/MHz
		1 MHz HFRCO	—	193	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode ² .	I _{EM1_DCM_VS}	19 MHz HFRCO	—	52	—	μA/MHz
		1 MHz HFRCO	—	587	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled. DCDC in LP mode ³ .	I _{EM1_LPM_VS}	19 MHz HFRCO	—	32	—	μA/MHz
		1 MHz HFRCO	—	170	—	μA/MHz
Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode. ³	I _{EM2_VS}	Full 256 kB RAM retention and RTCC running from LFXO	—	2.1	—	μA
		Full 256 kB RAM retention and RTCC running from LFRCO	—	2.2	—	μA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO ⁵	—	1.5	—	μA
Current consumption in EM3 mode, with voltage scaling enabled.	I _{EM3_VS}	Full 256 kB RAM retention and CRYOTIMER running from ULFRCO	—	1.81	—	μA
Current consumption in EM4H mode, with voltage scaling enabled.	I _{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.69	—	μA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.39	—	μA
		128 byte RAM retention, no RTCC	—	0.39	—	μA
Current consumption in EM4S mode	I _{EM4S}	No RAM retention, no RTCC	—	0.06	—	μA

Note:

1. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
2. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
3. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIMSEL=1, ANASW=DVDD.
4. CMU_HFXOCTRL_LOWPOWER=1.
5. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.8.2 High-Frequency Crystal Oscillator (HFXO)

Table 4.11. High-Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXO}		38	38.4	40	MHz
Supported crystal equivalent series resistance (ESR)	$\text{ESR}_{\text{HFXO}_38\text{M4}}$	Crystal frequency 38.4 MHz	—	—	60	Ω
Supported range of crystal load capacitance ¹	$C_{\text{HFXO_CL}}$		6	—	12	pF
On-chip tuning cap range ²	$C_{\text{HFXO_T}}$	On each of HFXTAL_N and HFXTAL_P pins	TBD	20	TBD	pF
On-chip tuning capacitance step	SS_{HFXO}		—	0.04	—	pF
Startup time	t_{HFXO}	38.4 MHz, ESR = 50 Ohm, C_L = 10 pF	—	300	—	μs
Frequency tolerance for the crystal	FT_{HFXO}	38.4 MHz, ESR = 50 Ohm, C_L = 10 pF	-40	—	40	ppm

Note:

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be $C_{\text{HFXO_T}}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal. .

4.1.8.3 Low-Frequency RC Oscillator (LFRCO)

Table 4.12. Low-Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}	$\text{ENVREF}^2 = 1$	TBD	32.768	TBD	kHz
		$\text{ENVREF}^2 = 1, T_{\text{AMB}} > 85^\circ\text{C}$	TBD	32.768	TBD	kHz
		$\text{ENVREF}^2 = 0$	TBD	32.768	TBD	kHz
		$\text{ENVREF}^2 = 0, T_{\text{AMB}} > 85^\circ\text{C}$	TBD	32.768	TBD	kHz
Startup time	t_{LFRCO}		—	500	—	μs
Current consumption ¹	I_{LFRCO}	$\text{ENVREF} = 1$ in CMU_LFRCOCTRL	—	370	—	nA
		$\text{ENVREF} = 0$ in CMU_LFRCOCTRL	—	520	—	nA

Note:

1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
2. in CMU_LFRCOCTRL register.

4.1.8.4 High-Frequency RC Oscillator (HFRCO)

Table 4.13. High-Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	$f_{\text{HFRCO_ACC}}$	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
Start-up time	t_{HFRCO}	$f_{\text{HFRCO}} \geq 19 \text{ MHz}$	—	300	—	ns
		$4 < f_{\text{HFRCO}} < 19 \text{ MHz}$	—	1	—	μs
		$f_{\text{HFRCO}} \leq 4 \text{ MHz}$	—	2.5	—	μs
Maximum DPLL lock time ¹	$t_{\text{DPLL_LOCK}}$	$f_{\text{REF}} = 32.768 \text{ kHz}$, $f_{\text{HFRCO}} = 39.98 \text{ MHz}$, $N = 1219$, $M = 0$	—	183	—	μs
Current consumption on all supplies	I_{HFRCO}	$f_{\text{HFRCO}} = 38 \text{ MHz}$	—	244	TBD	μA
		$f_{\text{HFRCO}} = 32 \text{ MHz}$	—	204	TBD	μA
		$f_{\text{HFRCO}} = 26 \text{ MHz}$	—	173	TBD	μA
		$f_{\text{HFRCO}} = 19 \text{ MHz}$	—	143	TBD	μA
		$f_{\text{HFRCO}} = 16 \text{ MHz}$	—	123	TBD	μA
		$f_{\text{HFRCO}} = 13 \text{ MHz}$	—	110	TBD	μA
		$f_{\text{HFRCO}} = 7 \text{ MHz}$	—	85	TBD	μA
		$f_{\text{HFRCO}} = 4 \text{ MHz}$	—	32	TBD	μA
		$f_{\text{HFRCO}} = 2 \text{ MHz}$	—	31	TBD	μA
		$f_{\text{HFRCO}} = 1 \text{ MHz}$	—	30	TBD	μA
		$f_{\text{HFRCO}} = 40 \text{ MHz}$, DPLL enabled	—	385	TBD	μA
		$f_{\text{HFRCO}} = 32 \text{ MHz}$, DPLL enabled	—	310	—	μA
		$f_{\text{HFRCO}} = 16 \text{ MHz}$, DPLL enabled	—	203	—	μA
		$f_{\text{HFRCO}} = 4 \text{ MHz}$, DPLL enabled	—	95	—	μA
		$f_{\text{HFRCO}} = 1 \text{ MHz}$, DPLL enabled	—	79	—	μA
Coarse trim step size (% of period)	$SS_{\text{HFRCO_COARSE}}$		—	0.8	—	%
Fine trim step size (% of period)	$SS_{\text{HFRCO_FINE}}$		—	0.1	—	%
Period jitter	PJ_{HFRCO}		—	0.2	—	% RMS

Note:

1. Maximum DPLL lock time $\sim 6 \times (M+1) \times t_{\text{REF}}$, where t_{REF} is the reference clock period.

4.1.10 General-Purpose I/O (GPIO)

Table 4.17. General-Purpose I/O (GPIO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IL}	GPIO pins	—	—	$IOVDD \cdot 0.3$	V
Input high voltage	V_{IH}	GPIO pins	$IOVDD \cdot 0.7$	—	—	V
Output high voltage relative to IOVDD	V_{OH}	Sourcing 3 mA, $IOVDD \geq 3$ V, DRIVESTRENGTH ¹ = WEAK	$IOVDD \cdot 0.8$	—	—	V
		Sourcing 1.2 mA, $IOVDD \geq 1.62$ V, DRIVESTRENGTH ¹ = WEAK	$IOVDD \cdot 0.6$	—	—	V
		Sourcing 20 mA, $IOVDD \geq 3$ V, DRIVESTRENGTH ¹ = STRONG	$IOVDD \cdot 0.8$	—	—	V
		Sourcing 8 mA, $IOVDD \geq 1.62$ V, DRIVESTRENGTH ¹ = STRONG	$IOVDD \cdot 0.6$	—	—	V
Output low voltage relative to IOVDD	V_{OL}	Sinking 3 mA, $IOVDD \geq 3$ V, DRIVESTRENGTH ¹ = WEAK	—	—	$IOVDD \cdot 0.2$	V
		Sinking 1.2 mA, $IOVDD \geq 1.62$ V, DRIVESTRENGTH ¹ = WEAK	—	—	$IOVDD \cdot 0.4$	V
		Sinking 20 mA, $IOVDD \geq 3$ V, DRIVESTRENGTH ¹ = STRONG	—	—	$IOVDD \cdot 0.2$	V
		Sinking 8 mA, $IOVDD \geq 1.62$ V, DRIVESTRENGTH ¹ = STRONG	—	—	$IOVDD \cdot 0.4$	V
Input leakage current	I_{IOLEAK}	All GPIO except LFXO pins, GPIO $\leq IOVDD$, $T_{amb} \leq 85$ °C	—	0.1	TBD	nA
		LFXO Pins, GPIO $\leq IOVDD$, $T_{amb} \leq 85$ °C	—	0.1	TBD	nA
		All GPIO except LFXO pins, GPIO $\leq IOVDD$, $T_{AMB} > 85$ °C	—	—	TBD	nA
		LFXO Pins, GPIO $\leq IOVDD$, $T_{AMB} > 85$ °C	—	—	TBD	nA
Input leakage current on 5VTOL pads above IOVDD	$I_{5VTOLLEAK}$	$IOVDD < GPIO \leq IOVDD + 2$ V	—	3.3	15	μ A
I/O pin pull-up/pull-down resistor	R_{PUD}		TBD	43	TBD	k Ω
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		TBD	25	TBD	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD. 2. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$. 3. ± 100 mV differential drive. 4. In ACMPn_CTRL register. 5. In ACMPn_HYSTERESIS register. 6. In ACMPn_INPUTSEL register.						

4.1.21 USART SPI

SPI Master Timing

Table 4.30. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 3 2}	t_{SCLK}		$2 \cdot t_{H\overline{F}PERCLK}$	—	—	ns
CS to MOSI ^{1 3}	t_{CS_MO}		0	—	13.3	ns
SCLK to MOSI ^{1 3}	t_{SCLK_MO}		0	—	8	ns
MISO setup time ^{1 3}	t_{SU_MI}	IOVDD = 1.62 V	90	—	—	ns
		IOVDD = 3.0 V	40	—	—	ns
MISO hold time ^{1 3}	t_{H_MI}		10	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{H\overline{F}PERCLK}$ is one period of the selected H $\overline{F}$ PERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

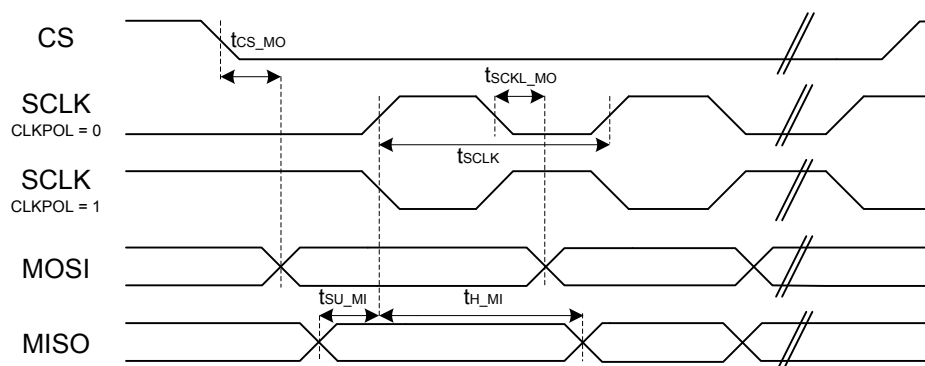


Figure 4.1. SPI Master Timing Diagram

SPI Slave Timing

Table 4.31. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 3 2}	t_{SCLK}		8 * t_{HFERCLK}	—	—	ns
SCLK high time ^{1 3 2}	$t_{\text{SCLK_HI}}$		3 * t_{HFERCLK}	—	—	ns
SCLK low time ^{1 3 2}	$t_{\text{SCLK_LO}}$		3 * t_{HFERCLK}	—	—	ns
CS active to MISO ^{1 3}	$t_{\text{CS_ACT_MI}}$		4	—	50	ns
CS disable to MISO ^{1 3}	$t_{\text{CS_DIS_MI}}$		4	—	50	ns
MOSI setup time ^{1 3}	$t_{\text{SU_MO}}$		4	—	—	ns
MOSI hold time ^{1 3 2}	$t_{\text{H_MO}}$		3 + 2 * t_{HFERCLK}	—	—	ns
SCLK to MISO ^{1 3 2}	$t_{\text{SCLK_MI}}$		16 + t_{HFERCLK}	—	66 + 2 * t_{HFERCLK}	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. t_{HFERCLK} is one period of the selected HFERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

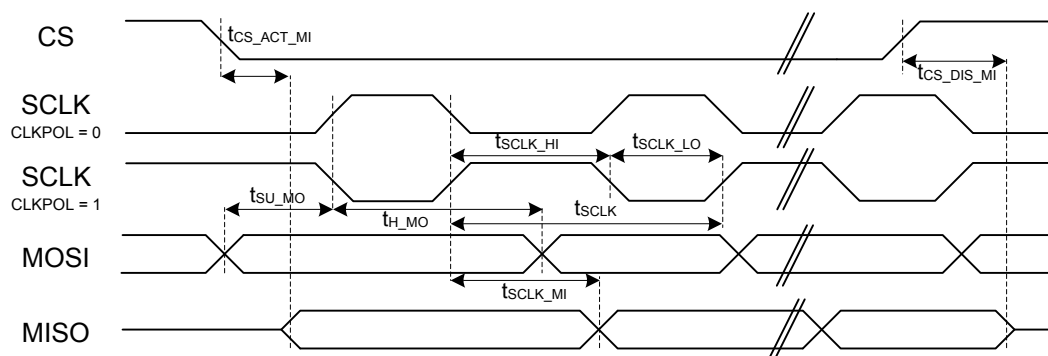


Figure 4.2. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

5. Typical Connection Diagrams

5.1 Power

Typical power supply connections for direct supply, without using the internal DC-DC converter, are shown in [Figure 5.1 EFM32PG12 Typical Application Circuit, Direct Supply, No DC-DC Converter on page 59](#).

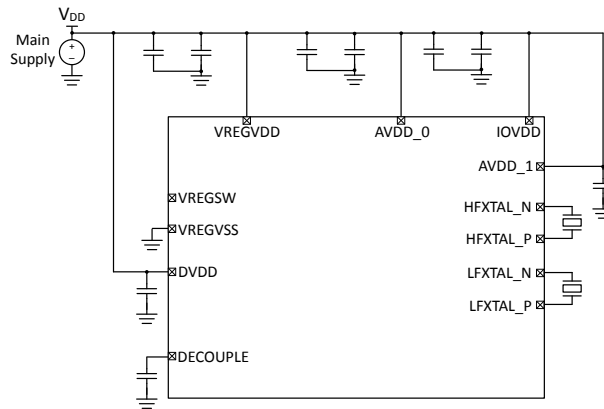


Figure 5.1. EFM32PG12 Typical Application Circuit, Direct Supply, No DC-DC Converter

A typical application circuit using the internal DC-DC converter is shown in [Figure 5.2 EFM32PG12 Typical Application Circuit Using the DC-DC Converter on page 59](#). The MCU operates from the DC-DC converter supply.

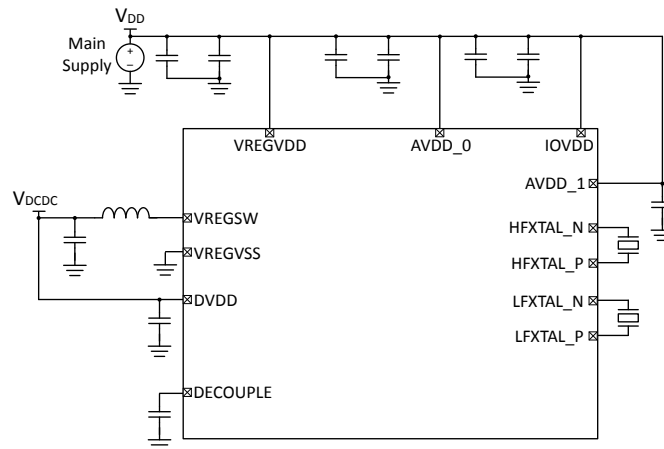


Figure 5.2. EFM32PG12 Typical Application Circuit Using the DC-DC Converter

5.2 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002: "Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
B8	PC8	BUSBY BUSAX	TIM0_CC0 #13 TIM0_CC1 #12 TIM0_CC2 #11 TIM0_CDTI0 #10 TIM0_CDTI1 #9 TIM0_CDTI2 #8 TIM1_CC0 #13 TIM1_CC1 #12 TIM1_CC2 #11 TIM1_CC3 #10 WTIM0_CC0 #28 WTIM0_CC1 #26 WTIM0_CC2 #24 WTIM0_CDTI0 #20 WTIM0_CDTI1 #18 WTIM0_CDTI2 #16 WTIM1_CC0 #12 WTIM1_CC1 #10 WTIM1_CC2 #8 WTIM1_CC3 #6 LE- TIM0_OUT0 #13 LE- TIM0_OUT1 #12 PCNT0_S0IN #13 PCNT0_S1IN #12	US0_TX #13 US0_RX #12 US0_CLK #11 US0_CS #10 US0_CTS #9 US0_RTS #8 US1_TX #13 US1_RX #12 US1_CLK #11 US1_CS #10 US1_CTS #9 US1_RTS #8 LEU0_TX #13 LEU0_RX #12 I2C0_SDA #13 I2C0_SCL #12	PRS_CH0 #10 PRS_CH9 #13 PRS_CH10 #2 PRS_CH11 #1 ACMP0_O #13 ACMP1_O #13 ETM_TD1 #3
B9	PC6	BUSBY BUSAX	TIM0_CC0 #11 TIM0_CC1 #10 TIM0_CC2 #9 TIM0_CDTI0 #8 TIM0_CDTI1 #7 TIM0_CDTI2 #6 TIM1_CC0 #11 TIM1_CC1 #10 TIM1_CC2 #9 TIM1_CC3 #8 WTIM0_CC0 #26 WTIM0_CC1 #24 WTIM0_CC2 #22 WTIM0_CDTI0 #18 WTIM0_CDTI1 #16 WTIM0_CDTI2 #14 WTIM1_CC0 #10 WTIM1_CC1 #8 WTIM1_CC2 #6 WTIM1_CC3 #4 LE- TIM0_OUT0 #11 LE- TIM0_OUT1 #10 PCNT0_S0IN #11 PCNT0_S1IN #10	US0_TX #11 US0_RX #10 US0_CLK #9 US0_CS #8 US0_CTS #7 US0_RTS #6 US1_TX #11 US1_RX #10 US1_CLK #9 US1_CS #8 US1_CTS #7 US1_RTS #6 LEU0_TX #11 LEU0_RX #10 I2C0_SDA #11 I2C0_SCL #10	CMU_CLK0 #2 CMU_CLKI0 #2 PRS_CH0 #8 PRS_CH9 #11 PRS_CH10 #0 PRS_CH11 #5 ACMP0_O #11 ACMP1_O #11 ETM_TCLK #3
B10	IOVDD	Digital IO power supply .			
B11	VREGVSS	Voltage regulator VSS			
B12	VREGVSS	Voltage regulator VSS			
B13	AVDD	Analog power supply .			

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
H12	PA9	BUSACMP0Y BU-SACMP0X	WTIM0_CC0 #9 WTIM0_CC1 #7 WTIM0_CC2 #5 WTIM0_CDTI0 #1 PCNT1_S0IN #3 PCNT1_S1IN #2 PCNT2_S0IN #3 PCNT2_S1IN #2	US2_TX #4 US2_RX #3 US2_CLK #2 US2_CS #1 US2_CTS #0 US2_RTS #31 I2C1_SDA #3 I2C1_SCL #2	LES_ALTEX1 ETM_TD3 #1
H13	PA8	BUSACMP0Y BU-SACMP0X	WTIM0_CC0 #8 WTIM0_CC1 #6 WTIM0_CC2 #4 WTIM0_CDTI0 #0 PCNT1_S0IN #2 PCNT1_S1IN #1 PCNT2_S0IN #2 PCNT2_S1IN #1	US2_TX #3 US2_RX #2 US2_CLK #1 US2_CS #0 US2_CTS #31 US2_RTS #30 I2C1_SDA #2 I2C1_SCL #1	LES_ALTEX0 ETM_TD2 #1
J1	AVDD	Analog power supply .			
J2	AVDD	Analog power supply .			
J5	VSS	Ground			
J6	VSS	Ground			
J7	VSS	Ground			
J8	VSS	Ground			
J9	VSS	Ground			
J11	PA7	BUSCY BUSDX	WTIM0_CC0 #7 WTIM0_CC1 #5 WTIM0_CC2 #3 PCNT1_S0IN #1 PCNT1_S1IN #0 PCNT2_S0IN #1 PCNT2_S1IN #0	US2_TX #2 US2_RX #1 US2_CLK #0 US2_CS #31 US2_CTS #30 US2_RTS #29 I2C1_SDA #1 I2C1_SCL #0	LES_CH15 ETM_TD1 #1
J12	PA6	BUSDY BUSCX	WTIM0_CC0 #6 WTIM0_CC1 #4 WTIM0_CC2 #2 PCNT1_S0IN #0 PCNT1_S1IN #31 PCNT2_S0IN #0 PCNT2_S1IN #31	US2_TX #1 US2_RX #0 US2_CLK #31 US2_CS #30 US2_CTS #29 US2_RTS #28 I2C1_SDA #0 I2C1_SCL #31	LES_CH14 ETM_TD0 #1

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
M9	PD9	BUSCY BUSDX	TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 WTIM0_CC1 #31 WTIM0_CC2 #29 WTIM0_CDTI0 #25 WTIM0_CDTI1 #23 WTIM0_CDTI2 #21 WTIM1_CC0 #17 WTIM1_CC1 #15 WTIM1_CC2 #13 WTIM1_CC3 #11 LE- TIM0_OUT0 #17 LE- TIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16	US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 US3_TX #1 US3_RX #0 US3_CLK #31 US3_CS #30 US3_CTS #29 US3_RTS #28 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16	CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17 LES_CH1
M10	PD11	BUSCY BUSDX	TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 WTIM0_CC2 #31 WTIM0_CDTI0 #27 WTIM0_CDTI1 #25 WTIM0_CDTI2 #23 WTIM1_CC0 #19 WTIM1_CC1 #17 WTIM1_CC2 #15 WTIM1_CC3 #13 LE- TIM0_OUT0 #19 LE- TIM0_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18	US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 US3_TX #3 US3_RX #2 US3_CLK #1 US3_CS #0 US3_CTS #31 US3_RTS #30 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18	PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19 LES_CH3

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
23	PD14	BUSDY BUSCX VDAC0_OUT1 / OPA1_OUT	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 WTIM0_CDTI0 #30 WTIM0_CDTI1 #28 WTIM0_CDTI2 #26 WTIM1_CC0 #22 WTIM1_CC1 #20 WTIM1_CC2 #18 WTIM1_CC3 #16 LE- TIM0_OUT0 #22 LE- TIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 US3_TX #6 US3_RX #5 US3_CLK #4 US3_CS #3 US3_CTS #2 US3_RTS #1 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 LES_CH6 GPIO_EM4WU4
24	PD15	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSCY BUSDX OPA1_N	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 WTIM0_CDTI0 #31 WTIM0_CDTI1 #29 WTIM0_CDTI2 #27 WTIM1_CC0 #23 WTIM1_CC1 #21 WTIM1_CC2 #19 WTIM1_CC3 #17 LE- TIM0_OUT0 #23 LE- TIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 US3_TX #7 US3_RX #6 US3_CLK #5 US3_CS #4 US3_CTS #3 US3_RTS #2 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 LES_CH7 DBG_SWO #2
25	PA0	BUSDY BUSCX ADC0_EXTN	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 WTIM0_CC0 #0 LE- TIM0_OUT0 #0 LE- TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0 LES_CH8

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
32	PB12	BUSDY BUSCX OPA2_OUT	TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 WTIM0_CC0 #16 WTIM0_CC1 #14 WTIM0_CC2 #12 WTIM0_CDTI0 #8 WTIM0_CDTI1 #6 WTIM0_CDTI2 #4 WTIM1_CC0 #0 LE- TIM0_OUT0 #7 LE- TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6	US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6	PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7
33	PB13	BUSCY BUSDX OPA2_N	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 WTIM0_CC0 #17 WTIM0_CC1 #15 WTIM0_CC2 #13 WTIM0_CDTI0 #9 WTIM0_CDTI1 #7 WTIM0_CDTI2 #5 WTIM1_CC0 #1 LE- TIM0_OUT0 #8 LE- TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	CMU_CLKI0 #0 PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9
34	AVDD	Analog power supply .			

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
43	PC6	BUSBY BUSAX	TIM0_CC0 #11 TIM0_CC1 #10 TIM0_CC2 #9 TIM0_CDTI0 #8 TIM0_CDTI1 #7 TIM0_CDTI2 #6 TIM1_CC0 #11 TIM1_CC1 #10 TIM1_CC2 #9 TIM1_CC3 #8 WTIM0_CC0 #26 WTIM0_CC1 #24 WTIM0_CC2 #22 WTIM0_CDTI0 #18 WTIM0_CDTI1 #16 WTIM0_CDTI2 #14 WTIM1_CC0 #10 WTIM1_CC1 #8 WTIM1_CC2 #6 WTIM1_CC3 #4 LE- TIM0_OUT0 #11 LE- TIM0_OUT1 #10 PCNT0_S0IN #11 PCNT0_S1IN #10	US0_TX #11 US0_RX #10 US0_CLK #9 US0_CS #8 US0_CTS #7 US0_RTS #6 US1_TX #11 US1_RX #10 US1_CLK #9 US1_CS #8 US1_CTS #7 US1_RTS #6 LEU0_TX #11 LEU0_RX #10 I2C0_SDA #11 I2C0_SCL #10	CMU_CLK0 #2 CMU_CLKI0 #2 PRS_CH0 #8 PRS_CH9 #11 PRS_CH10 #0 PRS_CH11 #5 ACMP0_O #11 ACMP1_O #11 ETM_TCLK #3
44	PC7	BUSAY BUSBX	TIM0_CC0 #12 TIM0_CC1 #11 TIM0_CC2 #10 TIM0_CDTI0 #9 TIM0_CDTI1 #8 TIM0_CDTI2 #7 TIM1_CC0 #12 TIM1_CC1 #11 TIM1_CC2 #10 TIM1_CC3 #9 WTIM0_CC0 #27 WTIM0_CC1 #25 WTIM0_CC2 #23 WTIM0_CDTI0 #19 WTIM0_CDTI1 #17 WTIM0_CDTI2 #15 WTIM1_CC0 #11 WTIM1_CC1 #9 WTIM1_CC2 #7 WTIM1_CC3 #5 LE- TIM0_OUT0 #12 LE- TIM0_OUT1 #11 PCNT0_S0IN #12 PCNT0_S1IN #11	US0_TX #12 US0_RX #11 US0_CLK #10 US0_CS #9 US0_CTS #8 US0_RTS #7 US1_TX #12 US1_RX #11 US1_CLK #10 US1_CS #9 US1_CTS #8 US1_RTS #7 LEU0_TX #12 LEU0_RX #11 I2C0_SDA #12 I2C0_SCL #11	CMU_CLK1 #2 PRS_CH0 #9 PRS_CH9 #12 PRS_CH10 #1 PRS_CH11 #0 ACMP0_O #12 ACMP1_O #12 ETM_TD0

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
47	PC10	BUSBY BUSAX	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 WTIM0_CC0 #30 WTIM0_CC1 #28 WTIM0_CC2 #26 WTIM0_CDTI0 #22 WTIM0_CDTI1 #20 WTIM0_CDTI2 #18 WTIM1_CC0 #14 WTIM1_CC1 #12 WTIM1_CC2 #10 WTIM1_CC3 #8 LE- TIM0_OUT0 #15 LE- TIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14 PCNT2_S0IN #19 PCNT2_S1IN #18	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14 I2C1_SDA #19 I2C1_SCL #18	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 ETM_TD3 GPIO_EM4WU12
48	PC11	BUSAY BUSBX	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 WTIM0_CC0 #31 WTIM0_CC1 #29 WTIM0_CC2 #27 WTIM0_CDTI0 #23 WTIM0_CDTI1 #21 WTIM0_CDTI2 #19 WTIM1_CC0 #15 WTIM1_CC1 #13 WTIM1_CC2 #11 WTIM1_CC3 #9 LE- TIM0_OUT0 #16 LE- TIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15 PCNT2_S0IN #20 PCNT2_S1IN #19	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15 I2C1_SDA #20 I2C1_SCL #19	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
PCNT0_S0IN	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	0: PA6 1: PA7 2: PA8 3: PA9	4: PI2 5: PI3 6: PB6 7: PB7	8: PB8 9: PB9 10: PB10 11: PJ14	12: PJ15 13: PC0 14: PC1 15: PC2	16: PC3 17: PC4 18: PC5 19: PF6	20: PF7 21: PF8 22: PF9 23: PF10	24: PF11 25: PF12 26: PF13 27: PF14	28: PF15 29: PK0 30: PK1 31: PK2	Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	0: PA7 1: PA8 2: PA9 3: PI2	4: PI3 5: PB6 6: PB7 7: PB8	8: PB9 9: PB10 10: PJ14 11: PJ15	12: PC0 13: PC1 14: PC2 15: PC3	16: PC4 17: PC5 18: PF6 19: PF7	20: PF8 21: PF9 22: PF10 23: PF11	24: PF12 25: PF13 26: PF14 27: PF15	28: PK0 29: PK1 30: PK2 31: PA6	Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	0: PA6 1: PA7 2: PA8 3: PA9	4: PI2 5: PI3 6: PB6 7: PB7	8: PB8 9: PB9 10: PB10 11: PJ14	12: PJ15 13: PC0 14: PC1 15: PC2	16: PC3 17: PC4 18: PC5 19: PC10	20: PC11 21: PF8 22: PF9 23: PF10	24: PF11 25: PF12 26: PF13 27: PF14	28: PF15 29: PK0 30: PK1 31: PK2	Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	0: PA7 1: PA8 2: PA9 3: PI2	4: PI3 5: PB6 6: PB7 7: PB8	8: PB9 9: PB10 10: PJ14 11: PJ15	12: PC0 13: PC1 14: PC2 15: PC3	16: PC4 17: PC5 18: PC10 19: PC11	20: PF8 21: PF9 22: PF10 23: PF11	24: PF12 25: PF13 26: PF14 27: PF15	28: PK0 29: PK1 30: PK2 31: PA6	Pulse Counter PCNT2 input number 1.
PRS_CH0	0: PF0 1: PF1 2: PF2 3: PF3	4: PF4 5: PF5 6: PF6 7: PF7	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11					Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PF1 1: PF2 2: PF3 3: PF4	4: PF5 5: PF6 6: PF7 7: PF0							Peripheral Reflex System PRS, channel 1.
PRS_CH2	0: PF2 1: PF3 2: PF4 3: PF5	4: PF6 5: PF7 6: PF0 7: PF1							Peripheral Reflex System PRS, channel 2.
PRS_CH3	0: PF3 1: PF4 2: PF5 3: PF6	4: PF7 5: PF0 6: PF1 7: PF2	8: PD9 9: PD10 10: PD11 11: PD12	12: PD13 13: PD14 14: PD15					Peripheral Reflex System PRS, channel 3.
PRS_CH4	0: PD9 1: PD10 2: PD11 3: PD12	4: PD13 5: PD14 6: PD15							Peripheral Reflex System PRS, channel 4.
PRS_CH5	0: PD10 1: PD11 2: PD12 3: PD13	4: PD14 5: PD15 6: PD9							Peripheral Reflex System PRS, channel 5.
PRS_CH6	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PD9	12: PD10 13: PD11 14: PD12 15: PD13	16: PD14 17: PD15				Peripheral Reflex System PRS, channel 6.

Table 7.1. BGA125 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.87	0.94
A1	0.16	0.21	0.26
A2	0.61	0.66	0.71
c	0.17	0.21	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D1	---	6.00	---
E1	---	6.00	---
e	---	0.50	---
b	0.25	0.30	0.35
aaa	0.10		
bbb	0.10		
ddd	0.08		
eee	0.15		
fff	0.05		
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.			

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