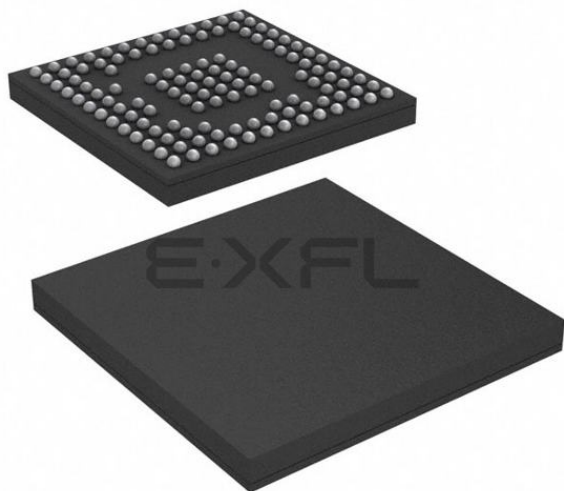




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	65
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D - 12b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	125-VFBGA
Supplier Device Package	125-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32pg12b500f1024gl125-cr

3.10.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.10.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Heavy Drive ² , $T_{amb} \leq 85\text{ }^{\circ}\text{C}$	—	—	TBD	mA
		Low noise (LN) mode, Heavy Drive ² , $T_{amb} > 85\text{ }^{\circ}\text{C}$	—	—	TBD	mA
		Low noise (LN) mode, Medium Drive ²	—	—	TBD	mA
		Low noise (LN) mode, Light Drive ²	—	—	TBD	mA
		Low power (LP) mode, $LPCMPBIASEM_{xx}^3 = 0$	—	—	TBD	μA
		Low power (LP) mode, $LPCMPBIASEM_{xx}^3 = 3$	—	—	TBD	mA
DCDC nominal output capacitor ⁵	C_{DCDC}	25% tolerance	1	4.7	4.7	μF
DCDC nominal output inductor	L_{DCDC}	20% tolerance	4.7	4.7	4.7	μH
Resistance in Bypass mode	R_{BYP}		—	1.2	TBD	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$.
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. In EMU_DCDCMISCCTRL register.
4. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 μF . Different control loop settings must be used if C_{DCDC} is lower than 4.7 μF .

4.1.5 Current Consumption

4.1.5.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T_{OP} = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C.

Table 4.5. Current Consumption 3.3 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I _{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash ¹	—	126	—	μA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	99	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	99	TBD	μA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	124	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	102	TBD	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	280	TBD	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I _{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	88	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	234	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled	I _{EM1}	38.4 MHz crystal ¹	—	76	—	μA/MHz
		38 MHz HFRCO	—	50	TBD	μA/MHz
		26 MHz HFRCO	—	52	TBD	μA/MHz
		1 MHz HFRCO	—	230	TBD	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I _{EM1_VS}	19 MHz HFRCO	—	47	—	μA/MHz
		1 MHz HFRCO	—	193	—	μA/MHz
Current consumption in EM2 mode, with voltage scaling enabled.	I _{EM2_VS}	Full 256 kB RAM retention and RTCC running from LFXO	—	2.9	—	μA
		Full 256 kB RAM retention and RTCC running from LFRCO	—	3.2	—	μA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO ²	—	2.1	TBD	μA
Current consumption in EM3 mode, with voltage scaling enabled.	I _{EM3_VS}	Full 256 kB RAM retention and CRYOTIMER running from ULFR-CO	—	2.56	TBD	μA
Current consumption in EM4H mode, with voltage scaling enabled.	I _{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	1.0	—	μA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.45	—	μA
		128 byte RAM retention, no RTCC	—	0.43	TBD	μA

4.1.8 Oscillators

4.1.8.1 Low-Frequency Crystal Oscillator (LFXO)

Table 4.10. Low-Frequency Crystal Oscillator (LFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	—	70	k Ω
Supported range of crystal load capacitance ¹	$C_{\text{LFXO_CL}}$		6	—	18	pF
On-chip tuning cap range ²	$C_{\text{LFXO_T}}$	On each of LFX TAL_N and LFX TAL_P pins	8	—	40	pF
On-chip tuning cap step size	SS_{LFXO}		—	0.25	—	pF
Current consumption after startup ³	I_{LFXO}	ESR = 70 k Ω , C_L = 7 pF, GAIN ⁴ = 2, AGC ⁴ = 1	—	273	—	nA
Start- up time	t_{LFXO}	ESR = 70 k Ω , C_L = 7 pF, GAIN ⁴ = 2	—	308	—	ms

Note:

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be $C_{\text{LFXO_T}}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal. .
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
4. In CMU_LFXOCTRL register.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Settling time, (output settled within 1% of steady state value),	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	μs
		Step value is changed	—	1	—	μs
Current consumption ²	I_{IDAC}	EM0 or EM1 Source mode, excluding output current	—	8.9	TBD	μA
		EM0 or EM1 Sink mode, excluding output current	—	12	TBD	μA
		EM2 or EM3 Source mode, excluding output current, $T = 25^{\circ}C$	—	1.04	—	μA
		EM2 or EM3 Sink mode, excluding output current, $T = 25^{\circ}C$	—	1.08	—	μA
		EM2 or EM3 Source mode, excluding output current, $T \geq 85^{\circ}C$	—	8.9	—	μA
		EM2 or EM3 Sink mode, excluding output current, $T \geq 85^{\circ}C$	—	12	—	μA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$	—	0.11	—	%
		RANGESEL1=1, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$	—	0.06	—	%
		RANGESEL1=2, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 150 \text{ mV})$	—	0.04	—	%
		RANGESEL1=3, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 250 \text{ mV})$	—	0.03	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.12	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.05	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.04	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.03	—	%

Note:

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.16 Capacitive Sense (CSEN)

Table 4.23. Capacitive Sense (CSEN)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single conversion time (1x accumulation)	t_{CNV}	12-bit SAR Conversions	—	20.2	—	μs
		16-bit SAR Conversions	—	26.4	—	μs
		Delta Modulation Conversion (single comparison)	—	1.55	—	μs
Maximum external capacitive load	C_{EXTMAX}	CS0CG=7 (Gain = 1x), including routing parasitics	—	68	—	pF
		CS0CG=0 (Gain = 10x), including routing parasitics	—	680	—	pF
Maximum external series impedance	R_{EXTMAX}		—	1	—	k Ω
Supply current, EM2 scan conversions, WARMUP-MODE=NORMAL, WARMUPCNT=0	I_{CSEN_EM2}	12-bit SAR conversions, 20 ms scan rate, 8 samples per scan ¹	—	800	—	nA
		Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), 8 samples per scan ¹	—	590	—	nA
		12-bit SAR conversions, 200 ms scan rate, 8 samples per scan ¹	—	80	—	nA
		Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), 8 samples per scan ¹	—	59	—	nA
Supply current, continuous conversions, WARMUP-MODE=KEEPCSENWARM	I_{CSEN_ACTIVE}	SAR or Delta Modulation conversions of 33 pF capacitor, always on	—	90.5	—	μA

Note:

- Current is specified with a total external capacitance of 33 pF. Average current is dependent on how long the module is actively sampling channels within the scan period, and will scale linearly with the number of samples acquired. Supply current for a specific application can be calculated by multiplying the current per sample by the total number of samples per period ($total_current = single_sample_current * (number_of_channels * accumulation)$).

4.1.20 I2C

4.1.20.1 I2C Standard-mode (Sm)¹

Table 4.27. I2C Standard-mode (Sm)¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ²	f _{SCL}		0	—	100	kHz
SCL clock low time	t _{LOW}		4.7	—	—	μs
SCL clock high time	t _{HIGH}		4	—	—	μs
SDA set-up time	t _{SU_DAT}		250	—	—	ns
SDA hold time ³	t _{HD_DAT}		100	—	3450	ns
Repeated START condition set-up time	t _{SU_STA}		4.7	—	—	μs
(Repeated) START condition hold time	t _{HD_STA}		4	—	—	μs
STOP condition set-up time	t _{SU_STO}		4	—	—	μs
Bus free time between a STOP and START condition	t _{BUF}		4.7	—	—	μs

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD_DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.20.3 I2C Fast-mode Plus (Fm+)¹

Table 4.29. I2C Fast-mode Plus (Fm+)¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ²	f _{SCL}		0	—	1000	kHz
SCL clock low time	t _{LOW}		0.5	—	—	μs
SCL clock high time	t _{HIGH}		0.26	—	—	μs
SDA set-up time	t _{SU_DAT}		50	—	—	ns
SDA hold time	t _{HD_DAT}		100	—	—	ns
Repeated START condition set-up time	t _{SU_STA}		0.26	—	—	μs
(Repeated) START condition hold time	t _{HD_STA}		0.26	—	—	μs
STOP condition set-up time	t _{SU_STO}		0.26	—	—	μs
Bus free time between a STOP and START condition	t _{BUF}		0.5	—	—	μs

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HPPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

5. Typical Connection Diagrams

5.1 Power

Typical power supply connections for direct supply, without using the internal DC-DC converter, are shown in [Figure 5.1 EFM32PG12 Typical Application Circuit, Direct Supply, No DC-DC Converter on page 59](#).

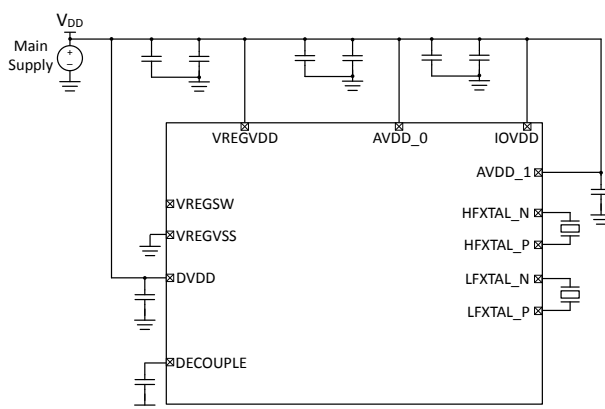


Figure 5.1. EFM32PG12 Typical Application Circuit, Direct Supply, No DC-DC Converter

A typical application circuit using the internal DC-DC converter is shown in [Figure 5.2 EFM32PG12 Typical Application Circuit Using the DC-DC Converter on page 59](#). The MCU operates from the DC-DC converter supply.

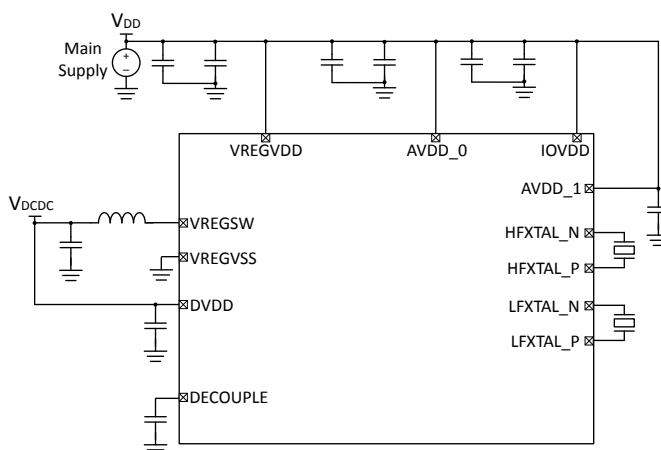


Figure 5.2. EFM32PG12 Typical Application Circuit Using the DC-DC Converter

5.2 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002: "Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

Table 6.1. EFM32PG12B5xx in BGA125 Device Pinout

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
A1	PF3	BUSAY BUSBX	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 WTIM0_CDTI2 #31 WTIM1_CC0 #27 WTIM1_CC1 #25 WTIM1_CC2 #23 WTIM1_CC3 #21 LE- TIM0_OUT0 #27 LE- TIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 US2_TX #16 US2_RX #15 US2_CLK #14 US2_CS #13 US2_CTS #12 US2_RTS #11 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI
A2	PF1	BUSAY BUSBX	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 WTIM0_CDTI1 #31 WTIM0_CDTI2 #29 WTIM1_CC0 #25 WTIM1_CC1 #23 WTIM1_CC2 #21 WTIM1_CC3 #19 LE- TIM0_OUT0 #25 LE- TIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 US2_TX #15 US2_RX #14 US2_CLK #13 US2_CS #12 US2_CTS #11 US2_RTS #10 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS BOOT_RX
A3	PC5	BUSAY BUSBX	WTIM0_CC0 #25 WTIM0_CC1 #23 WTIM0_CC2 #21 WTIM0_CDTI0 #17 WTIM0_CDTI1 #15 WTIM0_CDTI2 #13 WTIM1_CC0 #9 WTIM1_CC1 #7 WTIM1_CC2 #5 WTIM1_CC3 #3 PCNT1_S0IN #18 PCNT1_S1IN #17 PCNT2_S0IN #18 PCNT2_S1IN #17	US3_TX #23 US3_RX #22 US3_CLK #21 US3_CS #20 US3_CTS #19 US3_RTS #18 I2C1_SDA #18 I2C1_SCL #17	

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
A4	PC3	BUSAY BUSBX	WTIM0_CC0 #23 WTIM0_CC1 #21 WTIM0_CC2 #19 WTIM0_CDTI0 #15 WTIM0_CDTI1 #13 WTIM0_CDTI2 #11 WTIM1_CC0 #7 WTIM1_CC1 #5 WTIM1_CC2 #3 WTIM1_CC3 #1 PCNT1_S0IN #16 PCNT1_S1IN #15 PCNT2_S0IN #16 PCNT2_S1IN #15	US3_TX #21 US3_RX #20 US3_CLK #19 US3_CS #18 US3_CTS #17 US3_RTS #16 I2C1_SDA #16 I2C1_SCL #15	
A5	PC0	BUSBY BUSAX	WTIM0_CC0 #20 WTIM0_CC1 #18 WTIM0_CC2 #16 WTIM0_CDTI0 #12 WTIM0_CDTI1 #10 WTIM0_CDTI2 #8 WTIM1_CC0 #4 WTIM1_CC1 #2 WTIM1_CC2 #0 PCNT1_S0IN #13 PCNT1_S1IN #12 PCNT2_S0IN #13 PCNT2_S1IN #12	US3_TX #18 US3_RX #17 US3_CLK #16 US3_CS #15 US3_CTS #14 US3_RTS #13 I2C1_SDA #13 I2C1_SCL #12	
A6	PC11	BUSAY BUSBX	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 WTIM0_CC0 #31 WTIM0_CC1 #29 WTIM0_CC2 #27 WTIM0_CDTI0 #23 WTIM0_CDTI1 #21 WTIM0_CDTI2 #19 WTIM1_CC0 #15 WTIM1_CC1 #13 WTIM1_CC2 #11 WTIM1_CC3 #9 LE- TIM0_OUT0 #16 LE- TIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15 PCNT2_S0IN #20 PCNT2_S1IN #19	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15 I2C1_SDA #20 I2C1_SCL #19	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
D13	PB9	OPA2_OUTALT #0 BUSCY BUSDX	WTIM0_CC0 #13 WTIM0_CC1 #11 WTIM0_CC2 #9 WTIM0_CDTI0 #5 WTIM0_CDTI1 #3 WTIM0_CDTI2 #1 PCNT1_S0IN #9 PCNT1_S1IN #8 PCNT2_S0IN #9 PCNT2_S1IN #8	US2_TX #12 US2_RX #11 US2_CLK #10 US2_CS #9 US2_CTS #8 US2_RTS #7 US3_TX #13 US3_RX #12 US3_CLK #11 US3_CS #10 US3_CTS #9 US3_RTS #8 I2C1_SDA #9 I2C1_SCL #8	
E1	PK1		PCNT1_S0IN #30 PCNT1_S1IN #29 PCNT2_S0IN #30 PCNT2_S1IN #29	US2_TX #30 US2_RX #29 US2_CLK #28 US2_CS #27 US2_CTS #26 US2_RTS #25 US3_TX #30 US3_RX #29 US3_CLK #28 US3_CS #27 US3_CTS #26 US3_RTS #25 I2C1_SDA #30 I2C1_SCL #29	
E2	PK0	IDAC0_OUT	PCNT1_S0IN #29 PCNT1_S1IN #28 PCNT2_S0IN #29 PCNT2_S1IN #28	US2_TX #29 US2_RX #28 US2_CLK #27 US2_CS #26 US2_CTS #25 US2_RTS #24 US3_TX #29 US3_RX #28 US3_CLK #27 US3_CS #26 US3_CTS #25 US3_RTS #24 I2C1_SDA #29 I2C1_SCL #28	
E3	PF15	BUSAY BUSBX	PCNT1_S0IN #28 PCNT1_S1IN #27 PCNT2_S0IN #28 PCNT2_S1IN #27	US2_TX #28 US2_RX #27 US2_CLK #26 US2_CS #25 US2_CTS #24 US2_RTS #23 US3_TX #28 US3_RX #27 US3_CLK #26 US3_CS #25 US3_CTS #24 US3_RTS #23 I2C1_SDA #28 I2C1_SCL #27	
E5	VSS	Ground			
E6	VSS	Ground			
E7	VSS	Ground			
E8	VSS	Ground			
E9	VSS	Ground			
E12	PB8	BUSDY BUSCX	WTIM0_CC0 #12 WTIM0_CC1 #10 WTIM0_CC2 #8 WTIM0_CDTI0 #4 WTIM0_CDTI1 #2 WTIM0_CDTI2 #0 PCNT1_S0IN #8 PCNT1_S1IN #7 PCNT2_S0IN #8 PCNT2_S1IN #7	US2_TX #11 US2_RX #10 US2_CLK #9 US2_CS #8 US2_CTS #7 US2_RTS #6 US3_TX #12 US3_RX #11 US3_CLK #10 US3_CS #9 US3_CTS #8 US3_RTS #7 I2C1_SDA #8 I2C1_SCL #7	ETM_TD3 #2

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
M9	PD9	BUSCY BUSDX	TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 WTIM0_CC1 #31 WTIM0_CC2 #29 WTIM0_CDTI0 #25 WTIM0_CDTI1 #23 WTIM0_CDTI2 #21 WTIM1_CC0 #17 WTIM1_CC1 #15 WTIM1_CC2 #13 WTIM1_CC3 #11 LE- TIM0_OUT0 #17 LE- TIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16	US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 US3_TX #1 US3_RX #0 US3_CLK #31 US3_CS #30 US3_CTS #29 US3_RTS #28 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16	CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17 LES_CH1
M10	PD11	BUSCY BUSDX	TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 WTIM0_CC2 #31 WTIM0_CDTI0 #27 WTIM0_CDTI1 #25 WTIM0_CDTI2 #23 WTIM1_CC0 #19 WTIM1_CC1 #17 WTIM1_CC2 #15 WTIM1_CC3 #13 LE- TIM0_OUT0 #19 LE- TIM0_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18	US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 US3_TX #3 US3_RX #2 US3_CLK #1 US3_CS #0 US3_CTS #31 US3_RTS #30 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18	PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19 LES_CH3

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
23	PD14	BUSDY BUSCX VDAC0_OUT1 / OPA1_OUT	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 WTIM0_CDTI0 #30 WTIM0_CDTI1 #28 WTIM0_CDTI2 #26 WTIM1_CC0 #22 WTIM1_CC1 #20 WTIM1_CC2 #18 WTIM1_CC3 #16 LE- TIM0_OUT0 #22 LE- TIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 US3_TX #6 US3_RX #5 US3_CLK #4 US3_CS #3 US3_CTS #2 US3_RTS #1 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 LES_CH6 GPIO_EM4WU4
24	PD15	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSCY BUSDX OPA1_N	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 WTIM0_CDTI0 #31 WTIM0_CDTI1 #29 WTIM0_CDTI2 #27 WTIM1_CC0 #23 WTIM1_CC1 #21 WTIM1_CC2 #19 WTIM1_CC3 #17 LE- TIM0_OUT0 #23 LE- TIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 US3_TX #7 US3_RX #6 US3_CLK #5 US3_CS #4 US3_CTS #3 US3_RTS #2 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 LES_CH7 DBG_SWO #2
25	PA0	BUSDY BUSCX ADC0_EXTN	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 WTIM0_CC0 #0 LE- TIM0_OUT0 #0 LE- TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0 LES_CH8

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
32	PB12	BUSDY BUSCX OPA2_OUT	TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 WTIM0_CC0 #16 WTIM0_CC1 #14 WTIM0_CC2 #12 WTIM0_CDTI0 #8 WTIM0_CDTI1 #6 WTIM0_CDTI2 #4 WTIM1_CC0 #0 LE- TIM0_OUT0 #7 LE- TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6	US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6	PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7
33	PB13	BUSCY BUSDX OPA2_N	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 WTIM0_CC0 #17 WTIM0_CC1 #15 WTIM0_CC2 #13 WTIM0_CDTI0 #9 WTIM0_CDTI1 #7 WTIM0_CDTI2 #5 WTIM1_CC0 #1 LE- TIM0_OUT0 #8 LE- TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	CMU_CLKI0 #0 PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9
34	AVDD	Analog power supply .			

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US3_CLK	0: PD10 1: PD11 2: PD12 3: PD13	4: PD14 5: PD15 6: PI2 7: PI3	8: PB6 9: PB7 10: PB8 11: PB9	12: PB10 13: PB11 14: PJ14 15: PJ15	16: PC0 17: PC1 18: PC2 19: PC3	20: PC4 21: PC5 22: PF11 23: PF12	24: PF13 25: PF14 26: PF15 27: PK0	28: PK1 29: PK2 30: PD8 31: PD9	USART3 clock input / output.
US3_CS	0: PD11 1: PD12 2: PD13 3: PD14	4: PD15 5: PI2 6: PI3 7: PB6	8: PB7 9: PB8 10: PB9 11: PB10	12: PB11 13: PJ14 14: PJ15 15: PC0	16: PC1 17: PC2 18: PC3 19: PC4	20: PC5 21: PF11 22: PF12 23: PF13	24: PF14 25: PF15 26: PK0 27: PK1	28: PK2 29: PD8 30: PD9 31: PD10	USART3 chip select input / output.
US3_CTS	0: PD12 1: PD13 2: PD14 3: PD15	4: PI2 5: PI3 6: PB6 7: PB7	8: PB8 9: PB9 10: PB10 11: PB11	12: PJ14 13: PJ15 14: PC0 15: PC1	16: PC2 17: PC3 18: PC4 19: PC5	20: PF11 21: PF12 22: PF13 23: PF14	24: PF15 25: PK0 26: PK1 27: PK2	28: PD8 29: PD9 30: PD10 31: PD11	USART3 Clear To Send hardware flow control input.
US3_RTS	0: PD13 1: PD14 2: PD15 3: PI2	4: PI3 5: PB6 6: PB7 7: PB8	8: PB9 9: PB10 10: PB11 11: PJ14	12: PJ15 13: PC0 14: PC1 15: PC2	16: PC3 17: PC4 18: PC5 19: PF11	20: PF12 21: PF13 22: PF14 23: PF15	24: PK0 25: PK1 26: PK2 27: PD8	28: PD9 29: PD10 30: PD11 31: PD12	USART3 Request To Send hardware flow control output.
US3_RX	0: PD9 1: PD10 2: PD11 3: PD12	4: PD13 5: PD14 6: PD15 7: PI2	8: PI3 9: PB6 10: PB7 11: PB8	12: PB9 13: PB10 14: PB11 15: PJ14	16: PJ15 17: PC0 18: PC1 19: PC2	20: PC3 21: PC4 22: PC5 23: PF11	24: PF12 25: PF13 26: PF14 27: PF15	28: PK0 29: PK1 30: PK2 31: PD8	USART3 Asynchronous Receive. USART3 Synchronous mode Master Input / Slave Output (MISO).
US3_TX	0: PD8 1: PD9 2: PD10 3: PD11	4: PD12 5: PD13 6: PD14 7: PD15	8: PI2 9: PI3 10: PB6 11: PB7	12: PB8 13: PB9 14: PB10 15: PB11	16: PJ14 17: PJ15 18: PC0 19: PC1	20: PC2 21: PC3 22: PC4 23: PC5	24: PF11 25: PF12 26: PF13 27: PF14	28: PF15 29: PK0 30: PK1 31: PK2	USART3 Asynchronous Transmit. Also used as receive input in half duplex communication. USART3 Synchronous mode Master Output / Slave Input (MOSI).
VDAC0_EXT	0: PA1								Digital to analog converter VDAC0 external reference input pin.
VDAC0_OUT0 / OPA0_OUT	0: PA3								Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT0ALT / OPA0_OUT-ALT	0: PA5 1: PD13 2: PD15								Digital to Analog Converter DAC0 alternative output for channel 0.
VDAC0_OUT1 / OPA1_OUT	0: PD14								Digital to Analog Converter DAC0 output channel number 1.
VDAC0_OUT1ALT / OPA1_OUT-ALT	0: PD12 1: PA2 2: PA4								Digital to Analog Converter DAC0 alternative output for channel 1.

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA2_OUT																																	
APORT1Y	BUSAY	PB15	PF14	PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT2Y	BUSBY				PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10		PC8		PC6		PC4		PC2		PC0
APORT3Y	BUSCY	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PA0		PD14		PD12		PD10		PD8
OPA2_P																																	
APORT1X	BUSAX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10		PC8		PC6		PC4		PC2		PC0
APORT2X	BUSBX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT3X	BUSCX		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PA0		PD14		PD12		PD10		PD8
APORT4X	BUSDX	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	
VDAC0_OUT0 / OPA0_OUT																																	
APORT1Y	BUSAY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT2Y	BUSBY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10		PC8		PC6		PC4		PC2		PC0
APORT3Y	BUSCY	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PA0		PD14		PD12		PD10		PD8

8. QFN48 Package Specifications

8.1 QFN48 Package Dimensions

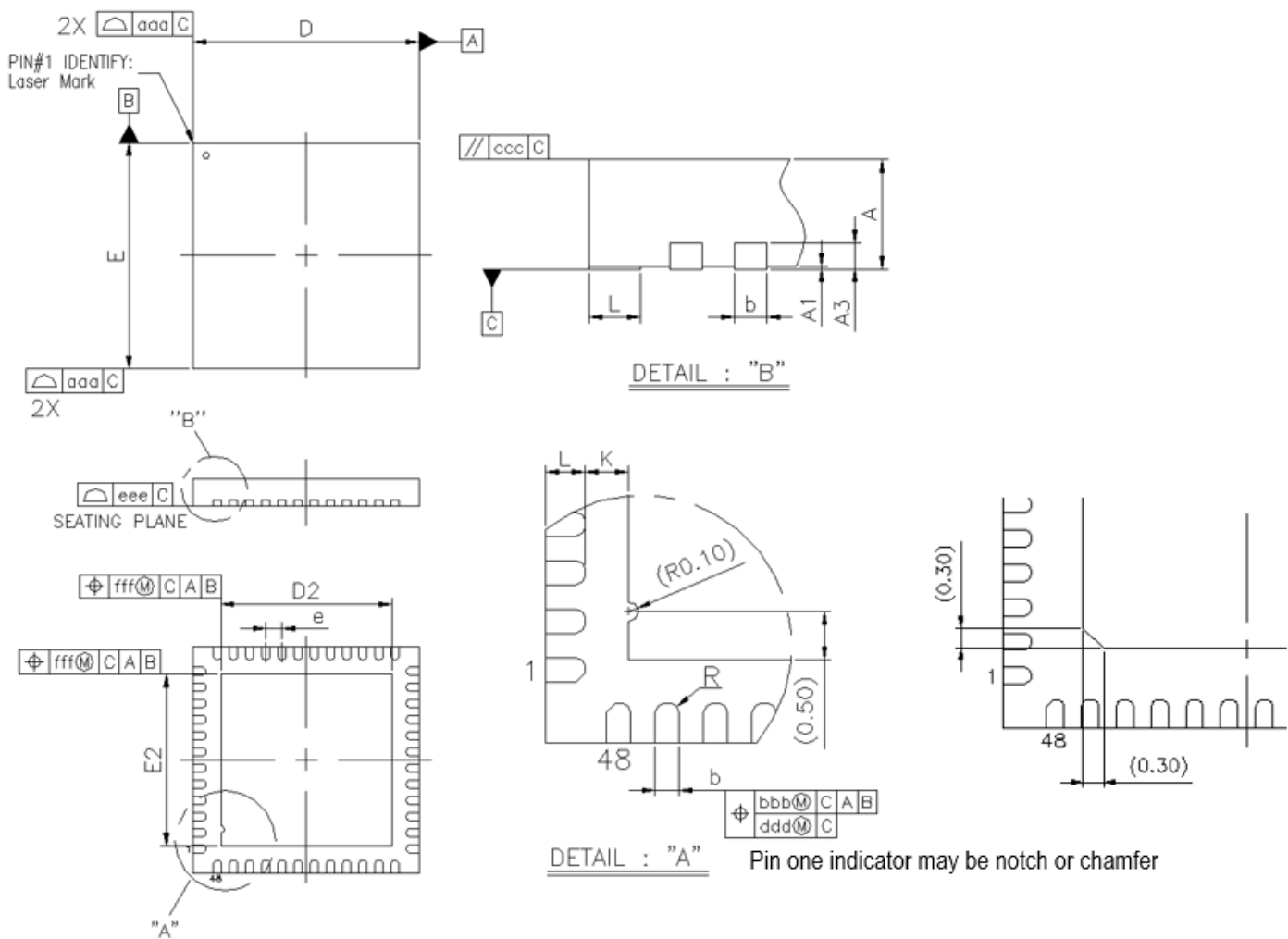


Figure 8.1. QFN48 Package Drawing

3.10.2	Memory System Controller (MSC)	9
3.10.3	Linked Direct Memory Access Controller (LDMA)	9
3.11	Memory Map	10
3.12	Configuration Summary	12
4.	Electrical Specifications	13
4.1	Electrical Characteristics	13
4.1.1	Absolute Maximum Ratings	13
4.1.2	Operating Conditions	14
4.1.2.1	General Operating Conditions	14
4.1.3	Thermal Characteristics	15
4.1.4	DC-DC Converter	16
4.1.5	Current Consumption	18
4.1.5.1	Current Consumption 3.3 V without DC-DC Converter	18
4.1.5.2	Current Consumption 3.3 V using DC-DC Converter	20
4.1.5.3	Current Consumption 1.8 V without DC-DC Converter	22
4.1.6	Wake Up Times	23
4.1.7	Brown Out Detector (BOD)	24
4.1.8	Oscillators	25
4.1.8.1	Low-Frequency Crystal Oscillator (LFXO)	25
4.1.8.2	High-Frequency Crystal Oscillator (HFXO)	26
4.1.8.3	Low-Frequency RC Oscillator (LFRCO)	26
4.1.8.4	High-Frequency RC Oscillator (HFRCO)	27
4.1.8.5	Auxiliary High-Frequency RC Oscillator (AUXHFRCO)	28
4.1.8.6	Ultra-low Frequency RC Oscillator (ULFRCO)	28
4.1.9	Flash Memory Characteristics	29
4.1.10	General-Purpose I/O (GPIO)	30
4.1.11	Voltage Monitor (VMON)	32
4.1.12	Analog to Digital Converter (ADC)	33
4.1.13	Analog Comparator (ACMP)	35
4.1.14	Digital to Analog Converter (VDAC)	38
4.1.15	Current Digital to Analog Converter (IDAC)	40
4.1.16	Capacitive Sense (CSEN)	42
4.1.17	Operational Amplifier (OPAMP)	43
4.1.18	Pulse Counter (PCNT)	46
4.1.19	Analog Port (APORT)	46
4.1.20	I2C	47
4.1.20.1	I2C Standard-mode (Sm)	47
4.1.20.2	I2C Fast-mode (Fm)	48
4.1.20.3	I2C Fast-mode Plus (Fm+)	49
4.1.21	USART SPI	50
4.2	Typical Performance Curves	51
4.2.1	Supply Current	52
4.2.2	DC-DC Converter	57
5.	Typical Connection Diagrams	59
5.1	Power	59
5.2	Other Connections	59

