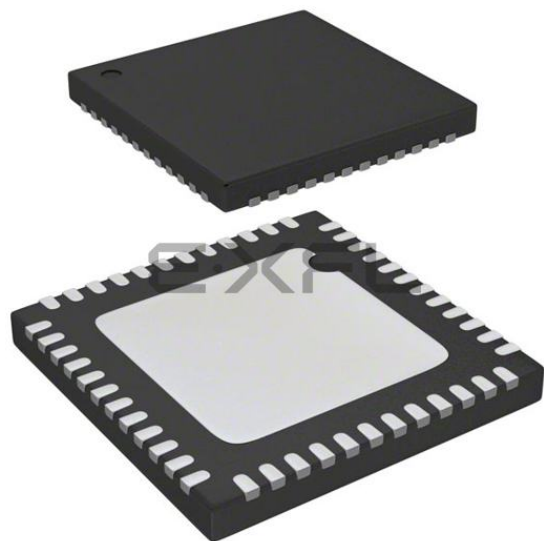




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D - 12b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32pg12b500f1024gm48-c

4.1.5 Current Consumption

4.1.5.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T_{OP} = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C.

Table 4.5. Current Consumption 3.3 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I _{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash ¹	—	126	—	μA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	99	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	99	TBD	μA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	124	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	102	TBD	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	280	TBD	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I _{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	88	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	234	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled	I _{EM1}	38.4 MHz crystal ¹	—	76	—	μA/MHz
		38 MHz HFRCO	—	50	TBD	μA/MHz
		26 MHz HFRCO	—	52	TBD	μA/MHz
		1 MHz HFRCO	—	230	TBD	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I _{EM1_VS}	19 MHz HFRCO	—	47	—	μA/MHz
		1 MHz HFRCO	—	193	—	μA/MHz
Current consumption in EM2 mode, with voltage scaling enabled.	I _{EM2_VS}	Full 256 kB RAM retention and RTCC running from LFXO	—	2.9	—	μA
		Full 256 kB RAM retention and RTCC running from LFRCO	—	3.2	—	μA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO ²	—	2.1	TBD	μA
Current consumption in EM3 mode, with voltage scaling enabled.	I _{EM3_VS}	Full 256 kB RAM retention and CRYOTIMER running from ULFR-CO	—	2.56	TBD	μA
Current consumption in EM4H mode, with voltage scaling enabled.	I _{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	1.0	—	μA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.45	—	μA
		128 byte RAM retention, no RTCC	—	0.43	TBD	μA

4.1.10 General-Purpose I/O (GPIO)

Table 4.17. General-Purpose I/O (GPIO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IL}	GPIO pins	—	—	$IOVDD \cdot 0.3$	V
Input high voltage	V_{IH}	GPIO pins	$IOVDD \cdot 0.7$	—	—	V
Output high voltage relative to IOVDD	V_{OH}	Sourcing 3 mA, $IOVDD \geq 3$ V, DRIVESTRENGTH ¹ = WEAK	$IOVDD \cdot 0.8$	—	—	V
		Sourcing 1.2 mA, $IOVDD \geq 1.62$ V, DRIVESTRENGTH ¹ = WEAK	$IOVDD \cdot 0.6$	—	—	V
		Sourcing 20 mA, $IOVDD \geq 3$ V, DRIVESTRENGTH ¹ = STRONG	$IOVDD \cdot 0.8$	—	—	V
		Sourcing 8 mA, $IOVDD \geq 1.62$ V, DRIVESTRENGTH ¹ = STRONG	$IOVDD \cdot 0.6$	—	—	V
Output low voltage relative to IOVDD	V_{OL}	Sinking 3 mA, $IOVDD \geq 3$ V, DRIVESTRENGTH ¹ = WEAK	—	—	$IOVDD \cdot 0.2$	V
		Sinking 1.2 mA, $IOVDD \geq 1.62$ V, DRIVESTRENGTH ¹ = WEAK	—	—	$IOVDD \cdot 0.4$	V
		Sinking 20 mA, $IOVDD \geq 3$ V, DRIVESTRENGTH ¹ = STRONG	—	—	$IOVDD \cdot 0.2$	V
		Sinking 8 mA, $IOVDD \geq 1.62$ V, DRIVESTRENGTH ¹ = STRONG	—	—	$IOVDD \cdot 0.4$	V
Input leakage current	I_{IOLEAK}	All GPIO except LFXO pins, GPIO $\leq IOVDD$, $T_{amb} \leq 85$ °C	—	0.1	TBD	nA
		LFXO Pins, GPIO $\leq IOVDD$, $T_{amb} \leq 85$ °C	—	0.1	TBD	nA
		All GPIO except LFXO pins, GPIO $\leq IOVDD$, $T_{AMB} > 85$ °C	—	—	TBD	nA
		LFXO Pins, GPIO $\leq IOVDD$, $T_{AMB} > 85$ °C	—	—	TBD	nA
Input leakage current on 5VTOL pads above IOVDD	$I_{5VTOLLEAK}$	$IOVDD < GPIO \leq IOVDD + 2$ V	—	3.3	15	μA
I/O pin pull-up/pull-down resistor	R_{PUD}		TBD	43	TBD	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		TBD	25	TBD	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Open-loop gain	G _{OL}	DRIVESTRENGTH = 3	—	135	—	dB
		DRIVESTRENGTH = 2	—	137	—	dB
		DRIVESTRENGTH = 1	—	121	—	dB
		DRIVESTRENGTH = 0	—	109	—	dB
Loop unit-gain frequency ⁷	UGF	DRIVESTRENGTH = 3, Buffer connection	—	3.38	—	MHz
		DRIVESTRENGTH = 2, Buffer connection	—	0.9	—	MHz
		DRIVESTRENGTH = 1, Buffer connection	—	132	—	kHz
		DRIVESTRENGTH = 0, Buffer connection	—	34	—	kHz
		DRIVESTRENGTH = 3, 3x Gain connection	—	2.57	—	MHz
		DRIVESTRENGTH = 2, 3x Gain connection	—	0.71	—	MHz
		DRIVESTRENGTH = 1, 3x Gain connection	—	113	—	kHz
		DRIVESTRENGTH = 0, 3x Gain connection	—	28	—	kHz
Phase margin	PM	DRIVESTRENGTH = 3, Buffer connection	—	67	—	°
		DRIVESTRENGTH = 2, Buffer connection	—	69	—	°
		DRIVESTRENGTH = 1, Buffer connection	—	63	—	°
		DRIVESTRENGTH = 0, Buffer connection	—	68	—	°
Output voltage noise	N _{OUT}	DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz	—	146	—	μVrms
		DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz	—	163	—	μVrms
		DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz	—	170	—	μVrms
		DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz	—	176	—	μVrms
		DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz	—	313	—	μVrms
		DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz	—	271	—	μVrms
		DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz	—	247	—	μVrms
		DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz	—	245	—	μVrms

4.2.1 Supply Current

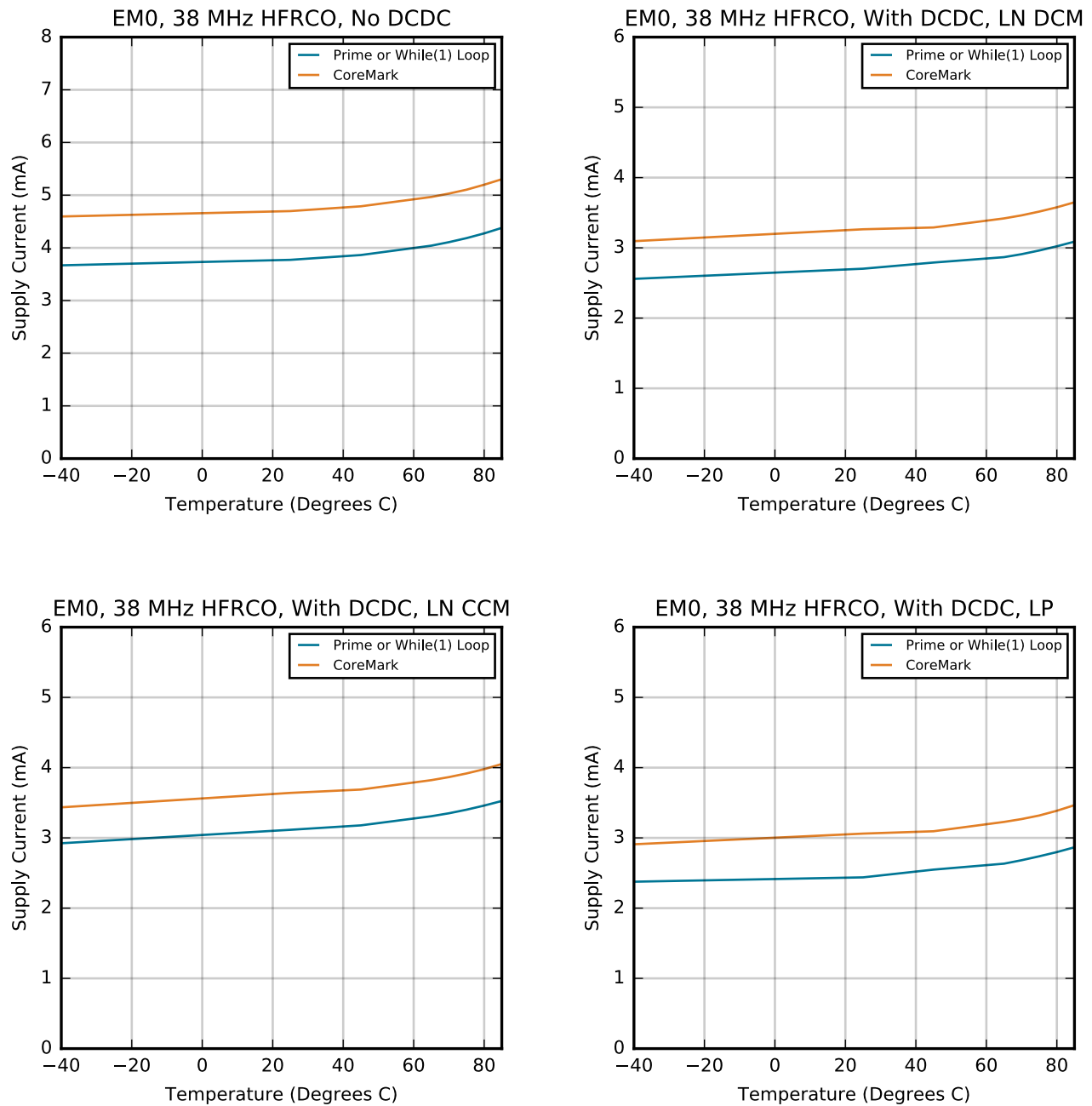


Figure 4.3. EM0 Active Mode Typical Supply Current vs. Temperature

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
A4	PC3	BUSAY BUSBX	WTIM0_CC0 #23 WTIM0_CC1 #21 WTIM0_CC2 #19 WTIM0_CDTI0 #15 WTIM0_CDTI1 #13 WTIM0_CDTI2 #11 WTIM1_CC0 #7 WTIM1_CC1 #5 WTIM1_CC2 #3 WTIM1_CC3 #1 PCNT1_S0IN #16 PCNT1_S1IN #15 PCNT2_S0IN #16 PCNT2_S1IN #15	US3_TX #21 US3_RX #20 US3_CLK #19 US3_CS #18 US3_CTS #17 US3_RTS #16 I2C1_SDA #16 I2C1_SCL #15	
A5	PC0	BUSBY BUSAX	WTIM0_CC0 #20 WTIM0_CC1 #18 WTIM0_CC2 #16 WTIM0_CDTI0 #12 WTIM0_CDTI1 #10 WTIM0_CDTI2 #8 WTIM1_CC0 #4 WTIM1_CC1 #2 WTIM1_CC2 #0 PCNT1_S0IN #13 PCNT1_S1IN #12 PCNT2_S0IN #13 PCNT2_S1IN #12	US3_TX #18 US3_RX #17 US3_CLK #16 US3_CS #15 US3_CTS #14 US3_RTS #13 I2C1_SDA #13 I2C1_SCL #12	
A6	PC11	BUSAY BUSBX	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 WTIM0_CC0 #31 WTIM0_CC1 #29 WTIM0_CC2 #27 WTIM0_CDTI0 #23 WTIM0_CDTI1 #21 WTIM0_CDTI2 #19 WTIM1_CC0 #15 WTIM1_CC1 #13 WTIM1_CC2 #11 WTIM1_CC3 #9 LE- TIM0_OUT0 #16 LE- TIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15 PCNT2_S0IN #20 PCNT2_S1IN #19	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15 I2C1_SDA #20 I2C1_SCL #19	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
D2	PF13	BUSAY BUSBX	WTIM1_CC3 #31 PCNT1_S0IN #26 PCNT1_S1IN #25 PCNT2_S0IN #26 PCNT2_S1IN #25	US2_TX #26 US2_RX #25 US2_CLK #24 US2_CS #23 US2_CTS #22 US2_RTS #21 US3_TX #26 US3_RX #25 US3_CLK #24 US3_CS #23 US3_CTS #22 US3_RTS #21 I2C1_SDA #26 I2C1_SCL #25	
D3	PF12	BUSBY BUSAX	WTIM1_CC3 #30 PCNT1_S0IN #25 PCNT1_S1IN #24 PCNT2_S0IN #25 PCNT2_S1IN #24	US2_TX #25 US2_RX #24 US2_CLK #23 US2_CS #22 US2_CTS #21 US2_RTS #20 US3_TX #25 US3_RX #24 US3_CLK #23 US3_CS #22 US3_CTS #21 US3_RTS #20 I2C1_SDA #25 I2C1_SCL #24	ETM_TD3 #0
D11	PB11	BUSCY BUSDX OPA2_P	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 WTIM0_CC0 #15 WTIM0_CC1 #13 WTIM0_CC2 #11 WTIM0_CDTI0 #7 WTIM0_CDTI1 #5 WTIM0_CDTI2 #3 LE- TIM0_OUT0 #6 LE- TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 US3_TX #15 US3_RX #14 US3_CLK #13 US3_CS #12 US3_CTS #11 US3_RTS #10 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6
D12	PB10	OPA2_OUTALT #1 BUSDY BUSCX	WTIM0_CC0 #14 WTIM0_CC1 #12 WTIM0_CC2 #10 WTIM0_CDTI0 #6 WTIM0_CDTI1 #4 WTIM0_CDTI2 #2 PCNT1_S0IN #10 PCNT1_S1IN #9 PCNT2_S0IN #10 PCNT2_S1IN #9	US2_TX #13 US2_RX #12 US2_CLK #11 US2_CS #10 US2_CTS #9 US2_RTS #8 US3_TX #14 US3_RX #13 US3_CLK #12 US3_CS #11 US3_CTS #10 US3_RTS #9 I2C1_SDA #10 I2C1_SCL #9	

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
D13	PB9	OPA2_OUTALT #0 BUSCY BUSDX	WTIM0_CC0 #13 WTIM0_CC1 #11 WTIM0_CC2 #9 WTIM0_CDTI0 #5 WTIM0_CDTI1 #3 WTIM0_CDTI2 #1 PCNT1_S0IN #9 PCNT1_S1IN #8 PCNT2_S0IN #9 PCNT2_S1IN #8	US2_TX #12 US2_RX #11 US2_CLK #10 US2_CS #9 US2_CTS #8 US2_RTS #7 US3_TX #13 US3_RX #12 US3_CLK #11 US3_CS #10 US3_CTS #9 US3_RTS #8 I2C1_SDA #9 I2C1_SCL #8	
E1	PK1		PCNT1_S0IN #30 PCNT1_S1IN #29 PCNT2_S0IN #30 PCNT2_S1IN #29	US2_TX #30 US2_RX #29 US2_CLK #28 US2_CS #27 US2_CTS #26 US2_RTS #25 US3_TX #30 US3_RX #29 US3_CLK #28 US3_CS #27 US3_CTS #26 US3_RTS #25 I2C1_SDA #30 I2C1_SCL #29	
E2	PK0	IDAC0_OUT	PCNT1_S0IN #29 PCNT1_S1IN #28 PCNT2_S0IN #29 PCNT2_S1IN #28	US2_TX #29 US2_RX #28 US2_CLK #27 US2_CS #26 US2_CTS #25 US2_RTS #24 US3_TX #29 US3_RX #28 US3_CLK #27 US3_CS #26 US3_CTS #25 US3_RTS #24 I2C1_SDA #29 I2C1_SCL #28	
E3	PF15	BUSAY BUSBX	PCNT1_S0IN #28 PCNT1_S1IN #27 PCNT2_S0IN #28 PCNT2_S1IN #27	US2_TX #28 US2_RX #27 US2_CLK #26 US2_CS #25 US2_CTS #24 US2_RTS #23 US3_TX #28 US3_RX #27 US3_CLK #26 US3_CS #25 US3_CTS #24 US3_RTS #23 I2C1_SDA #28 I2C1_SCL #27	
E5	VSS	Ground			
E6	VSS	Ground			
E7	VSS	Ground			
E8	VSS	Ground			
E9	VSS	Ground			
E12	PB8	BUSDY BUSCX	WTIM0_CC0 #12 WTIM0_CC1 #10 WTIM0_CC2 #8 WTIM0_CDTI0 #4 WTIM0_CDTI1 #2 WTIM0_CDTI2 #0 PCNT1_S0IN #8 PCNT1_S1IN #7 PCNT2_S0IN #8 PCNT2_S1IN #7	US2_TX #11 US2_RX #10 US2_CLK #9 US2_CS #8 US2_CTS #7 US2_RTS #6 US3_TX #12 US3_RX #11 US3_CLK #10 US3_CS #9 US3_CTS #8 US3_RTS #7 I2C1_SDA #8 I2C1_SCL #7	ETM_TD3 #2

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
M11	PD13	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSCY BUSDX OPA1_P	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 WTIM0_CDTI0 #29 WTIM0_CDTI1 #27 WTIM0_CDTI2 #25 WTIM1_CC0 #21 WTIM1_CC1 #19 WTIM1_CC2 #17 WTIM1_CC3 #15 LE- TIM0_OUT0 #21 LE- TIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 US3_TX #5 US3_RX #4 US3_CLK #3 US3_CS #2 US3_CTS #1 US3_RTS #0 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21 LES_CH5
M12	IOVDD	Digital IO power supply .			
M13	PA0	BUSDY BUSCX ADC0_EXTN	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 WTIM0_CC0 #0 LE- TIM0_OUT0 #0 LE- TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0 LES_CH8
N1	NC	No Connect.			
N2	NC	No Connect.			
N3	NC	No Connect.			
N4	NC	No Connect.			
N5	VSS	Ground			
N6	NC	No Connect.			
N7	NC	No Connect.			
N8	NC	No Connect.			

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
10	HFXTAL_N	High Frequency Crystal input pin.			
11	HFXTAL_P	High Frequency Crystal output pin.			
12	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
13	NC	No Connect.			
14	NC	No Connect.			
15	NC	No Connect.			
16	NC	No Connect.			
17	PD8	BUSDY BUSCX	WTIM0_CC1 #30 WTIM0_CC2 #28 WTIM0_CDTI0 #24 WTIM0_CDTI1 #22 WTIM0_CDTI2 #20 WTIM1_CC0 #16 WTIM1_CC1 #14 WTIM1_CC2 #12 WTIM1_CC3 #10	US3_TX #0 US3_RX #31 US3_CLK #30 US3_CS #29 US3_CTS #28 US3_RTS #27	LES_CH0
18	PD9	BUSCY BUSDX	TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 WTIM0_CC1 #31 WTIM0_CC2 #29 WTIM0_CDTI0 #25 WTIM0_CDTI1 #23 WTIM0_CDTI2 #21 WTIM1_CC0 #17 WTIM1_CC1 #15 WTIM1_CC2 #13 WTIM1_CC3 #11 LE- TIM0_OUT0 #17 LE- TIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16	US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 US3_TX #1 US3_RX #0 US3_CLK #31 US3_CS #30 US3_CTS #29 US3_RTS #28 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16	CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17 LES_CH1

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
21	PD12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BUSDY BUSCX	TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 WTIM0_CDTI0 #28 WTIM0_CDTI1 #26 WTIM0_CDTI2 #24 WTIM1_CC0 #20 WTIM1_CC1 #18 WTIM1_CC2 #16 WTIM1_CC3 #14 LE- TIM0_OUT0 #20 LE- TIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19	US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 US3_TX #4 US3_RX #3 US3_CLK #2 US3_CS #1 US3_CTS #0 US3_RTS #31 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19	PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20 LES_CH4
22	PD13	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSCY BUSDX OPA1_P	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 WTIM0_CDTI0 #29 WTIM0_CDTI1 #27 WTIM0_CDTI2 #25 WTIM1_CC0 #21 WTIM1_CC1 #19 WTIM1_CC2 #17 WTIM1_CC3 #15 LE- TIM0_OUT0 #21 LE- TIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 US3_TX #5 US3_RX #4 US3_CLK #3 US3_CS #2 US3_CTS #1 US3_RTS #0 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21 LES_CH5

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
PRS_CH7	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PA0						Peripheral Reflex System PRS, channel 7.
PRS_CH8	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PA0 10: PA1						Peripheral Reflex System PRS, channel 8.
PRS_CH9	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PA0 9: PA1 10: PA2 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11				Peripheral Reflex System PRS, channel 9.
PRS_CH10	0: PC6 1: PC7 2: PC8 3: PC9	4: PC10 5: PC11							Peripheral Reflex System PRS, channel 10.
PRS_CH11	0: PC7 1: PC8 2: PC9 3: PC10	4: PC11 5: PC6							Peripheral Reflex System PRS, channel 11.
TIM0_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 0 Capture Compare input / output channel 2.
TIM0_CDT10	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDT11	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDT12	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 1 Capture Compare input / output channel 1.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
TIM1_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 1 Capture Compare input / output channel 3.
US0_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART0 clock input / output.
US0_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART0 chip select input / output.
US0_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART0 Request To Send hardware flow control output.
US0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART1 clock input / output.
US1_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART1 chip select input / output.
US1_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART1 Clear To Send hardware flow control input.

Table 6.7. ACMP1 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSACMP1Y	BUSACMP1X	Bus
PB14	PB15	PB15	PB14	PF14	PF15	PF15	PF14			CH31
	PB13	PB13			PF13	PF13				CH30
PB12			PB12	PF12			PF12			CH29
	PB11	PB11			PF11	PF11				CH28
PB10			PB10	PF10			PF10			CH27
	PB9	PB9			PF9	PF9				CH26
PB8			PB8	PF8			PF8			CH25
	PB7	PB7			PF7	PF7				CH24
PB6			PB6	PF6			PF6			CH23
					PF5	PF5				CH22
				PF4			PF4			CH21
					PF3	PF3				CH20
				PF2			PF2			CH19
					PF1	PF1				CH18
				PF0			PF0			CH17
	PA7	PA7								CH16
PA6			PA6							CH15
	PA5	PA5								CH14
PA4			PA4							CH13
	PA3	PA3			PC11	PC11				CH12
PA2			PA2	PC10			PC10			CH11
	PA1	PA1			PC9	PC9				CH10
PA0			PA0	PC8			PC8			CH9
	PD15	PD15			PC7	PC7		PJ15	PJ15	CH8
PD14			PD14	PC6			PC6	PJ14	PJ14	CH7
	PD13	PD13			PC5	PC5				CH6
PD12			PD12	PC4			PC4			CH5
	PD11	PD11			PC3	PC3				CH4
PD10			PD10	PC2			PC2			CH3
	PD9	PD9			PC1	PC1				CH2
PD8			PD8	PC0			PC0			CH1
										CH0

7. BGA125 Package Specifications

7.1 BGA125 Package Dimensions

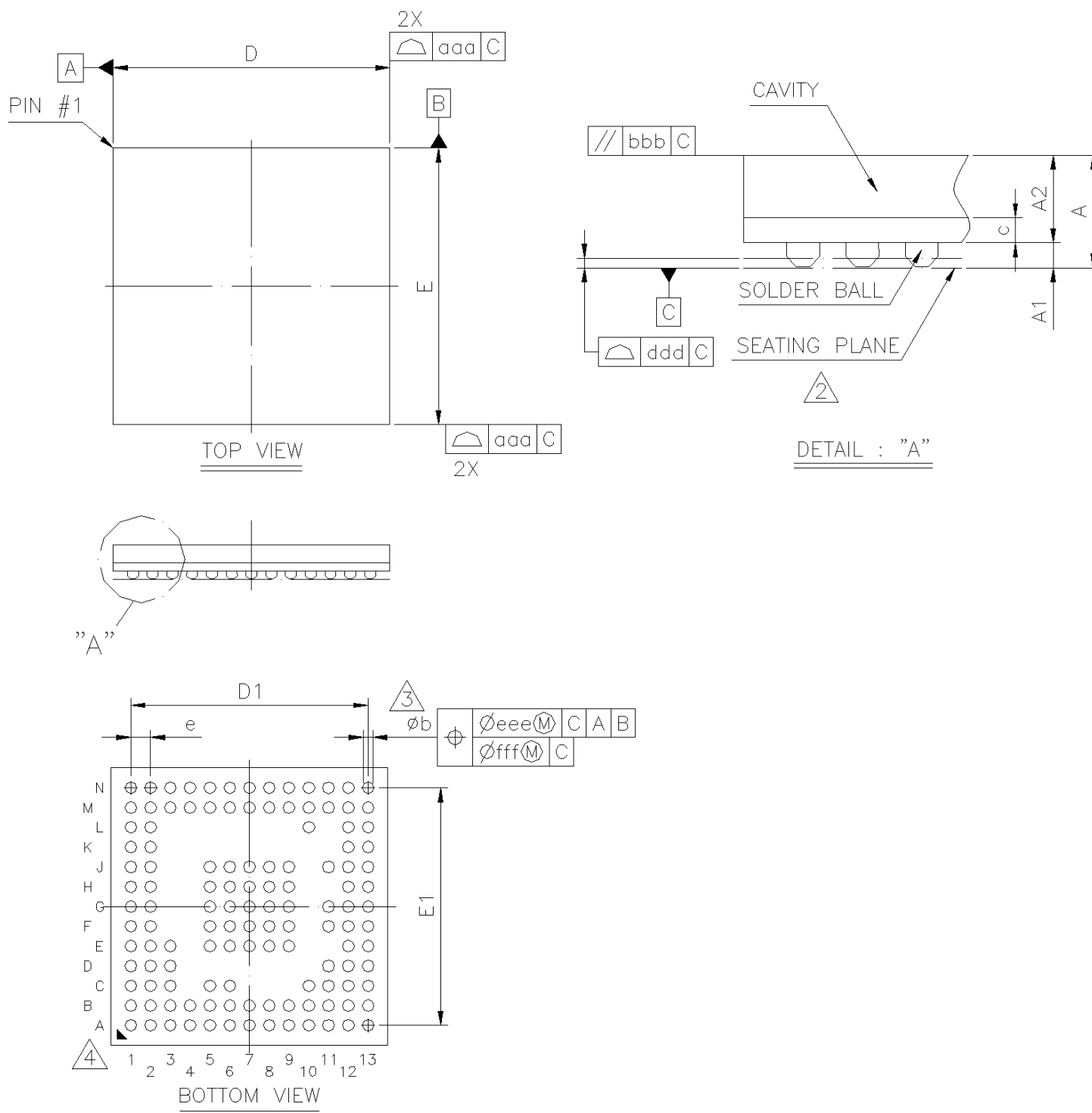


Figure 7.1. BGA125 Package Drawing

Table 7.1. BGA125 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.87	0.94
A1	0.16	0.21	0.26
A2	0.61	0.66	0.71
c	0.17	0.21	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D1	---	6.00	---
E1	---	6.00	---
e	---	0.50	---
b	0.25	0.30	0.35
aaa	0.10		
bbb	0.10		
ddd	0.08		
eee	0.15		
fff	0.05		
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.			

Table 7.2. BGA125 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.25	
C1		6.00	
C2		6.00	
E1		0.5	
E2		0.5	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Table 8.1. QFN48 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.15	5.30	5.45
E2	5.15	5.30	5.45
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
R	0.09	—	—
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 QFN48 PCB Land Pattern

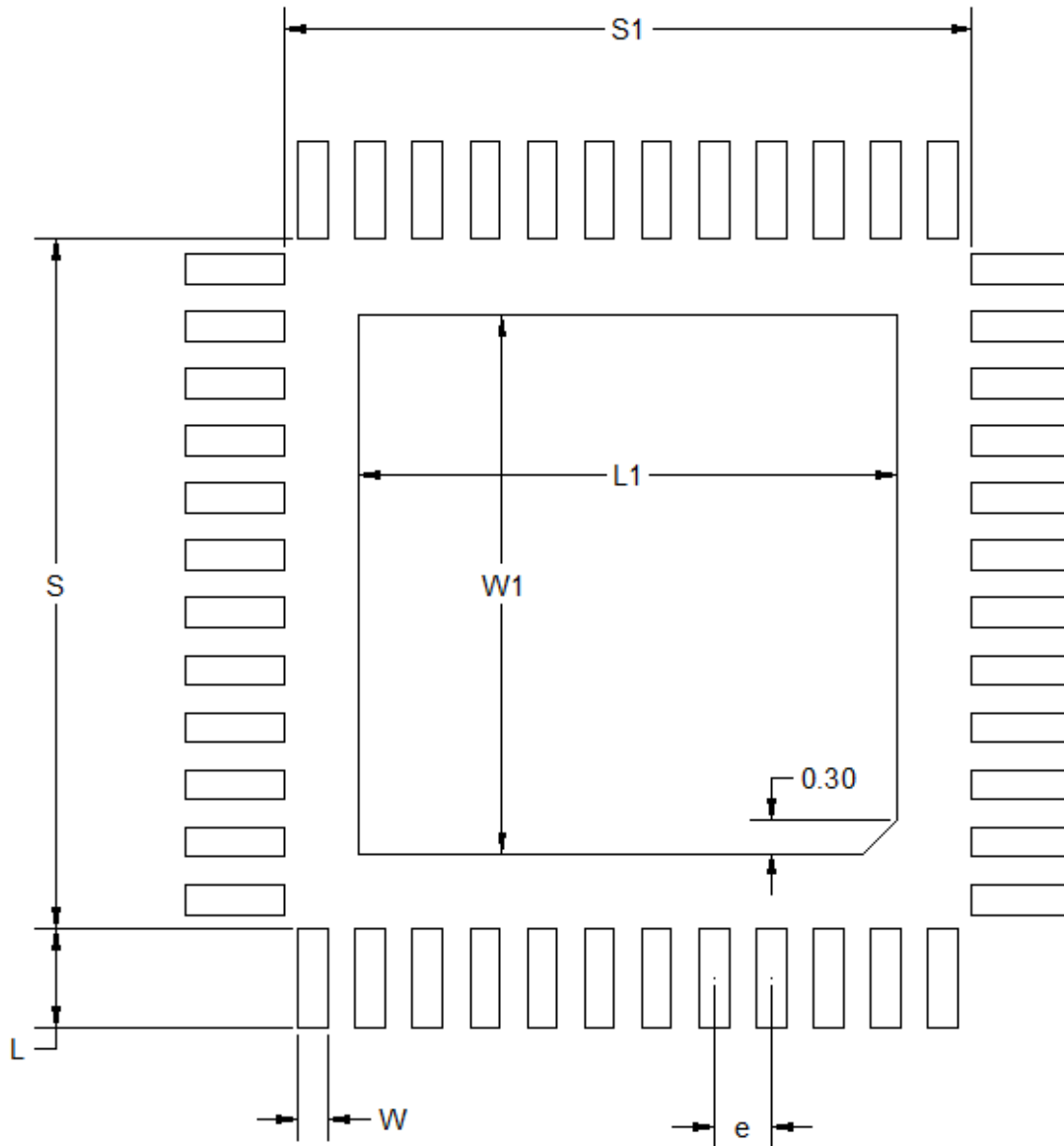


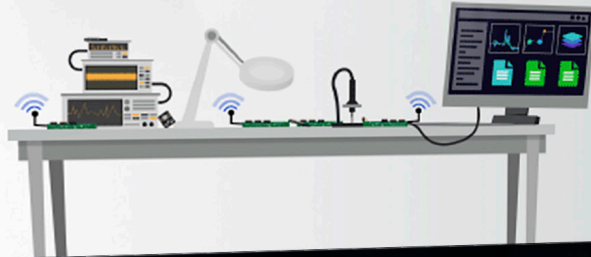
Figure 8.2. QFN48 PCB Land Pattern Drawing

Table of Contents

1. Feature List	1
2. Ordering Information	2
3. System Overview	3
3.1 Introduction	3
3.2 Power	4
3.2.1 Energy Management Unit (EMU)	4
3.2.2 DC-DC Converter	4
3.2.3 Power Domains	4
3.3 General Purpose Input/Output (GPIO)	5
3.4 Clocking	5
3.4.1 Clock Management Unit (CMU)	5
3.4.2 Internal and External Oscillators	5
3.5 Counters/Timers and PWM	5
3.5.1 Timer/Counter (TIMER)	5
3.5.2 Wide Timer/Counter (WTIMER)	5
3.5.3 Real Time Counter and Calendar (RTCC)	5
3.5.4 Low Energy Timer (LETIMER)	6
3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)	6
3.5.6 Pulse Counter (PCNT)	6
3.5.7 Watchdog Timer (WDOG)	6
3.6 Communications and Other Digital Peripherals	6
3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)	6
3.6.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)	6
3.6.3 Inter-Integrated Circuit Interface (I ² C)	6
3.6.4 Peripheral Reflex System (PRS)	6
3.6.5 Low Energy Sensor Interface (LESENSE)	7
3.7 Security Features	7
3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)	7
3.7.2 Crypto Accelerator (CRYPTO)	7
3.7.3 True Random Number Generator (TRNG)	7
3.7.4 Security Management Unit (SMU)	7
3.8 Analog	7
3.8.1 Analog Port (APORT)	7
3.8.2 Analog Comparator (ACMP)	7
3.8.3 Analog to Digital Converter (ADC)	8
3.8.4 Capacitive Sense (CSEN)	8
3.8.5 Digital to Analog Current Converter (IDAC)	8
3.8.6 Digital to Analog Converter (VDAC)	8
3.8.7 Operational Amplifiers	8
3.9 Reset Management Unit (RMU)	8
3.10 Core and Memory	8
3.10.1 Processor Core	8

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