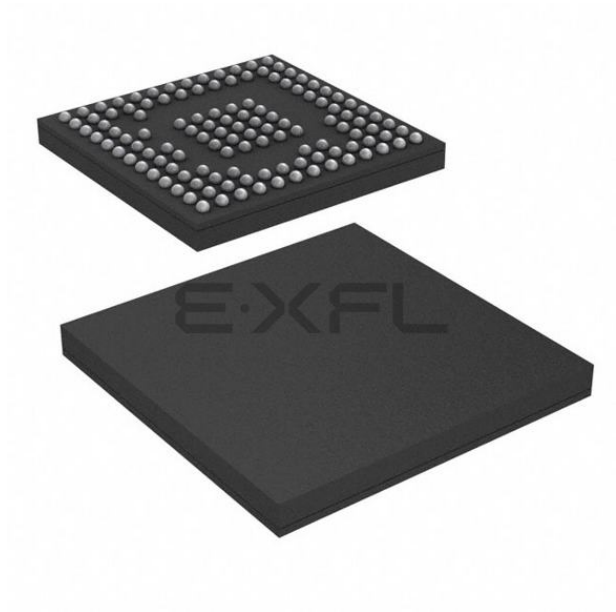

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What is "Embedded - Microcontrollers"?

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	65
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D - 12b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	125-VFBGA
Supplier Device Package	125-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32pg12b500f1024il125-br

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Con-verter	GPIO	Package	Temp Range
EFM32PG12B500F1024GL125-B	1024	256	Yes	65	BGA125	-40 to +85
EFM32PG12B500F1024IL125-B	1024	256	Yes	65	BGA125	-40 to +125
EFM32PG12B500F1024GM48-B	1024	256	Yes	33	QFN48	-40 to +85
EFM32PG12B500F1024IM48-B	1024	256	Yes	33	QFN48	-40 to +125

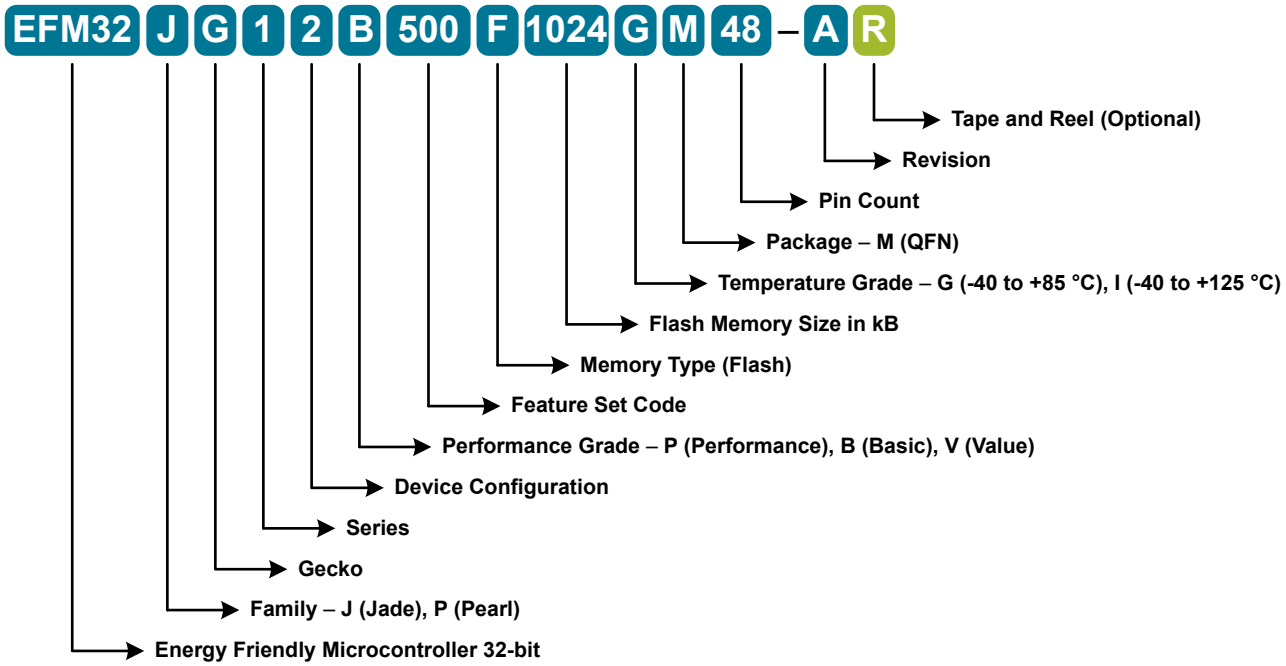


Figure 2.1. OPN Decoder

3. System Overview

3.1 Introduction

The EFM32PG12 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the EFM32PG12 Reference Manual.

A block diagram of the EFM32PG12 family is shown in Figure 3.1 Detailed EFM32PG12 Block Diagram on page 3. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

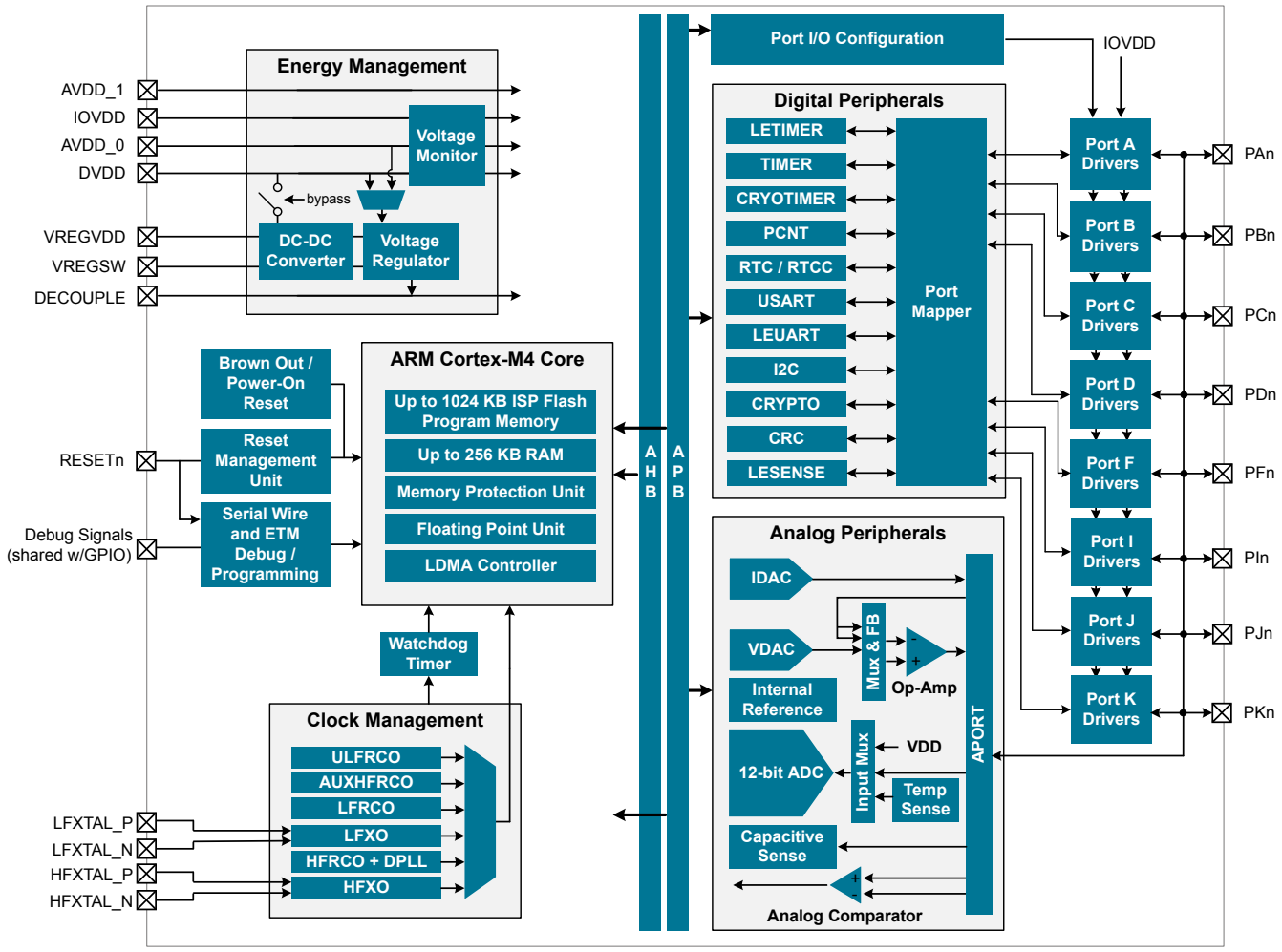


Figure 3.1. Detailed EFM32PG12 Block Diagram

3.3 General Purpose Input/Output (GPIO)

EFM32PG12 has up to 65 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32PG12. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFM32PG12 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 38 to 40 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire debug port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes.

3.6.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE™ is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.7 Security Features

3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFM32PG12 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO module allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.7.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.7.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only priveleged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.8 Analog

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.07	TBD	µA

Note:

1. CMU_HFXOCTRL_LOWPOWER=1.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.8.4 High-Freqency RC Oscillator (HFRCO)

Table 4.13. High-Freqency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	f_{HFRCO_ACC}	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
Start-up time	t_{HFRCO}	$f_{HFRCO} \geq 19$ MHz	—	300	—	ns
		$4 < f_{HFRCO} < 19$ MHz	—	1	—	µs
		$f_{HFRCO} \leq 4$ MHz	—	2.5	—	µs
Maximum DPLL lock time[1]	t_{DPLL_LOCK}	f_{REF} = 32.768 kHz, f_{HFRCO} = 39.98 MHz, N = 1219, M = 0	—	183	—	µs
Current consumption on all supplies	I_{HFRCO}	f_{HFRCO} = 38 MHz	—	244	TBD	µA
		f_{HFRCO} = 32 MHz	—	204	TBD	µA
		f_{HFRCO} = 26 MHz	—	173	TBD	µA
		f_{HFRCO} = 19 MHz	—	143	TBD	µA
		f_{HFRCO} = 16 MHz	—	123	TBD	µA
		f_{HFRCO} = 13 MHz	—	110	TBD	µA
		f_{HFRCO} = 7 MHz	—	85	TBD	µA
		f_{HFRCO} = 4 MHz	—	32	TBD	µA
		f_{HFRCO} = 2 MHz	—	31	TBD	µA
		f_{HFRCO} = 1 MHz	—	30	TBD	µA
		f_{HFRCO} = 40 MHz, DPLL enabled	—	385	TBD	µA
		f_{HFRCO} = 32 MHz, DPLL enabled	—	310	—	µA
		f_{HFRCO} = 16 MHz, DPLL enabled	—	203	—	µA
		f_{HFRCO} = 4 MHz, DPLL enabled	—	95	—	µA
		f_{HFRCO} = 1 MHz, DPLL enabled	—	79	—	µA
Coarse trim step size (% of period)	SS_{HFRCO_COARSE}		—	0.8	—	%
Fine trim step size (% of period)	SS_{HFRCO_FINE}		—	0.1	—	%
Period jitter	PJ_{HFRCO}		—	0.2	—	% RMS

Note:

1. Maximum DPLL lock time ~= 6 x (M+1) x t_{REF}, where t_{REF} is the reference clock period.

4.1.9 Flash Memory Characteristics[3]

Table 4.16. Flash Memory Characteristics[3]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		10000	—	—	cycles
Flash data retention	RET_{FLASH}	T_{AMB} ≤ 85 °C	10	—	—	years
		T_{AMB} ≤ 125 °C	10	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	24.4	30	µs
Page erase time	t_{PERASE}		20	26.4	35	ms
Mass erase time[1]	t_{MERASE}		20	26.5	35	ms
Device erase time[2]	t_{DERASE}	T_{AMB} ≤ 85 °C	—	69	100	ms
		T_{AMB} ≤ 125 °C	—	69	110	ms
Page erase current[4]	I_{ERASE}		—	—	1.6	mA
Write current[4]	I_{WRITE}		—	—	3.8	mA
Supply voltage during flash erase and write	V_{FLASH}		1.62	—	TBD	V

Note:

1. Mass erase is issued by the CPU and erases all flash.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
3. Flash data retention information is published in the Quarterly Quality and Reliability Report.
4. Measured at 25 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC clock frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	$f_{ADCRATE}$		—	—	1	Msps
Conversion time[1]	$t_{ADCCONV}$	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	$t_{ADCSTART}$	WARMUPMODE[4] = NORMAL	—	—	5	µs
		WARMUPMODE[4] = KEEPIN-STANDBY	—	—	2	µs
		WARMUPMODE[4] = KEEPINSLO-WACC	—	—	1	µs
SNDR at 1Msps and f_{IN} = 10kHz	$SNDR_{ADC}$	Internal reference, 2.5 V full-scale, differential (-1.25, 1.25)	TBD	67	—	dB
		vrefp_in = 1.25 V direct mode with 2.5 V full-scale, differential	—	68	—	dB
Spurious-free dynamic range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution, No missing co-des	TBD	—	TBD	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	TBD	—	TBD	LSB
Offset error	$V_{ADCOFFSETERR}$		TBD	0	TBD	LSB
Gain error in ADC	$V_{ADCGAIN}$	Using internal reference	—	-0.2	TBD	%
		Using external reference	—	-1	—	%
Temperature sensor slope	V_{TS_SLOPE}		—	-1.84	—	mV/°C

Note:

1. Derived from ADCCLK.
2. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
3. In ADCn_BIASPROG register.
4. In ADCn_CNTL register.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis (V_{CM} = 1.25 V, BIASPROG[4] = 0x10, FULLBIAS[4] = 1)	$V_{ACMPHYST}$	HYSTSEL[5] = HYST0	TBD	—	TBD	mV
		HYSTSEL[5] = HYST1	TBD	18	TBD	mV
		HYSTSEL[5] = HYST2	TBD	32	TBD	mV
		HYSTSEL[5] = HYST3	TBD	44	TBD	mV
		HYSTSEL[5] = HYST4	TBD	55	TBD	mV
		HYSTSEL[5] = HYST5	TBD	65	TBD	mV
		HYSTSEL[5] = HYST6	TBD	77	TBD	mV
		HYSTSEL[5] = HYST7	TBD	86	TBD	mV
		HYSTSEL[5] = HYST8	TBD	—	TBD	mV
		HYSTSEL[5] = HYST9	TBD	-18	TBD	mV
		HYSTSEL[5] = HYST10	TBD	-32	TBD	mV
		HYSTSEL[5] = HYST11	TBD	-43	TBD	mV
		HYSTSEL[5] = HYST12	TBD	-54	TBD	mV
		HYSTSEL[5] = HYST13	TBD	-64	TBD	mV
		HYSTSEL[5] = HYST14	TBD	-74	TBD	mV
		HYSTSEL[5] = HYST15	TBD	-85	TBD	mV
Comparator delay[3]	$t_{ACMPDELAY}$	BIASPROG[4] = 1, FULLBIAS[4] = 0	—	30	—	µs
		BIASPROG[4] = 0x10, FULLBIAS[4] = 0	—	3.7	—	µs
		BIASPROG[4] = 0x02, FULLBIAS[4] = 1	—	360	—	ns
		BIASPROG[4] = 0x20, FULLBIAS[4] = 1	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG[4] =0x10, FULLBIAS[4] = 1	TBD	—	TBD	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive sense internal resistance	R_{CSRES}	CSRESSEL[6] = 0	—	inf	—	kΩ
		CSRESSEL[6] = 1	—	15	—	kΩ
		CSRESSEL[6] = 2	—	27	—	kΩ
		CSRESSEL[6] = 3	—	39	—	kΩ
		CSRESSEL[6] = 4	—	51	—	kΩ
		CSRESSEL[6] = 5	—	102	—	kΩ
		CSRESSEL[6] = 6	—	164	—	kΩ
		CSRESSEL[6] = 7	—	239	—	kΩ

4.1.15 Current Digital to Analog Converter (IDAC)

Table 4.22. Current Digital to Analog Converter (IDAC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Number of ranges	N_{IDAC_RANGES}		—	4	—	-
Output current	I_{IDAC_OUT}	RANGSEL[1] = RANGE0	0.05	—	1.6	µA
		RANGSEL[1] = RANGE1	1.6	—	4.7	µA
		RANGSEL[1] = RANGE2	0.5	—	16	µA
		RANGSEL[1] = RANGE3	2	—	64	µA
Linear steps within each range	N_{IDAC_STEPS}		—	32	—	
Step size	SS_{IDAC}	RANGSEL[1] = RANGE0	—	50	—	nA
		RANGSEL[1] = RANGE1	—	100	—	nA
		RANGSEL[1] = RANGE2	—	500	—	nA
		RANGSEL[1] = RANGE3	—	2	—	µA
Total accuracy, STEPSEL[1] = 0x80	ACC_{IDAC}	EM0 or EM1, AVDD=3.3 V, T = 25 °C	TBD	—	TBD	%
		EM0 or EM1	TBD	—	TBD	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-2	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-1.7	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.8	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-0.7	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-0.6	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
Start up time	t_{IDAC_SU}	Output within 1% of steady state value	—	5	—	µs

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 µH, CDCDC = 4.7 µF, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

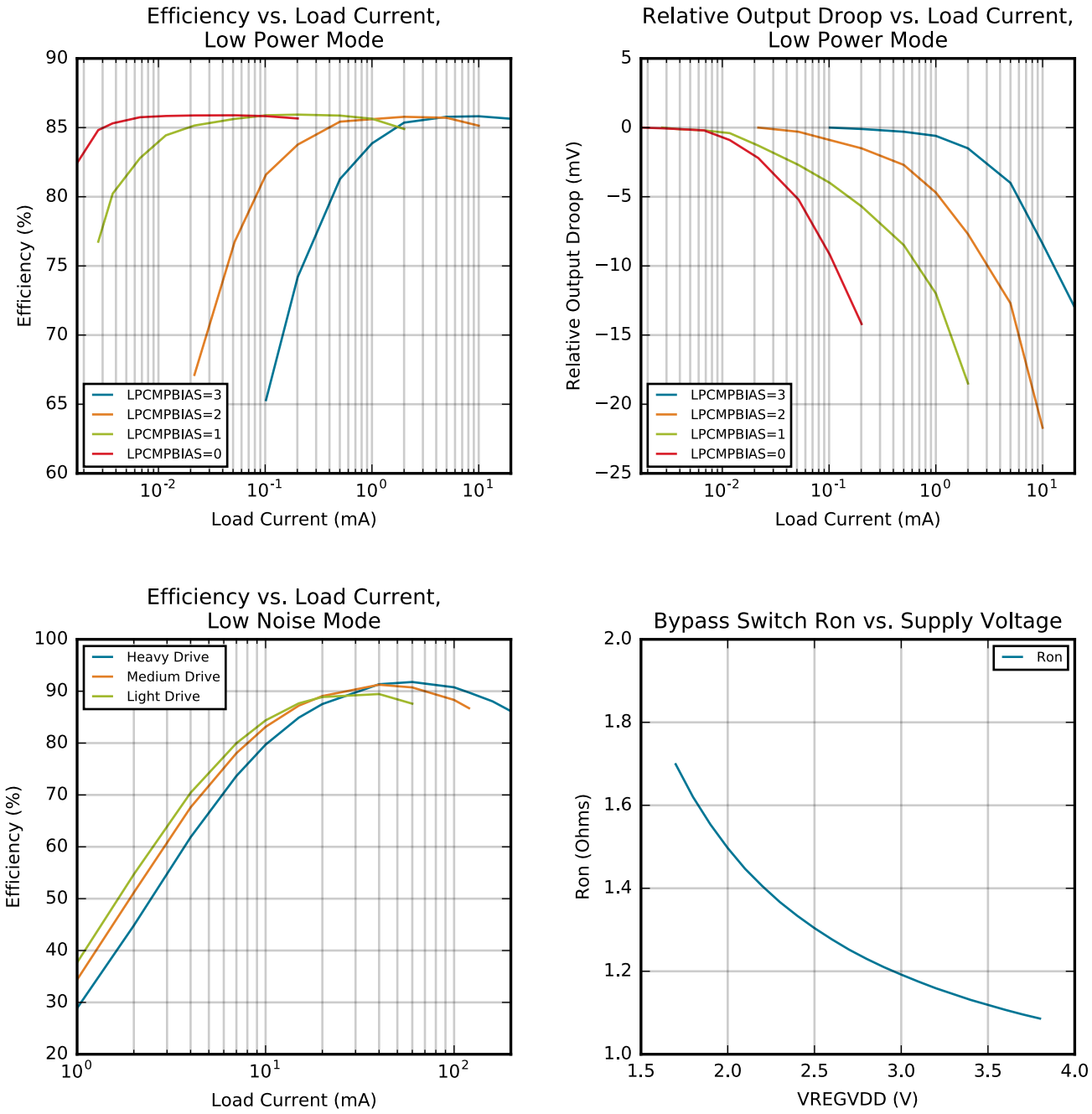


Figure 4.8. DC-DC Converter Typical Performance Characteristics

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
M11	PD13	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSCY BUSDX OPA1_P	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 WTIM0_CDTI0 #29 WTIM0_CDTI1 #27 WTIM0_CDTI2 #25 WTIM1_CC0 #21 WTIM1_CC1 #19 WTIM1_CC2 #17 WTIM1_CC3 #15 LE-TIM0_OUT0 #21 LE-TIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 US3_TX #5 US3_RX #4 US3_CLK #3 US3_CS #2 US3_CTS #1 US3_RTS #0 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21 LES_CH5
M12	IOVDD	Digital IO power supply .			
M13	PA0	BUSDY BUSCX ADC0_EXTN	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 WTIM0_CC0 #0 LE-TIM0_OUT0 #0 LE-TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0 LES_CH8
N1	NC	No Connect.			
N2	NC	No Connect.			
N3	NC	No Connect.			
N4	NC	No Connect.			
N5	VSS	Ground			
N6	NC	No Connect.			
N7	NC	No Connect.			
N8	NC	No Connect.			

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
6	PF5	BUSAY BUSBX	TIM0_CC0 #29 TIM0_CC1 #28 TIM0_CC2 #27 TIM0_CDTI0 #26 TIM0_CDTI1 #25 TIM0_CDTI2 #24 TIM1_CC0 #29 TIM1_CC1 #28 TIM1_CC2 #27 TIM1_CC3 #26 WTIM1_CC0 #29 WTIM1_CC1 #27 WTIM1_CC2 #25 WTIM1_CC3 #23 LE-TIM0_OUT0 #29 LE-TIM0_OUT1 #28 PCNT0_S0IN #29 PCNT0_S1IN #28	US0_TX #29 US0_RX #28 US0_CLK #27 US0_CS #26 US0_CTS #25 US0_RTS #24 US1_TX #29 US1_RX #28 US1_CLK #27 US1_CS #26 US1_CTS #25 US1_RTS #24 US2_TX #18 US2_RX #17 US2_CLK #16 US2_CS #15 US2_CTS #14 US2_RTS #13 LEU0_TX #29 LEU0_RX #28 I2C0_SDA #29 I2C0_SCL #28	PRS_CH0 #5 PRS_CH1 #4 PRS_CH2 #3 PRS_CH3 #2 ACMP0_O #29 ACMP1_O #29
7	PF6	BUSBY BUSAX	TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDTI0 #27 TIM0_CDTI1 #26 TIM0_CDTI2 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 WTIM1_CC0 #30 WTIM1_CC1 #28 WTIM1_CC2 #26 WTIM1_CC3 #24 LE-TIM0_OUT0 #30 LE-TIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29 PCNT1_S0IN #19 PCNT1_S1IN #18	US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 US2_TX #19 US2_RX #18 US2_CLK #17 US2_CS #16 US2_CTS #15 US2_RTS #14 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29	CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30
8	PF7	BUSAY BUSBX	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 WTIM1_CC0 #31 WTIM1_CC1 #29 WTIM1_CC2 #27 WTIM1_CC3 #25 LE-TIM0_OUT0 #31 LE-TIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30 PCNT1_S0IN #20 PCNT1_S1IN #19	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 US2_TX #20 US2_RX #19 US2_CLK #18 US2_CS #17 US2_CTS #16 US2_RTS #15 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	CMU_CLKI0 #1 CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1
9	AVDD	Analog power supply .			

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
TIM1_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 1 Capture Compare input / output channel 3.
US0_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART0 clock input / output.
US0_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART0 chip select input / output.
US0_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART0 Request To Send hardware flow control output.
US0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART1 clock input / output.
US1_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART1 chip select input / output.
US1_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART1 Clear To Send hardware flow control input.

Table 6.7. ACMP1 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSACMP1X																									PJ15	PJ14						
APORT0Y	BUSACMP1Y																									PJ15	PJ14						
APORT1X	BUSAX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10		PC8		PC6		PC4		PC2		PC0
APORT1Y	BUSAY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT2X	BUSBX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT2Y	BUSBY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10		PC8		PC6		PC4		PC2		PC0
APORT3X	BUSCX		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PA0		PD14		PD12		PD10		PD8
APORT3Y	BUSCY	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PA0		PD14		PD12		PD10		PD8

Table 6.8. ADC0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSADC0X																													PI3	PI2	PI1	PI0
APORT0Y	BUSADC0Y																													PI3	PI2	PI1	PI0
APORT1X	BUSAX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10		PC8		PC6		PC4		PC2		PC0
APORT1Y	BUSAY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT2X	BUSBX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT2Y	BUSBY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10		PC8		PC6		PC4		PC2		PC0
APORT3X	BUSCX		PB14		PB12		PB10		PB8		PB6							PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8
APORT3Y	BUSCY	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11		PB9		PB7								PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8
APORT4Y	BUSDY		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PA0		PD14		PD12		PD10		PD8

Table 7.1. BGA125 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.87	0.94
A1	0.16	0.21	0.26
A2	0.61	0.66	0.71
c	0.17	0.21	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D1	---	6.00	---
E1	---	6.00	---
e	---	0.50	---
b	0.25	0.30	0.35
aaa	0.10		
bbb	0.10		
ddd	0.08		
eee	0.15		
fff	0.05		

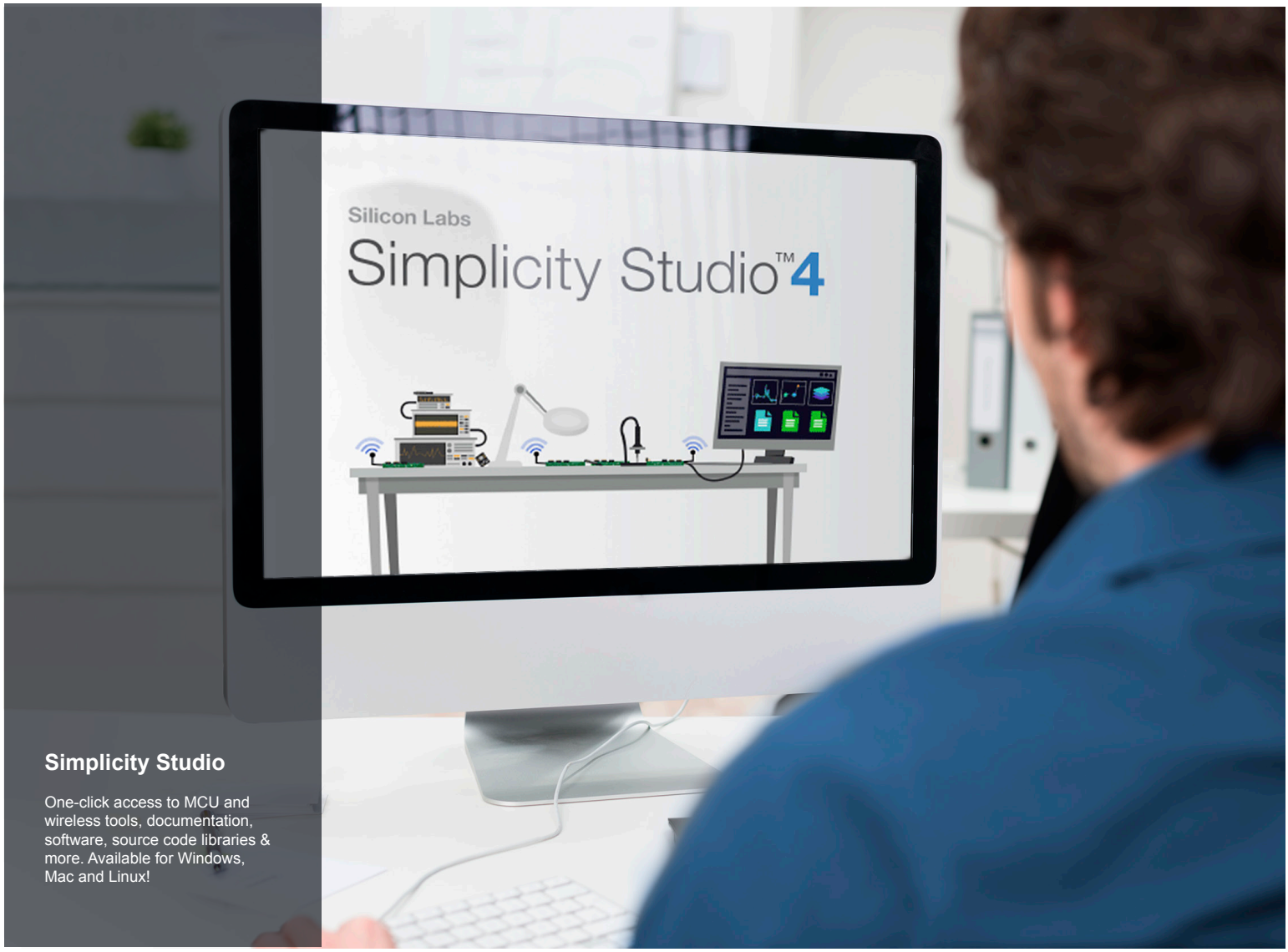
Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

8.3 QFN48 Package Marking

Figure 8.3. QFN48 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.



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