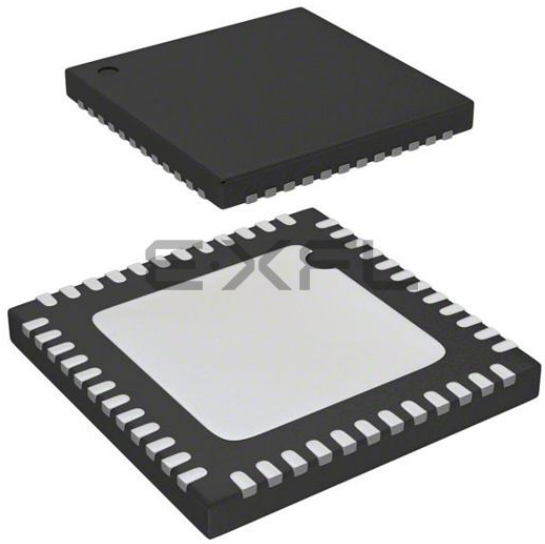
Silicon Labs - EFM32PG12B500F1024IM48-B Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D - 12b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32pg12b500f1024im48-b

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Con-verter	GPIO	Package	Temp Range
EFM32PG12B500F1024GL125-B	1024	256	Yes	65	BGA125	-40 to +85
EFM32PG12B500F1024IL125-B	1024	256	Yes	65	BGA125	-40 to +125
EFM32PG12B500F1024GM48-B	1024	256	Yes	33	QFN48	-40 to +85
EFM32PG12B500F1024IM48-B	1024	256	Yes	33	QFN48	-40 to +125

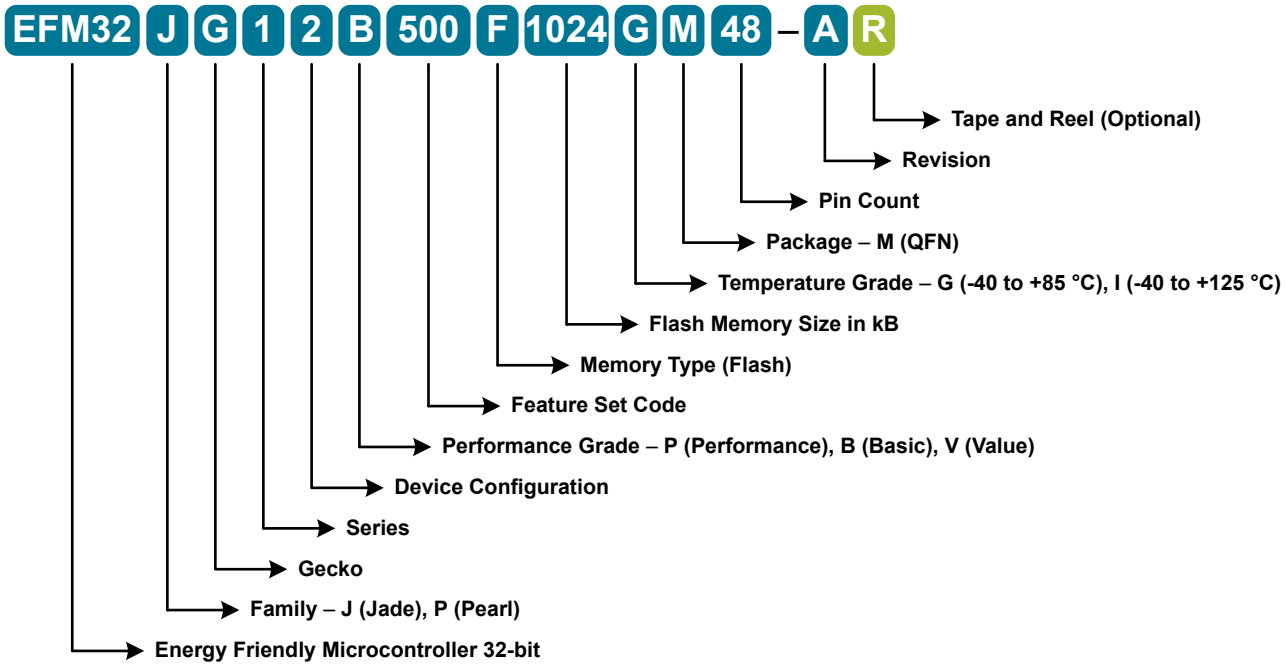

Figure 2.1. OPN Decoder

3.2 Power

The EFM32PG12 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32PG12 device family includes support for internal supply voltage scaling, as well as two different power domains groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 Power Domains

The EFM32PG12 has two peripheral power domains for operation in EM2 and lower. If all of the peripherals in a peripheral power domain are configured as unused, the power domain for that group will be powered off in the low-power mode, reducing the overall current consumption of the device.

Table 3.1. Peripheral Power Subdomains

Peripheral Power Domain 1	Peripheral Power Domain 2
ACMP0	ACMP1
PCNT0	PCNT1
ADC0	PCNT2
LETIMER0	CSEN
LESENSE	DAC0
APORT	LEUART0
-	I2C0
-	I2C1
-	IDAC

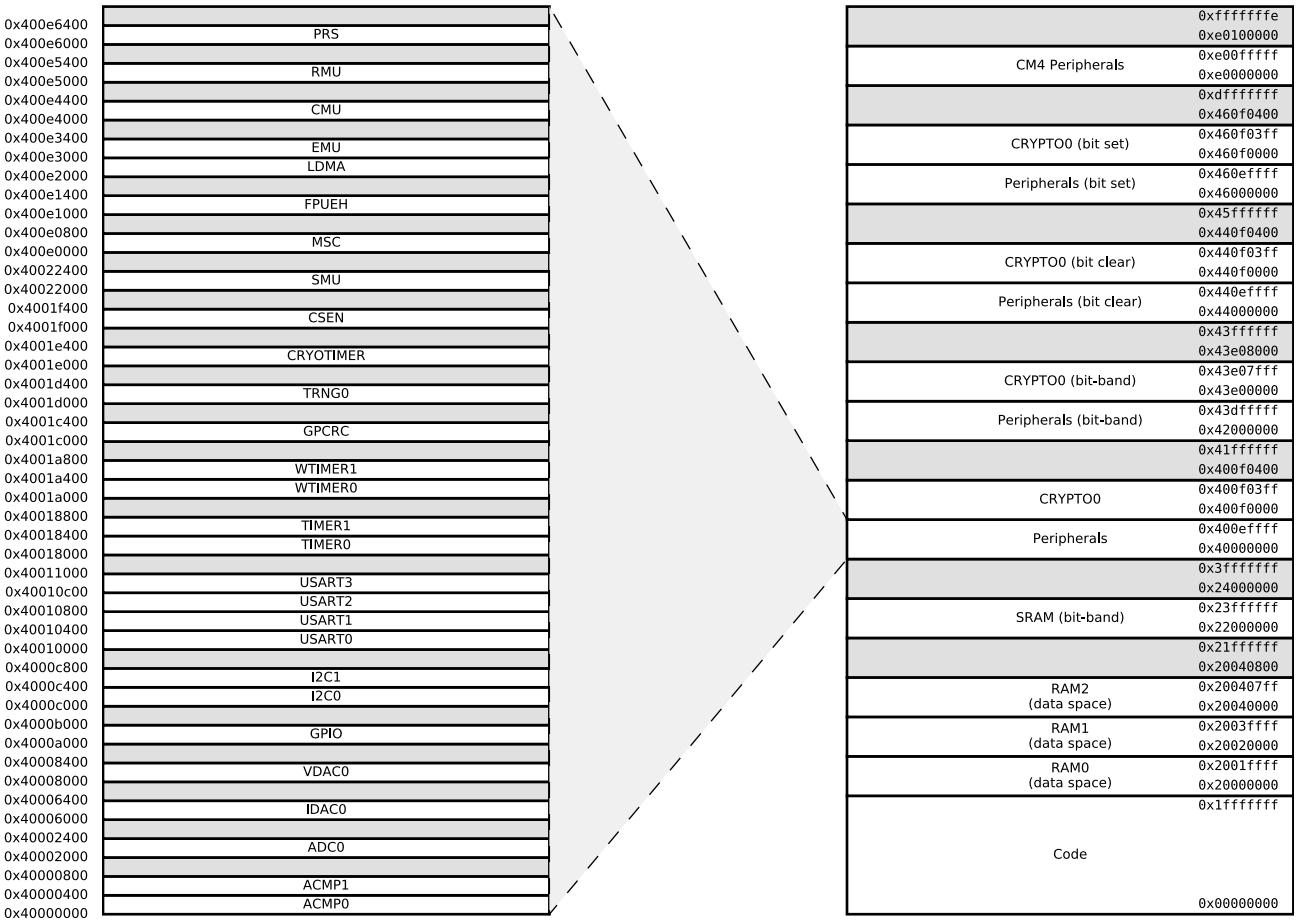

Figure 3.3. EFM32PG12 Memory Map — Peripherals

4.1.5 Current Consumption

4.1.5.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T_{OP} = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C.

Table 4.5. Current Consumption 3.3 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash[1]	—	126	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	99	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	99	TBD	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	124	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	102	TBD	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	280	TBD	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I_{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	88	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	234	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	38.4 MHz crystal[1]	—	76	—	µA/MHz
		38 MHz HFRCO	—	50	TBD	µA/MHz
		26 MHz HFRCO	—	52	TBD	µA/MHz
		1 MHz HFRCO	—	230	TBD	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I_{EM1_VS}	19 MHz HFRCO	—	47	—	µA/MHz
		1 MHz HFRCO	—	193	—	µA/MHz
Current consumption in EM2 mode, with votage scaling enabled.	I_{EM2_VS}	Full 256 kB RAM retention and RTCC running from LFXO	—	2.9	—	µA
		Full 256 kB RAM retention and RTCC running from LFRCO	—	3.2	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[2]	—	2.1	TBD	µA
Current consumption in EM3 mode, with voltage scaling enabled.	I_{EM3_VS}	Full 256 kB RAM retention and CRYOTIMER running from ULFRCO	—	2.56	TBD	µA
Current consumption in EM4H mode, with voltage scaling enabled.	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	1.0	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.45	—	µA
		128 byte RAM retention, no RTCC	—	0.43	TBD	µA

4.1.12 Analog to Digital Converter (ADC)

Table 4.19. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	$V_{RESOLUTION}$		6	—	12	Bits
Input voltage range	V_{ADCIN}	Single ended	—	—	$2xV_{REF}$	V
		Differential	$-V_{REF}$	—	V_{REF}	V
Input range of external reference voltage, single ended and differential	$V_{ADCREFIN\_P}$		1	—	V_{AVDD}	V
Power supply rejection[2]	$PSRR_{ADC}$	At DC	—	80	—	dB
Analog input common mode rejection ratio	$CMRR_{ADC}$	At DC	—	80	—	dB
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[4] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_LP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	270	TBD	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 [3]	—	125	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 [3]	—	80	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL	$I_{ADC\_NORMAL\_LP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	45	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 [3]	—	8	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_LP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	105	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	70	—	µA
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[4] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_HP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	325	—	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 [3]	—	175	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 [3]	—	125	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL	$I_{ADC\_NORMAL\_HP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	85	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 [3]	—	16	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_HP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	160	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	125	—	µA
Current from HFPERCLK	I_{ADC_CLK}	HFPERCLK = 16 MHz	—	180	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Open-loop gain	G_{OL}	DRIVESTRENGTH = 3	—	135	—	dB
		DRIVESTRENGTH = 2	—	137	—	dB
		DRIVESTRENGTH = 1	—	121	—	dB
		DRIVESTRENGTH = 0	—	109	—	dB
Loop unit-gain frequency[7]	UGF	DRIVESTRENGTH = 3, Buffer connection	—	3.38	—	MHz
		DRIVESTRENGTH = 2, Buffer connection	—	0.9	—	MHz
		DRIVESTRENGTH = 1, Buffer connection	—	132	—	kHz
		DRIVESTRENGTH = 0, Buffer connection	—	34	—	kHz
		DRIVESTRENGTH = 3, 3x Gain connection	—	2.57	—	MHz
		DRIVESTRENGTH = 2, 3x Gain connection	—	0.71	—	MHz
		DRIVESTRENGTH = 1, 3x Gain connection	—	113	—	kHz
		DRIVESTRENGTH = 0, 3x Gain connection	—	28	—	kHz
Phase margin	PM	DRIVESTRENGTH = 3, Buffer connection	—	67	—	°
		DRIVESTRENGTH = 2, Buffer connection	—	69	—	°
		DRIVESTRENGTH = 1, Buffer connection	—	63	—	°
		DRIVESTRENGTH = 0, Buffer connection	—	68	—	°
Output voltage noise	N_{OUT}	DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz	—	146	—	µVrms
		DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz	—	163	—	µVrms
		DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz	—	170	—	µVrms
		DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz	—	176	—	µVrms
		DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz	—	313	—	µVrms
		DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz	—	271	—	µVrms
		DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz	—	247	—	µVrms
		DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz	—	245	—	µVrms

SPI Slave Timing

Table 4.31. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [3] [2]	t_{SCLK}		8 * $t_{HFPERCLK}$	—	—	ns
SCLK high time [1] [3] [2]	t_{SCLK_HI}		3 * $t_{HFPERCLK}$	—	—	ns
SCLK low time [1] [3] [2]	t_{SCLK_LO}		3 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1] [3]	$t_{CS\_ACT\_MI}$		4	—	50	ns
CS disable to MISO [1] [3]	$t_{CS\_DIS\_MI}$		4	—	50	ns
MOSI setup time [1] [3]	t_{SU_MO}		4	—	—	ns
MOSI hold time [1] [3] [2]	t_{H_MO}		3 + 2 * $t_{HFPERCLK}$	—	—	ns
SCLK to MISO [1] [3] [2]	t_{SCLK_MI}		16 + $t_{HFPERCLK}$	—	66 + 2 * $t_{HFPERCLK}$	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

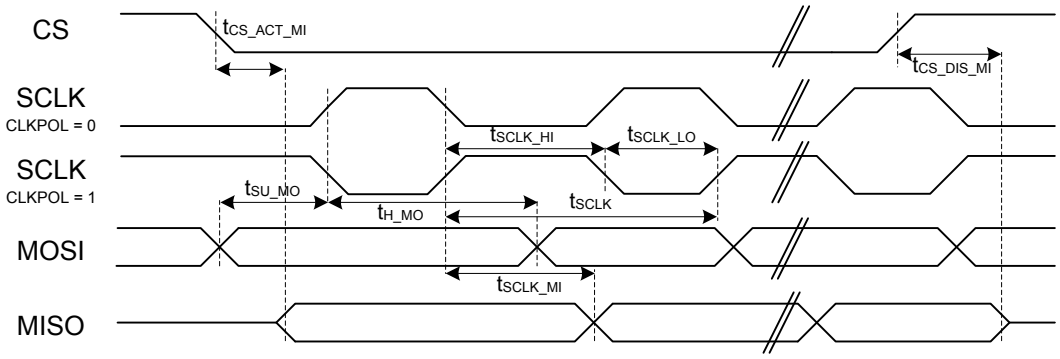

Figure 4.2. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

6. Pin Definitions

6.1 EFM32PG12B5xx in BGA125 Device Pinout

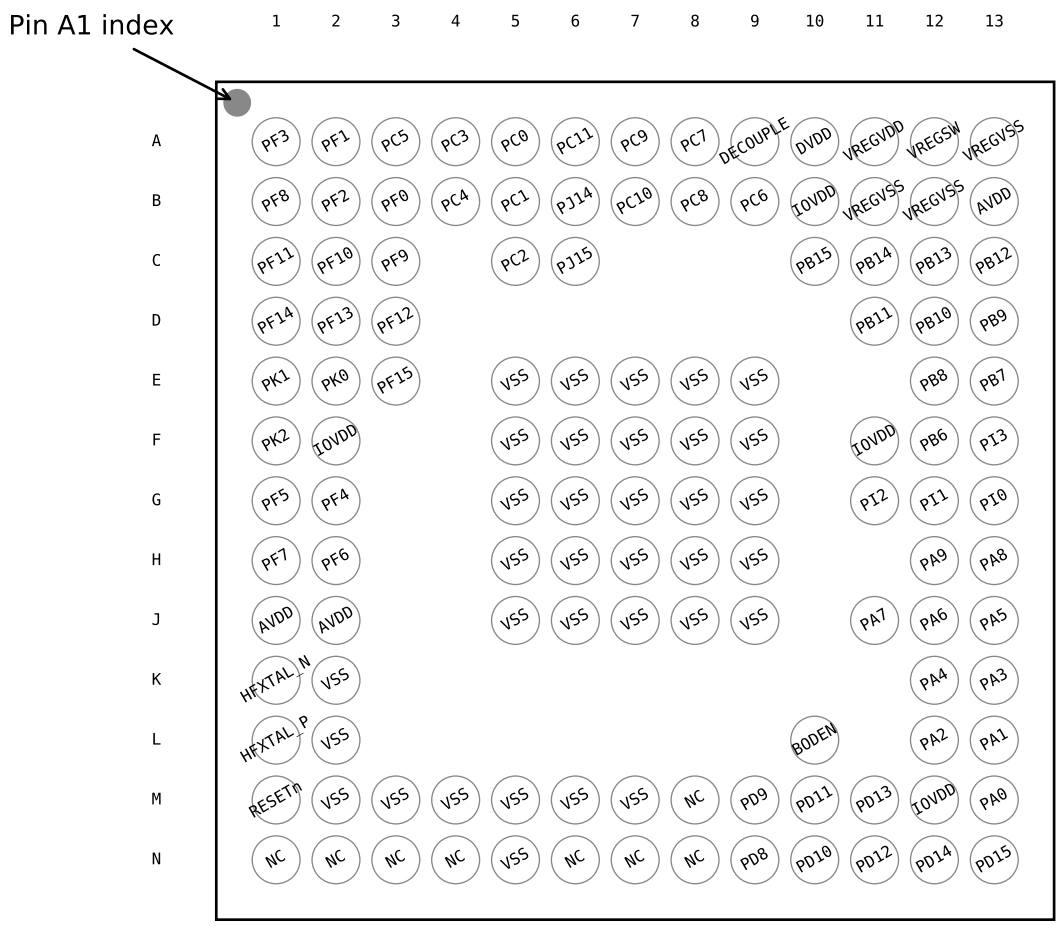

Figure 6.1. EFM32PG12B5xx in BGA125 Device Pinout

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
C10	PB15	BUSCY BUSDX LFXTAL_P	TIM0_CC0 #10 TIM0_CC1 #9 TIM0_CC2 #8 TIM0_CDTI0 #7 TIM0_CDTI1 #6 TIM0_CDTI2 #5 TIM1_CC0 #10 TIM1_CC1 #9 TIM1_CC2 #8 TIM1_CC3 #7 WTIM0_CC0 #19 WTIM0_CC1 #17 WTIM0_CC2 #15 WTIM0_CDTI0 #11 WTIM0_CDTI1 #9 WTIM0_CDTI2 #7 WTIM1_CC0 #3 WTIM1_CC1 #1 LE-TIM0_OUT0 #10 LE-TIM0_OUT1 #9 PCNT0_S0IN #10 PCNT0_S1IN #9	US0_TX #10 US0_RX #9 US0_CLK #8 US0_CS #7 US0_CTS #6 US0_RTS #5 US1_TX #10 US1_RX #9 US1_CLK #8 US1_CS #7 US1_CTS #6 US1_RTS #5 LEU0_TX #10 LEU0_RX #9 I2C0_SDA #10 I2C0_SCL #9	CMU_CLK0 #1 PRS_CH6 #10 PRS_CH7 #9 PRS_CH8 #8 PRS_CH9 #7 ACMP0_O #10 ACMP1_O #10
C11	PB14	BUSDY BUSCX LFXTAL_N	TIM0_CC0 #9 TIM0_CC1 #8 TIM0_CC2 #7 TIM0_CDTI0 #6 TIM0_CDTI1 #5 TIM0_CDTI2 #4 TIM1_CC0 #9 TIM1_CC1 #8 TIM1_CC2 #7 TIM1_CC3 #6 WTIM0_CC0 #18 WTIM0_CC1 #16 WTIM0_CC2 #14 WTIM0_CDTI0 #10 WTIM0_CDTI1 #8 WTIM0_CDTI2 #6 WTIM1_CC0 #2 WTIM1_CC1 #0 LE-TIM0_OUT0 #9 LE-TIM0_OUT1 #8 PCNT0_S0IN #9 PCNT0_S1IN #8	US0_TX #9 US0_RX #8 US0_CLK #7 US0_CS #6 US0_CTS #5 US0_RTS #4 US1_TX #9 US1_RX #8 US1_CLK #7 US1_CS #6 US1_CTS #5 US1_RTS #4 LEU0_TX #9 LEU0_RX #8 I2C0_SDA #9 I2C0_SCL #8	CMU_CLK1 #1 PRS_CH6 #9 PRS_CH7 #8 PRS_CH8 #7 PRS_CH9 #6 ACMP0_O #9 ACMP1_O #9

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
G13	PI0	BUSADC0Y BUSADC0X		US2_TX #5 US2_RX #4 US2_CLK #3 US2_CS #2 US2_CTS #1 US2_RTS #0	LES_ALTEX4
H1	PF7	BUSAY BUSBX	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 WTIM1_CC0 #31 WTIM1_CC1 #29 WTIM1_CC2 #27 WTIM1_CC3 #25 LE-TIM0_OUT0 #31 LE-TIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30 PCNT1_S0IN #20 PCNT1_S1IN #19	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 US2_TX #20 US2_RX #19 US2_CLK #18 US2_CS #17 US2_CTS #16 US2_RTS #15 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	CMU_CLKI0 #1 CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1
H2	PF6	BUSBY BUSAX	TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDTI0 #27 TIM0_CDTI1 #26 TIM0_CDTI2 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 WTIM1_CC0 #30 WTIM1_CC1 #28 WTIM1_CC2 #26 WTIM1_CC3 #24 LE-TIM0_OUT0 #30 LE-TIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29 PCNT1_S0IN #19 PCNT1_S1IN #18	US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 US2_TX #19 US2_RX #18 US2_CLK #17 US2_CS #16 US2_CTS #15 US2_RTS #14 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29	CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30
H5	VSS	Ground			
H6	VSS	Ground			
H7	VSS	Ground			
H8	VSS	Ground			
H9	VSS	Ground			

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
N9	PD8	BUSDY BUSCX	WTIM0_CC1 #30 WTIM0_CC2 #28 WTIM0_CDTI0 #24 WTIM0_CDTI1 #22 WTIM0_CDTI2 #20 WTIM1_CC0 #16 WTIM1_CC1 #14 WTIM1_CC2 #12 WTIM1_CC3 #10	US3_TX #0 US3_RX #31 US3_CLK #30 US3_CS #29 US3_CTS #28 US3_RTS #27	LES_CH0
N10	PD10	BUSDY BUSCX	TIM0_CC0 #18 TIM0_CC1 #17 TIM0_CC2 #16 TIM0_CDTI0 #15 TIM0_CDTI1 #14 TIM0_CDTI2 #13 TIM1_CC0 #18 TIM1_CC1 #17 TIM1_CC2 #16 TIM1_CC3 #15 WTIM0_CC2 #30 WTIM0_CDTI0 #26 WTIM0_CDTI1 #24 WTIM0_CDTI2 #22 WTIM1_CC0 #18 WTIM1_CC1 #16 WTIM1_CC2 #14 WTIM1_CC3 #12 LE-TIM0_OUT0 #18 LE-TIM0_OUT1 #17 PCNT0_S0IN #18 PCNT0_S1IN #17	US0_TX #18 US0_RX #17 US0_CLK #16 US0_CS #15 US0_CTS #14 US0_RTS #13 US1_TX #18 US1_RX #17 US1_CLK #16 US1_CS #15 US1_CTS #14 US1_RTS #13 US3_TX #2 US3_RX #1 US3_CLK #0 US3_CS #31 US3_CTS #30 US3_RTS #29 LEU0_TX #18 LEU0_RX #17 I2C0_SDA #18 I2C0_SCL #17	CMU_CLK1 #4 PRS_CH3 #9 PRS_CH4 #1 PRS_CH5 #0 PRS_CH6 #12 ACMP0_O #18 ACMP1_O #18 LES_CH2
N11	PD12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BUSDY BUSCX	TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 WTIM0_CDTI0 #28 WTIM0_CDTI1 #26 WTIM0_CDTI2 #24 WTIM1_CC0 #20 WTIM1_CC1 #18 WTIM1_CC2 #16 WTIM1_CC3 #14 LE-TIM0_OUT0 #20 LE-TIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19	US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 US3_TX #4 US3_RX #3 US3_CLK #2 US3_CS #1 US3_CTS #0 US3_RTS #31 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19	PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20 LES_CH4

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
10	HFXTAL_N	High Frequency Crystal input pin.			
11	HFXTAL_P	High Frequency Crystal output pin.			
12	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
13	NC	No Connect.			
14	NC	No Connect.			
15	NC	No Connect.			
16	NC	No Connect.			
17	PD8	BUSDY BUSCX	WTIM0_CC1 #30 WTIM0_CC2 #28 WTIM0_CDTI0 #24 WTIM0_CDTI1 #22 WTIM0_CDTI2 #20 WTIM1_CC0 #16 WTIM1_CC1 #14 WTIM1_CC2 #12 WTIM1_CC3 #10	US3_TX #0 US3_RX #31 US3_CLK #30 US3_CS #29 US3_CTS #28 US3_RTS #27	LES_CH0
18	PD9	BUSCY BUSDX	TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 WTIM0_CC1 #31 WTIM0_CC2 #29 WTIM0_CDTI0 #25 WTIM0_CDTI1 #23 WTIM0_CDTI2 #21 WTIM1_CC0 #17 WTIM1_CC1 #15 WTIM1_CC2 #13 WTIM1_CC3 #11 LE-TIM0_OUT0 #17 LE-TIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16	US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 US3_TX #1 US3_RX #0 US3_CLK #31 US3_CS #30 US3_CTS #29 US3_RTS #28 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16	CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17 LES_CH1

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
19	PD10	BUSDY BUSCX	TIM0_CC0 #18 TIM0_CC1 #17 TIM0_CC2 #16 TIM0_CDTI0 #15 TIM0_CDTI1 #14 TIM0_CDTI2 #13 TIM1_CC0 #18 TIM1_CC1 #17 TIM1_CC2 #16 TIM1_CC3 #15 WTIM0_CC2 #30 WTIM0_CDTI0 #26 WTIM0_CDTI1 #24 WTIM0_CDTI2 #22 WTIM1_CC0 #18 WTIM1_CC1 #16 WTIM1_CC2 #14 WTIM1_CC3 #12 LE-TIM0_OUT0 #18 LE-TIM0_OUT1 #17 PCNT0_S0IN #18 PCNT0_S1IN #17	US0_TX #18 US0_RX #17 US0_CLK #16 US0_CS #15 US0_CTS #14 US0_RTS #13 US1_TX #18 US1_RX #17 US1_CLK #16 US1_CS #15 US1_CTS #14 US1_RTS #13 US3_TX #2 US3_RX #1 US3_CLK #0 US3_CS #31 US3_CTS #30 US3_RTS #29 LEU0_TX #18 LEU0_RX #17 I2C0_SDA #18 I2C0_SCL #17	CMU_CLK1 #4 PRS_CH3 #9 PRS_CH4 #1 PRS_CH5 #0 PRS_CH6 #12 ACMP0_O #18 ACMP1_O #18 LES_CH2
20	PD11	BUSCY BUSDX	TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 WTIM0_CC2 #31 WTIM0_CDTI0 #27 WTIM0_CDTI1 #25 WTIM0_CDTI2 #23 WTIM1_CC0 #19 WTIM1_CC1 #17 WTIM1_CC2 #15 WTIM1_CC3 #13 LE-TIM0_OUT0 #19 LE-TIM0_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18	US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 US3_TX #3 US3_RX #2 US3_CLK #1 US3_CS #0 US3_CTS #31 US3_RTS #30 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18	PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19 LES_CH3

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
ETM_TD2	0: PF11 1: PA8 2: PB7 3: PC9								Embedded Trace Module ETM data 2.
ETM_TD3	0: PF12 1: PA9 2: PB8 3: PC10								Embedded Trace Module ETM data 3.
GPIO_EM4WU0	0: PF2								Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PF7								Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PD14								Pin can be used to wake the system up from EM4
GPIO_EM4WU8	0: PA3								Pin can be used to wake the system up from EM4
GPIO_EM4WU9	0: PB13								Pin can be used to wake the system up from EM4
GPIO_EM4WU12	0: PC10								Pin can be used to wake the system up from EM4
I2C0_SCL	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	I2C0 Serial Clock Line input / output.
I2C0_SDA	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	I2C0 Serial Data input / output.
I2C1_SCL	0: PA7 1: PA8 2: PA9 3: PI2	4: PI3 5: PB6 6: PB7 7: PB8	8: PB9 9: PB10 10: PJ14 11: PJ15	12: PC0 13: PC1 14: PC2 15: PC3	16: PC4 17: PC5 18: PC10 19: PC11	20: PF8 21: PF9 22: PF10 23: PF11	24: PF12 25: PF13 26: PF14 27: PF15	28: PK0 29: PK1 30: PK2 31: PA6	I2C1 Serial Clock Line input / output.
I2C1_SDA	0: PA6 1: PA7 2: PA8 3: PA9	4: PI2 5: PI3 6: PB6 7: PB7	8: PB8 9: PB9 10: PB10 11: PJ14	12: PJ15 13: PC0 14: PC1 15: PC2	16: PC3 17: PC4 18: PC5 19: PC10	20: PC11 21: PF8 22: PF9 23: PF10	24: PF11 25: PF12 26: PF13 27: PF14	28: PF15 29: PK0 30: PK1 31: PK2	I2C1 Serial Data input / output.
IDAC0_OUT	0: PK0								IDAC0 output.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US3_CLK	0: PD10 1: PD11 2: PD12 3: PD13	4: PD14 5: PD15 6: PI2 7: PI3	8: PB6 9: PB7 10: PB8 11: PB9	12: PB10 13: PB11 14: PJ14 15: PJ15	16: PC0 17: PC1 18: PC2 19: PC3	20: PC4 21: PC5 22: PF11 23: PF12	24: PF13 25: PF14 26: PF15 27: PK0	28: PK1 29: PK2 30: PD8 31: PD9	USART3 clock input / output.
US3_CS	0: PD11 1: PD12 2: PD13 3: PD14	4: PD15 5: PI2 6: PI3 7: PB6	8: PB7 9: PB8 10: PB9 11: PB10	12: PB11 13: PJ14 14: PJ15 15: PC0	16: PC1 17: PC2 18: PC3 19: PC4	20: PC5 21: PF11 22: PF12 23: PF13	24: PF14 25: PF15 26: PK0 27: PK1	28: PK2 29: PD8 30: PD9 31: PD10	USART3 chip select input / output.
US3_CTS	0: PD12 1: PD13 2: PD14 3: PD15	4: PI2 5: PI3 6: PB6 7: PB7	8: PB8 9: PB9 10: PB10 11: PB11	12: PJ14 13: PJ15 14: PC0 15: PC1	16: PC2 17: PC3 18: PC4 19: PC5	20: PF11 21: PF12 22: PF13 23: PF14	24: PF15 25: PK0 26: PK1 27: PK2	28: PD8 29: PD9 30: PD10 31: PD11	USART3 Clear To Send hardware flow control input.
US3_RTS	0: PD13 1: PD14 2: PD15 3: PI2	4: PI3 5: PB6 6: PB7 7: PB8	8: PB9 9: PB10 10: PB11 11: PJ14	12: PJ15 13: PC0 14: PC1 15: PC2	16: PC3 17: PC4 18: PC5 19: PF11	20: PF12 21: PF13 22: PF14 23: PF15	24: PK0 25: PK1 26: PK2 27: PD8	28: PD9 29: PD10 30: PD11 31: PD12	USART3 Request To Send hardware flow control output.
US3_RX	0: PD9 1: PD10 2: PD11 3: PD12	4: PD13 5: PD14 6: PD15 7: PI2	8: PI3 9: PB6 10: PB7 11: PB8	12: PB9 13: PB10 14: PB11 15: PJ14	16: PJ15 17: PC0 18: PC1 19: PC2	20: PC3 21: PC4 22: PC5 23: PF11	24: PF12 25: PF13 26: PF14 27: PF15	28: PK0 29: PK1 30: PK2 31: PD8	USART3 Asynchronous Receive. USART3 Synchronous mode Master Input / Slave Output (MISO).
US3_TX	0: PD8 1: PD9 2: PD10 3: PD11	4: PD12 5: PD13 6: PD14 7: PD15	8: PI2 9: PI3 10: PB6 11: PB7	12: PB8 13: PB9 14: PB10 15: PB11	16: PJ14 17: PJ15 18: PC0 19: PC1	20: PC2 21: PC3 22: PC4 23: PC5	24: PF11 25: PF12 26: PF13 27: PF14	28: PF15 29: PK0 30: PK1 31: PK2	USART3 Asynchronous Transmit. Also used as receive input in half duplex communication. USART3 Synchronous mode Master Output / Slave Input (MOSI).
VDAC0_EXT	0: PA1								Digital to analog converter VDAC0 external reference input pin.
VDAC0_OUT0 / OPA0_OUT	0: PA3								Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT0ALT / OPA0_OUTALT	0: PA5 1: PD13 2: PD15								Digital to Analog Converter DAC0 alternative output for channel 0.
VDAC0_OUT1 / OPA1_OUT	0: PD14								Digital to Analog Converter DAC0 output channel number 1.
VDAC0_OUT1ALT / OPA1_OUTALT	0: PD12 1: PA2 2: PA4								Digital to Analog Converter DAC0 alternative output for channel 1.

PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

Table 6.6. ACMP0 Bus and Pin Mapping

Port	APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X
Bus	BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSACMP0Y	BUSACMP0X
CH31		PB15	PB15			PF15	PF15			
CH30	PB14			PB14	PF14			PF14		
CH29		PB13	PB13			PF13	PF13			
CH28	PB12			PB12	PF12			PF12		
CH27		PB11	PB11			PF11	PF11			
CH26	PB10			PB10	PF10			PF10		
CH25		PB9	PB9			PF9	PF9			
CH24	PB8			PB8	PF8			PF8		
CH23		PB7	PB7			PF7	PF7			
CH22	PB6			PB6	PF6			PF6		
CH21						PF5	PF5			
CH20					PF4			PF4		
CH19						PF3	PF3			
CH18					PF2			PF2		
CH17						PF1	PF1			
CH16					PF0			PF0		
CH15		PA7	PA7							
CH14	PA6			PA6						
CH13		PA5	PA5							
CH12	PA4			PA4						
CH11		PA3	PA3			PC11	PC11			
CH10	PA2			PA2	PC10			PC10		
CH9		PA1	PA1			PC9	PC9			
CH8	PA0			PA0	PC8			PC8		
CH7		PD15	PD15			PC7	PC7			
CH6	PD14			PD14	PC6			PC6		
CH5		PD13	PD13			PC5	PC5			
CH4	PD12			PD12	PC4			PC4		
CH3		PD11	PD11			PC3	PC3			
CH2	PD10			PD10	PC2			PC2		
CH1		PD9	PD9			PC1	PC1		PA9	PA9
CH0	PD8			PD8	PC0			PC0	PA8	PA8

Table 7.1. BGA125 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.87	0.94
A1	0.16	0.21	0.26
A2	0.61	0.66	0.71
c	0.17	0.21	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D1	---	6.00	---
E1	---	6.00	---
e	---	0.50	---
b	0.25	0.30	0.35
aaa	0.10		
bbb	0.10		
ddd	0.08		
eee	0.15		
fff	0.05		

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

7.2 BGA125 PCB Land Pattern

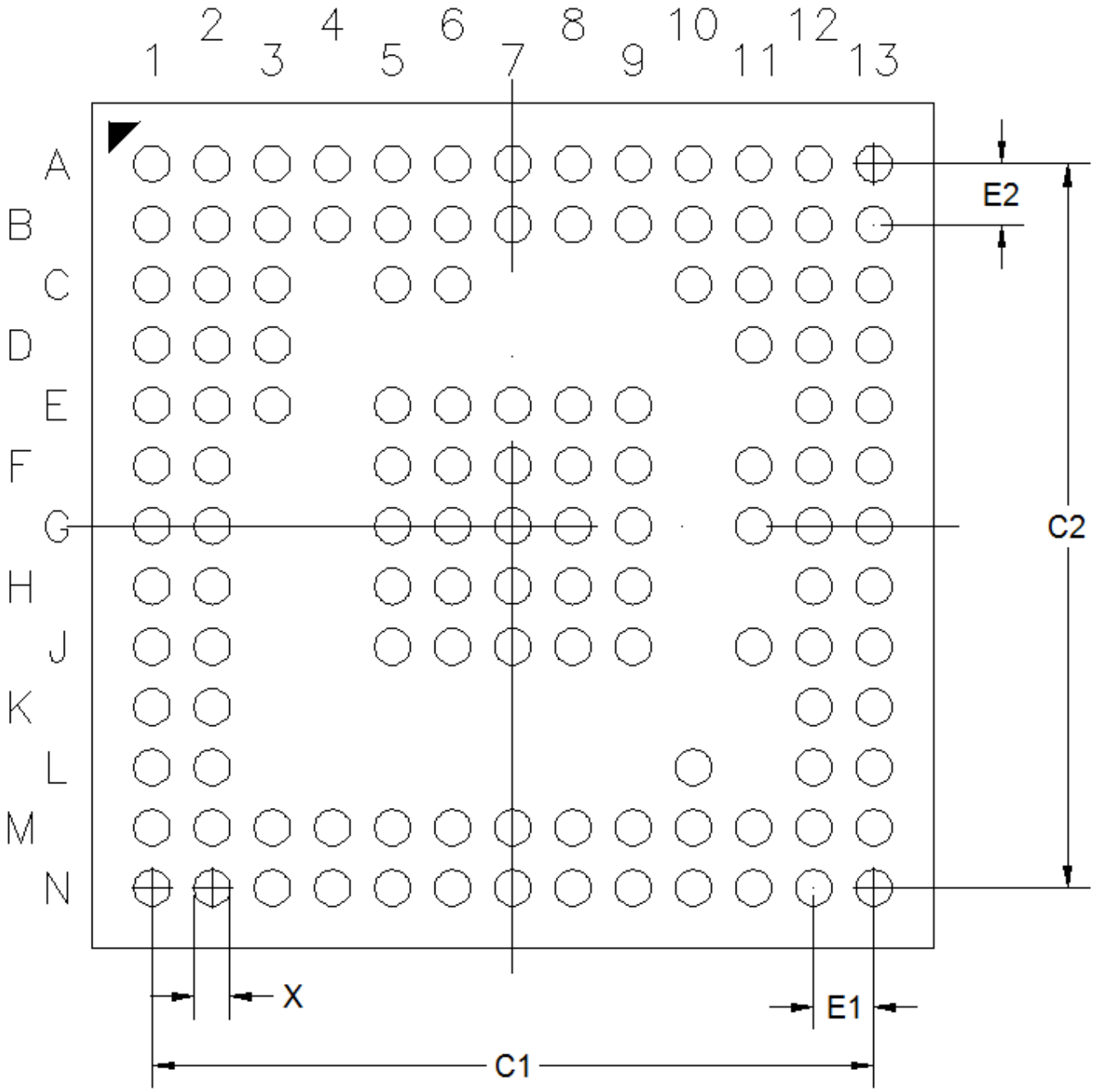

Figure 7.2. BGA125 PCB Land Pattern Drawing

Table 8.2. QFN48 PCB Land Pattern Dimensions

Dimension	Typ
S1	6.01
S	6.01
L1	4.70
W1	4.70
e	0.50
W	0.26
L	0.86

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 4x4 array of 0.75 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.