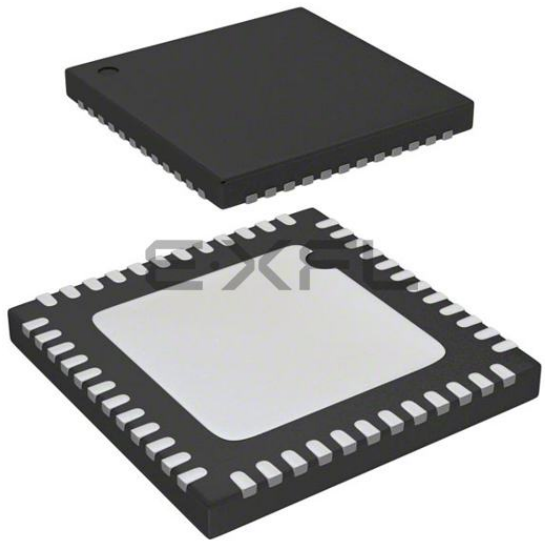
Silicon Labs - EFM32PG12B500F1024IM48-BR Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D - 12b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32pg12b500f1024im48-br

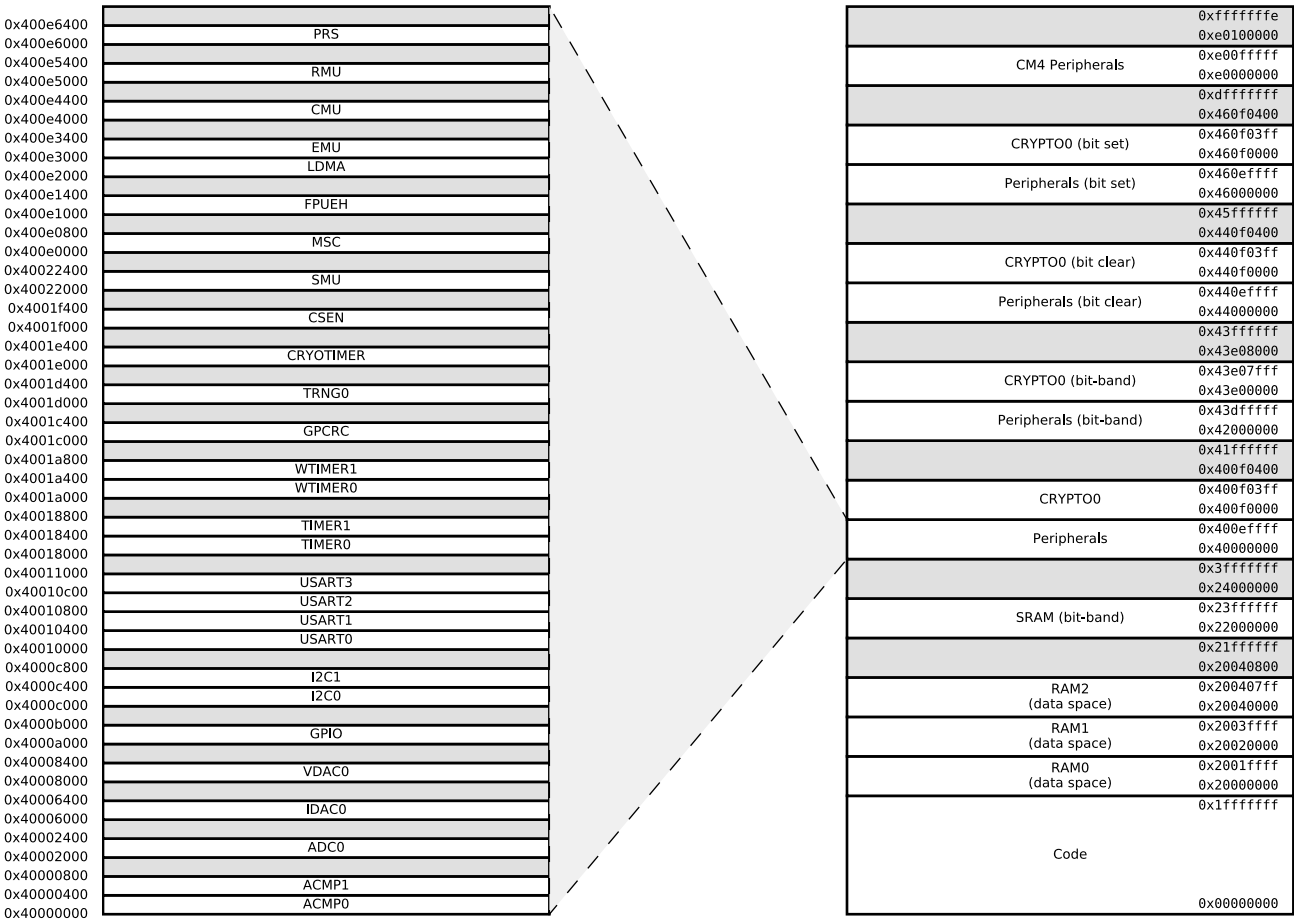

Figure 3.3. EFM32PG12 Memory Map — Peripherals

4.1.5.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V DC-DC output. T_{OP} = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C.

Table 4.6. Current Consumption 3.3 V using DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2].	I_{ACTIVE_DCM}	38.4 MHz crystal, CPU running while loop from flash[4]	—	86	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	70	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	70	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	85	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	77	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	636	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode[1].	I_{ACTIVE_CCM}	38.4 MHz crystal, CPU running while loop from flash[4]	—	96	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	81	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	82	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	95	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	95	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1155	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode[3].	I_{ACTIVE_LPM}	38.4 MHz crystal, CPU running while loop from flash[4]	—	80	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	64	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	64	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	79	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	66	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	224	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode[1].	$I_{ACTIVE\_CCM\_VS}$	19 MHz HFRCO, CPU running while loop from flash	—	101	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1128	—	µA/MHz

4.1.8.4 High-Freqency RC Oscillator (HFRCO)

Table 4.13. High-Freqency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	f_{HFRCO_ACC}	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
Start-up time	t_{HFRCO}	$f_{HFRCO} \geq 19$ MHz	—	300	—	ns
		$4 < f_{HFRCO} < 19$ MHz	—	1	—	µs
		$f_{HFRCO} \leq 4$ MHz	—	2.5	—	µs
Maximum DPLL lock time[1]	t_{DPLL_LOCK}	f_{REF} = 32.768 kHz, f_{HFRCO} = 39.98 MHz, N = 1219, M = 0	—	183	—	µs
Current consumption on all supplies	I_{HFRCO}	f_{HFRCO} = 38 MHz	—	244	TBD	µA
		f_{HFRCO} = 32 MHz	—	204	TBD	µA
		f_{HFRCO} = 26 MHz	—	173	TBD	µA
		f_{HFRCO} = 19 MHz	—	143	TBD	µA
		f_{HFRCO} = 16 MHz	—	123	TBD	µA
		f_{HFRCO} = 13 MHz	—	110	TBD	µA
		f_{HFRCO} = 7 MHz	—	85	TBD	µA
		f_{HFRCO} = 4 MHz	—	32	TBD	µA
		f_{HFRCO} = 2 MHz	—	31	TBD	µA
		f_{HFRCO} = 1 MHz	—	30	TBD	µA
		f_{HFRCO} = 40 MHz, DPLL enabled	—	385	TBD	µA
		f_{HFRCO} = 32 MHz, DPLL enabled	—	310	—	µA
		f_{HFRCO} = 16 MHz, DPLL enabled	—	203	—	µA
		f_{HFRCO} = 4 MHz, DPLL enabled	—	95	—	µA
		f_{HFRCO} = 1 MHz, DPLL enabled	—	79	—	µA
Coarse trim step size (% of period)	SS_{HFRCO_COARSE}		—	0.8	—	%
Fine trim step size (% of period)	SS_{HFRCO_FINE}		—	0.1	—	%
Period jitter	PJ_{HFRCO}		—	0.2	—	% RMS

Note:

1. Maximum DPLL lock time ~= 6 x (M+1) x t_{REF}, where t_{REF} is the reference clock period.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz	$SNDR_{DAC}$	500 ksps, single-ended, internal 1.25V reference	—	60.4	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	61.6	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	64.0	—	dB
		500 ksps, differential, internal 1.25V reference	—	63.3	—	dB
		500 ksps, differential, internal 2.5V reference	—	64.4	—	dB
		500 ksps, differential, 3.3V VDD reference	—	65.8	—	dB
Signal to noise and distortion ratio (1 kHz sine wave). Noise band limited to 22 kHz.	$SNDR_{DAC\_BAND}$	500 ksps, single-ended, internal 1.25V reference	—	65.3	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	66.7	—	dB
		500 ksps, differential, 3.3V VDD reference	—	68.5	—	dB
		500 ksps, differential, internal 1.25V reference	—	67.8	—	dB
		500 ksps, differential, internal 2.5V reference	—	69.0	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	70.0	—	dB
Total harmonic distortion	THD		—	70.2	—	dB
Differential non-linearity[3]	DNL_{DAC}		TBD	—	TBD	LSB
Intergral non-linearity	INL_{DAC}		TBD	—	TBD	LSB
Offset error[5]	V_{OFFSET}	T_J = 25 °C	TBD	—	TBD	mV
		-40 °C ≤ T_J ≤ 85 °C	TBD	—	TBD	mV
Gain error[5]	V_{GAIN}	T_J = 25 °C	TBD	—	TBD	%
		-40 °C ≤ T_J ≤ 85 °C	TBD	—	TBD	%
External load capactiance, OUTSCALE=0	C_{LOAD}		—	—	75	pF

Note:

1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
3. Entire range is monotonic and has no missing codes.
4. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
6. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Settling time, (output settled within 1% of steady state value),	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	µs
		Step value is changed	—	1	—	µs
Current consumption[2]	I_{IDAC}	EM0 or EM1 Source mode, excluding output current	—	8.9	TBD	µA
		EM0 or EM1 Sink mode, excluding output current	—	12	TBD	µA
		EM2 or EM3 Source mode, excluding output current, T = 25 °C	—	1.04	—	µA
		EM2 or EM3 Sink mode, excluding output current, T = 25 °C	—	1.08	—	µA
		EM2 or EM3 Source mode, excluding output current, T ≥ 85 °C	—	8.9	—	µA
		EM2 or EM3 Sink mode, excluding output current, T ≥ 85 °C	—	12	—	µA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mv)	—	0.11	—	%
		RANGESEL1=1, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mV)	—	0.06	—	%
		RANGESEL1=2, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-150 mV)	—	0.04	—	%
		RANGESEL1=3, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-250 mV)	—	0.03	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.12	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.05	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.04	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.03	—	%

Note:

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.20.2 I2C Fast-mode (Fm)[1]

Table 4.28. I2C Fast-mode (Fm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time[3]	t_{HD_DAT}		100	—	900	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		0.6	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:

1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

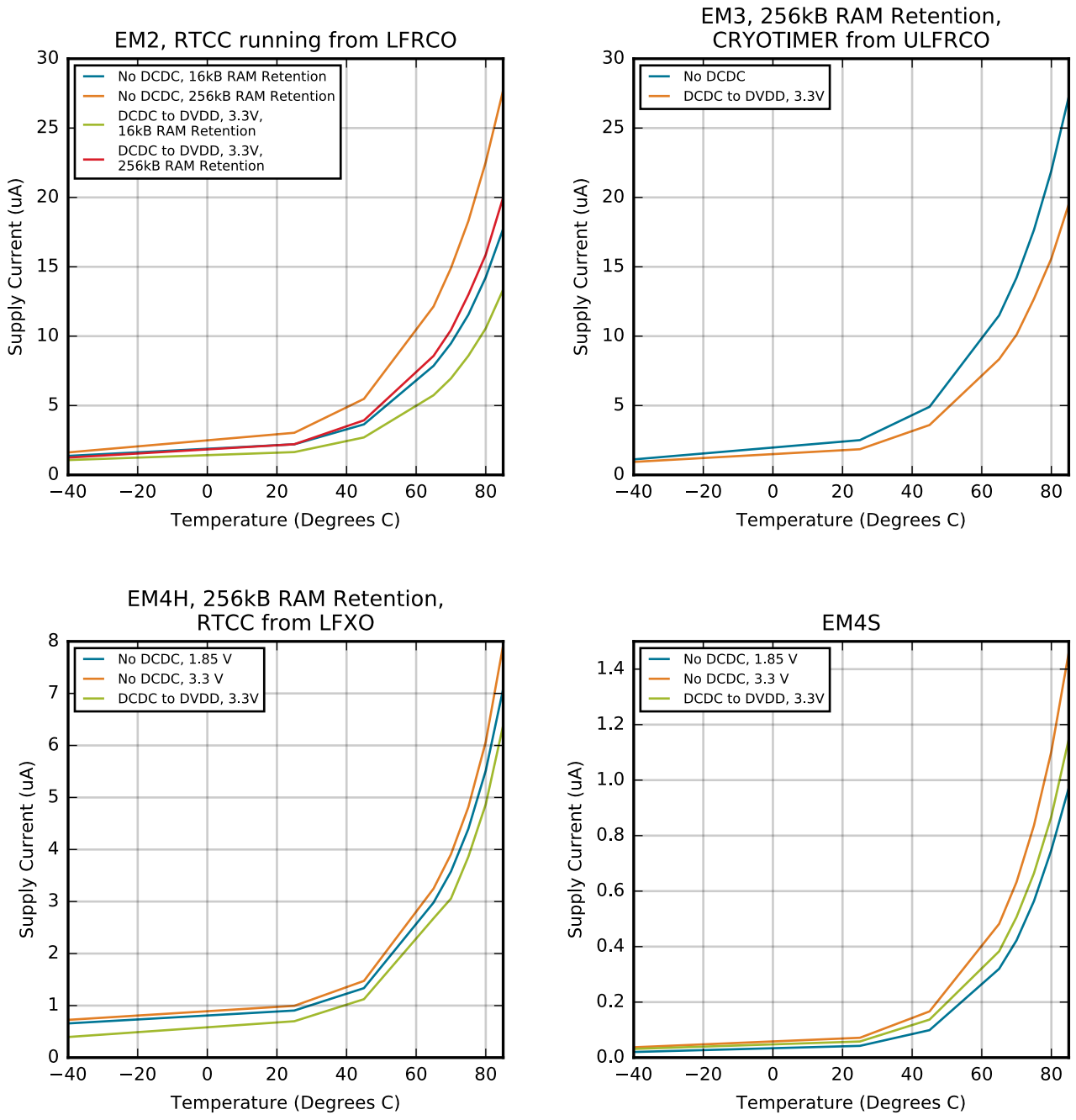

Figure 4.5. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Temperature

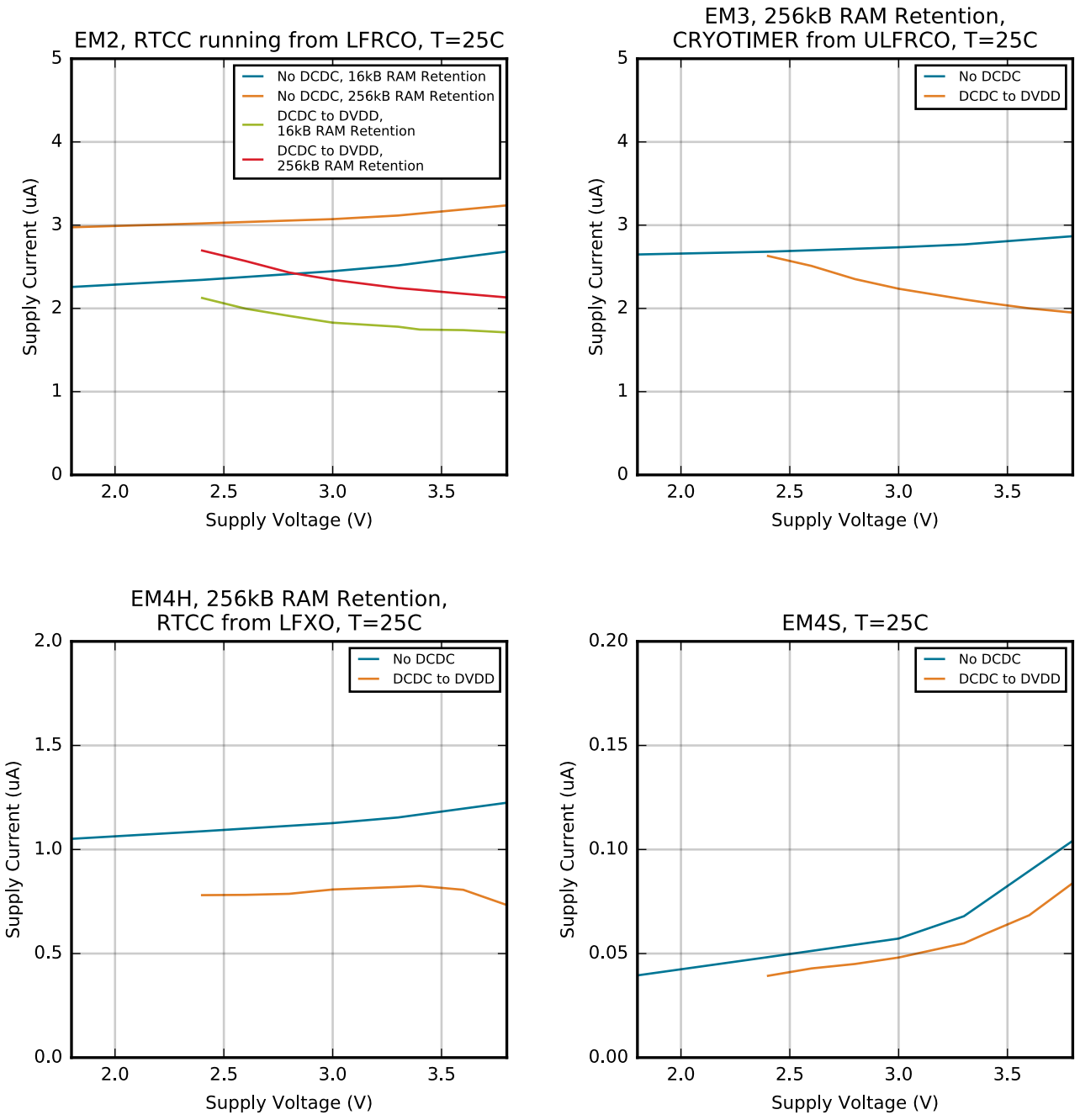

Figure 4.7. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Supply

Table 6.1. EFM32PG12B5xx in BGA125 Device Pinout

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
A1	PF3	BUSAY BUSBX	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 WTIM0_CDTI2 #31 WTIM1_CC0 #27 WTIM1_CC1 #25 WTIM1_CC2 #23 WTIM1_CC3 #21 LE-TIM0_OUT0 #27 LE-TIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 US2_TX #16 US2_RX #15 US2_CLK #14 US2_CS #13 US2_CTS #12 US2_RTS #11 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI
A2	PF1	BUSAY BUSBX	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 WTIM0_CDTI1 #31 WTIM0_CDTI2 #29 WTIM1_CC0 #25 WTIM1_CC1 #23 WTIM1_CC2 #21 WTIM1_CC3 #19 LE-TIM0_OUT0 #25 LE-TIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 US2_TX #15 US2_RX #14 US2_CLK #13 US2_CS #12 US2_CTS #11 US2_RTS #10 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS BOOT_RX
A3	PC5	BUSAY BUSBX	WTIM0_CC0 #25 WTIM0_CC1 #23 WTIM0_CC2 #21 WTIM0_CDTI0 #17 WTIM0_CDTI1 #15 WTIM0_CDTI2 #13 WTIM1_CC0 #9 WTIM1_CC1 #7 WTIM1_CC2 #5 WTIM1_CC3 #3 PCNT1_S0IN #18 PCNT1_S1IN #17 PCNT2_S0IN #18 PCNT2_S1IN #17	US3_TX #23 US3_RX #22 US3_CLK #21 US3_CS #20 US3_CTS #19 US3_RTS #18 I2C1_SDA #18 I2C1_SCL #17	

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
C1	PF11	BUSAY BUSBX	WTIM1_CC2 #31 WTIM1_CC3 #29 PCNT1_S0IN #24 PCNT1_S1IN #23 PCNT2_S0IN #24 PCNT2_S1IN #23	US2_TX #24 US2_RX #23 US2_CLK #22 US2_CS #21 US2_CTS #20 US2_RTS #19 US3_TX #24 US3_RX #23 US3_CLK #22 US3_CS #21 US3_CTS #20 US3_RTS #19 I2C1_SDA #24 I2C1_SCL #23	ETM_TD2 #0
C2	PF10	BUSBY BUSAX	WTIM1_CC2 #30 WTIM1_CC3 #28 PCNT1_S0IN #23 PCNT1_S1IN #22 PCNT2_S0IN #23 PCNT2_S1IN #22	US2_TX #23 US2_RX #22 US2_CLK #21 US2_CS #20 US2_CTS #19 US2_RTS #18 I2C1_SDA #23 I2C1_SCL #22	ETM_TD1 #0
C3	PF9	BUSAY BUSBX	WTIM1_CC1 #31 WTIM1_CC2 #29 WTIM1_CC3 #27 PCNT1_S0IN #22 PCNT1_S1IN #21 PCNT2_S0IN #22 PCNT2_S1IN #21	US2_TX #22 US2_RX #21 US2_CLK #20 US2_CS #19 US2_CTS #18 US2_RTS #17 I2C1_SDA #22 I2C1_SCL #21	ETM_TD0 #0
C5	PC2	BUSBY BUSAX	WTIM0_CC0 #22 WTIM0_CC1 #20 WTIM0_CC2 #18 WTIM0_CDTI0 #14 WTIM0_CDTI1 #12 WTIM0_CDTI2 #10 WTIM1_CC0 #6 WTIM1_CC1 #4 WTIM1_CC2 #2 WTIM1_CC3 #0 PCNT1_S0IN #15 PCNT1_S1IN #14 PCNT2_S0IN #15 PCNT2_S1IN #14	US3_TX #20 US3_RX #19 US3_CLK #18 US3_CS #17 US3_CTS #16 US3_RTS #15 I2C1_SDA #15 I2C1_SCL #14	
C6	PJ15	BUSACMP1Y BUSACMP1X	PCNT1_S0IN #12 PCNT1_S1IN #11 PCNT2_S0IN #12 PCNT2_S1IN #11	US3_TX #17 US3_RX #16 US3_CLK #15 US3_CS #14 US3_CTS #13 US3_RTS #12 I2C1_SDA #12 I2C1_SCL #11	LES_ALTEX3

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
C10	PB15	BUSCY BUSDX LFXTAL_P	TIM0_CC0 #10 TIM0_CC1 #9 TIM0_CC2 #8 TIM0_CDTI0 #7 TIM0_CDTI1 #6 TIM0_CDTI2 #5 TIM1_CC0 #10 TIM1_CC1 #9 TIM1_CC2 #8 TIM1_CC3 #7 WTIM0_CC0 #19 WTIM0_CC1 #17 WTIM0_CC2 #15 WTIM0_CDTI0 #11 WTIM0_CDTI1 #9 WTIM0_CDTI2 #7 WTIM1_CC0 #3 WTIM1_CC1 #1 LE-TIM0_OUT0 #10 LE-TIM0_OUT1 #9 PCNT0_S0IN #10 PCNT0_S1IN #9	US0_TX #10 US0_RX #9 US0_CLK #8 US0_CS #7 US0_CTS #6 US0_RTS #5 US1_TX #10 US1_RX #9 US1_CLK #8 US1_CS #7 US1_CTS #6 US1_RTS #5 LEU0_TX #10 LEU0_RX #9 I2C0_SDA #10 I2C0_SCL #9	CMU_CLK0 #1 PRS_CH6 #10 PRS_CH7 #9 PRS_CH8 #8 PRS_CH9 #7 ACMP0_O #10 ACMP1_O #10
C11	PB14	BUSDY BUSCX LFXTAL_N	TIM0_CC0 #9 TIM0_CC1 #8 TIM0_CC2 #7 TIM0_CDTI0 #6 TIM0_CDTI1 #5 TIM0_CDTI2 #4 TIM1_CC0 #9 TIM1_CC1 #8 TIM1_CC2 #7 TIM1_CC3 #6 WTIM0_CC0 #18 WTIM0_CC1 #16 WTIM0_CC2 #14 WTIM0_CDTI0 #10 WTIM0_CDTI1 #8 WTIM0_CDTI2 #6 WTIM1_CC0 #2 WTIM1_CC1 #0 LE-TIM0_OUT0 #9 LE-TIM0_OUT1 #8 PCNT0_S0IN #9 PCNT0_S1IN #8	US0_TX #9 US0_RX #8 US0_CLK #7 US0_CS #6 US0_CTS #5 US0_RTS #4 US1_TX #9 US1_RX #8 US1_CLK #7 US1_CS #6 US1_CTS #5 US1_RTS #4 LEU0_TX #9 LEU0_RX #8 I2C0_SDA #9 I2C0_SCL #8	CMU_CLK1 #1 PRS_CH6 #9 PRS_CH7 #8 PRS_CH8 #7 PRS_CH9 #6 ACMP0_O #9 ACMP1_O #9

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
D2	PF13	BUSAY BUSBX	WTIM1_CC3 #31 PCNT1_S0IN #26 PCNT1_S1IN #25 PCNT2_S0IN #26 PCNT2_S1IN #25	US2_TX #26 US2_RX #25 US2_CLK #24 US2_CS #23 US2_CTS #22 US2_RTS #21 US3_TX #26 US3_RX #25 US3_CLK #24 US3_CS #23 US3_CTS #22 US3_RTS #21 I2C1_SDA #26 I2C1_SCL #25	
D3	PF12	BUSBY BUSAX	WTIM1_CC3 #30 PCNT1_S0IN #25 PCNT1_S1IN #24 PCNT2_S0IN #25 PCNT2_S1IN #24	US2_TX #25 US2_RX #24 US2_CLK #23 US2_CS #22 US2_CTS #21 US2_RTS #20 US3_TX #25 US3_RX #24 US3_CLK #23 US3_CS #22 US3_CTS #21 US3_RTS #20 I2C1_SDA #25 I2C1_SCL #24	ETM_TD3 #0
D11	PB11	BUSCY BUSDX OPA2_P	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 WTIM0_CC0 #15 WTIM0_CC1 #13 WTIM0_CC2 #11 WTIM0_CDTI0 #7 WTIM0_CDTI1 #5 WTIM0_CDTI2 #3 LE-TIM0_OUT0 #6 LE-TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 US3_TX #15 US3_RX #14 US3_CLK #13 US3_CS #12 US3_CTS #11 US3_RTS #10 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6
D12	PB10	OPA2_OUTALT #1 BUSDY BUSCX	WTIM0_CC0 #14 WTIM0_CC1 #12 WTIM0_CC2 #10 WTIM0_CDTI0 #6 WTIM0_CDTI1 #4 WTIM0_CDTI2 #2 PCNT1_S0IN #10 PCNT1_S1IN #9 PCNT2_S0IN #10 PCNT2_S1IN #9	US2_TX #13 US2_RX #12 US2_CLK #11 US2_CS #10 US2_CTS #9 US2_RTS #8 US3_TX #14 US3_RX #13 US3_CLK #12 US3_CS #11 US3_CTS #10 US3_RTS #9 I2C1_SDA #10 I2C1_SCL #9	

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
D13	PB9	OPA2_OUTALT #0 BUSCY BUSDX	WTIM0_CC0 #13 WTIM0_CC1 #11 WTIM0_CC2 #9 WTIM0_CDTI0 #5 WTIM0_CDTI1 #3 WTIM0_CDTI2 #1 PCNT1_S0IN #9 PCNT1_S1IN #8 PCNT2_S0IN #9 PCNT2_S1IN #8	US2_TX #12 US2_RX #11 US2_CLK #10 US2_CS #9 US2_CTS #8 US2_RTS #7 US3_TX #13 US3_RX #12 US3_CLK #11 US3_CS #10 US3_CTS #9 US3_RTS #8 I2C1_SDA #9 I2C1_SCL #8	
E1	PK1		PCNT1_S0IN #30 PCNT1_S1IN #29 PCNT2_S0IN #30 PCNT2_S1IN #29	US2_TX #30 US2_RX #29 US2_CLK #28 US2_CS #27 US2_CTS #26 US2_RTS #25 US3_TX #30 US3_RX #29 US3_CLK #28 US3_CS #27 US3_CTS #26 US3_RTS #25 I2C1_SDA #30 I2C1_SCL #29	
E2	PK0	IDAC0_OUT	PCNT1_S0IN #29 PCNT1_S1IN #28 PCNT2_S0IN #29 PCNT2_S1IN #28	US2_TX #29 US2_RX #28 US2_CLK #27 US2_CS #26 US2_CTS #25 US2_RTS #24 US3_TX #29 US3_RX #28 US3_CLK #27 US3_CS #26 US3_CTS #25 US3_RTS #24 I2C1_SDA #29 I2C1_SCL #28	
E3	PF15	BUSAY BUSBX	PCNT1_S0IN #28 PCNT1_S1IN #27 PCNT2_S0IN #28 PCNT2_S1IN #27	US2_TX #28 US2_RX #27 US2_CLK #26 US2_CS #25 US2_CTS #24 US2_RTS #23 US3_TX #28 US3_RX #27 US3_CLK #26 US3_CS #25 US3_CTS #24 US3_RTS #23 I2C1_SDA #28 I2C1_SCL #27	
E5	VSS	Ground			
E6	VSS	Ground			
E7	VSS	Ground			
E8	VSS	Ground			
E9	VSS	Ground			
E12	PB8	BUSDY BUSCX	WTIM0_CC0 #12 WTIM0_CC1 #10 WTIM0_CC2 #8 WTIM0_CDTI0 #4 WTIM0_CDTI1 #2 WTIM0_CDTI2 #0 PCNT1_S0IN #8 PCNT1_S1IN #7 PCNT2_S0IN #8 PCNT2_S1IN #7	US2_TX #11 US2_RX #10 US2_CLK #9 US2_CS #8 US2_CTS #7 US2_RTS #6 US3_TX #12 US3_RX #11 US3_CLK #10 US3_CS #9 US3_CTS #8 US3_RTS #7 I2C1_SDA #8 I2C1_SCL #7	ETM_TD3 #2

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
G13	PI0	BUSADC0Y BUSADC0X		US2_TX #5 US2_RX #4 US2_CLK #3 US2_CS #2 US2_CTS #1 US2_RTS #0	LES_ALTEX4
H1	PF7	BUSAY BUSBX	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 WTIM1_CC0 #31 WTIM1_CC1 #29 WTIM1_CC2 #27 WTIM1_CC3 #25 LE-TIM0_OUT0 #31 LE-TIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30 PCNT1_S0IN #20 PCNT1_S1IN #19	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 US2_TX #20 US2_RX #19 US2_CLK #18 US2_CS #17 US2_CTS #16 US2_RTS #15 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	CMU_CLKI0 #1 CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1
H2	PF6	BUSBY BUSAX	TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDTI0 #27 TIM0_CDTI1 #26 TIM0_CDTI2 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 WTIM1_CC0 #30 WTIM1_CC1 #28 WTIM1_CC2 #26 WTIM1_CC3 #24 LE-TIM0_OUT0 #30 LE-TIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29 PCNT1_S0IN #19 PCNT1_S1IN #18	US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 US2_TX #19 US2_RX #18 US2_CLK #17 US2_CS #16 US2_CTS #15 US2_RTS #14 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29	CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30
H5	VSS	Ground			
H6	VSS	Ground			
H7	VSS	Ground			
H8	VSS	Ground			
H9	VSS	Ground			

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
M11	PD13	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSCY BUSDX OPA1_P	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 WTIM0_CDTI0 #29 WTIM0_CDTI1 #27 WTIM0_CDTI2 #25 WTIM1_CC0 #21 WTIM1_CC1 #19 WTIM1_CC2 #17 WTIM1_CC3 #15 LE-TIM0_OUT0 #21 LE-TIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 US3_TX #5 US3_RX #4 US3_CLK #3 US3_CS #2 US3_CTS #1 US3_RTS #0 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21 LES_CH5
M12	IOVDD	Digital IO power supply .			
M13	PA0	BUSDY BUSCX ADC0_EXTN	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 WTIM0_CC0 #0 LE-TIM0_OUT0 #0 LE-TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0 LES_CH8
N1	NC	No Connect.			
N2	NC	No Connect.			
N3	NC	No Connect.			
N4	NC	No Connect.			
N5	VSS	Ground			
N6	NC	No Connect.			
N7	NC	No Connect.			
N8	NC	No Connect.			

6.1.1 EFM32PG12B5xx in BGA125 GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters (A, B, C...), with individual pins on each port indicated by a number from 15 down to 0.

Table 6.2. EFM32PG12B5xx in BGA125 GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	PA9 (5V)	PA8 (5V)	PA7 (5V)	PA6 (5V)	PA5 (5V)	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10 (5V)	PB9 (5V)	PB8 (5V)	PB7 (5V)	PB6 (5V)	-	-	-	-	-	-
Port C	-	-	-	-	PC11 (5V)	PC10 (5V)	PC9 (5V)	PC8 (5V)	PC7 (5V)	PC6 (5V)	PC5 (5V)	PC4 (5V)	PC3 (5V)	PC2 (5V)	PC1 (5V)	PC0 (5V)
Port D	PD15	PD14	PD13	PD12 (5V)	PD11 (5V)	PD10 (5V)	PD9 (5V)	PD8 (5V)	-	-	-	-	-	-	-	-
Port F	PF15 (5V)	PF14 (5V)	PF13 (5V)	PF12 (5V)	PF11 (5V)	PF10 (5V)	PF9 (5V)	PF8 (5V)	PF7 (5V)	PF6 (5V)	PF5 (5V)	PF4 (5V)	PF3 (5V)	PF2 (5V)	PF1 (5V)	PF0 (5V)
Port I	-	-	-	-	-	-	-	-	-	-	-	-	PI3 (5V)	PI2 (5V)	PI1 (5V)	PI0 (5V)
Port J	PJ15 (5V)	PJ14 (5V)	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port K	-	-	-	-	-	-	-	-	-	-	-	-	-	PK2 (5V)	PK1 (5V)	PK0

Note:
1. GPIO with 5V tolerance are indicated by (5V).

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
29	PA4	VDAC0_OUT1ALT / OPA1_OUTALT #2 BUSDY BUSCX OPA0_N	TIM0_CC0 #4 TIM0_CC1 #3 TIM0_CC2 #2 TIM0_CDTI0 #1 TIM0_CDTI1 #0 TIM0_CDTI2 #31 TIM1_CC0 #4 TIM1_CC1 #3 TIM1_CC2 #2 TIM1_CC3 #1 WTIM0_CC0 #4 WTIM0_CC1 #2 WTIM0_CC2 #0 LE-TIM0_OUT0 #4 LE-TIM0_OUT1 #3 PCNT0_S0IN #4 PCNT0_S1IN #3	US0_TX #4 US0_RX #3 US0_CLK #2 US0_CS #1 US0_CTS #0 US0_RTS #31 US1_TX #4 US1_RX #3 US1_CLK #2 US1_CS #1 US1_CTS #0 US1_RTS #31 LEU0_TX #4 LEU0_RX #3 I2C0_SDA #4 I2C0_SCL #3	PRS_CH6 #4 PRS_CH7 #3 PRS_CH8 #2 PRS_CH9 #1 ACMP0_O #4 ACMP1_O #4 LES_CH12
30	PA5	VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSCY BUSDX	TIM0_CC0 #5 TIM0_CC1 #4 TIM0_CC2 #3 TIM0_CDTI0 #2 TIM0_CDTI1 #1 TIM0_CDTI2 #0 TIM1_CC0 #5 TIM1_CC1 #4 TIM1_CC2 #3 TIM1_CC3 #2 WTIM0_CC0 #5 WTIM0_CC1 #3 WTIM0_CC2 #1 LE-TIM0_OUT0 #5 LE-TIM0_OUT1 #4 PCNT0_S0IN #5 PCNT0_S1IN #4	US0_TX #5 US0_RX #4 US0_CLK #3 US0_CS #2 US0_CTS #1 US0_RTS #0 US1_TX #5 US1_RX #4 US1_CLK #3 US1_CS #2 US1_CTS #1 US1_RTS #0 US2_TX #0 US2_RX #31 US2_CLK #30 US2_CS #29 US2_CTS #28 US2_RTS #27 LEU0_TX #5 LEU0_RX #4 I2C0_SDA #5 I2C0_SCL #4	CMU_CLKI0 #4 PRS_CH6 #5 PRS_CH7 #4 PRS_CH8 #3 PRS_CH9 #2 ACMP0_O #5 ACMP1_O #5 LES_CH13 ETM_TCLK #1
31	PB11	BUSCY BUSDX OPA2_P	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 WTIM0_CC0 #15 WTIM0_CC1 #13 WTIM0_CC2 #11 WTIM0_CDTI0 #7 WTIM0_CDTI1 #5 WTIM0_CDTI2 #3 LE-TIM0_OUT0 #6 LE-TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 US3_TX #15 US3_RX #14 US3_CLK #13 US3_CS #12 US3_CTS #11 US3_RTS #10 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
32	PB12	BUSDY BUSCX OPA2_OUT	TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 WTIM0_CC0 #16 WTIM0_CC1 #14 WTIM0_CC2 #12 WTIM0_CDTI0 #8 WTIM0_CDTI1 #6 WTIM0_CDTI2 #4 WTIM1_CC0 #0 LE-TIM0_OUT0 #7 LE-TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6	US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6	PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7
33	PB13	BUSCY BUSDX OPA2_N	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 WTIM0_CC0 #17 WTIM0_CC1 #15 WTIM0_CC2 #13 WTIM0_CDTI0 #9 WTIM0_CDTI1 #7 WTIM0_CDTI2 #5 WTIM1_CC0 #1 LE-TIM0_OUT0 #8 LE-TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	CMU_CLKI0 #0 PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9
34	AVDD	Analog power supply .			

PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

Table 6.6. ACMP0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSACMP0X																															PA9	PA8
APORT0Y	BUSACMP0Y																															PA9	PA8
APORT1X	BUSAX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10		PC8		PC6		PC4		PC2		PC0
APORT1Y	BUSAY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT2X	BUSBX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT2Y	BUSBY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10		PC8		PC6		PC4		PC2		PC0
APORT3X	BUSCX		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PA0		PD14		PD12		PD10		PD8
APORT3Y	BUSCY	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PA0		PD14		PD12		PD10		PD8

Table 6.7. ACMP1 Bus and Pin Mapping

Port	APORT0X	APORT0Y	APORT1X	APORT1Y	APORT2X	APORT2Y	APORT3X	APORT3Y	APORT4X	APORT4Y
Bus	BUSACMP1X	BUSACMP1Y	BUSAX	BUSAY	BUSBX	BUSBY	BUSCX	BUSCY	BUSDX	BUSDY
CH31				PF15	PF15			PB15	PB15	
CH30			PF14			PF14	PB14			PB14
CH29				PF13	PF13			PB13	PB13	
CH28			PF12			PF12	PB12			PB12
CH27				PF11	PF11			PB11	PB11	
CH26			PF10			PF10	PB10			PB10
CH25				PF9	PF9			PB9	PB9	
CH24			PF8			PF8	PB8			PB8
CH23				PF7	PF7			PB7	PB7	
CH22			PF6			PF6	PB6			PB6
CH21				PF5	PF5					
CH20			PF4			PF4				
CH19				PF3	PF3					
CH18			PF2			PF2				
CH17				PF1	PF1					
CH16			PF0			PF0				
CH15								PA7	PA7	
CH14							PA6			PA6
CH13								PA5	PA5	
CH12							PA4			PA4
CH11				PC11	PC11			PA3	PA3	
CH10			PC10			PC10	PA2			PA2
CH9				PC9	PC9			PA1	PA1	
CH8			PC8			PC8	PA0			PA0
CH7	PJ15	PJ15		PC7	PC7			PD15	PD15	
CH6	PJ14	PJ14	PC6			PC6	PD14			PD14
CH5				PC5	PC5			PD13	PD13	
CH4			PC4			PC4	PD12			PD12
CH3				PC3	PC3			PD11	PD11	
CH2			PC2			PC2	PD10			PD10
CH1				PC1	PC1			PD9	PD9	
CH0			PC0			PC0	PD8			PD8