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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	36MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f101rft6

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2.3.17 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock/calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.18 Timers and watchdogs

The XL-density STM32F101xx access line devices include up to ten general-purpose timers, two basic timers, two watchdog timers and a SysTick timer.

Table 4: STM32F101xF and STM32F101xG timer feature comparison compares the features of the general-purpose and basic timers.

Table 4. STM32F101xF and STM32F101xG timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9, TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No
TIM10, TIM11, TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

General-purpose timers (TIMx)

There are 10 synchronizable general-purpose timers embedded in the STM32F101xF and STM32F101xG XL-density access line devices (see [Table 4](#) for differences).

- **TIM2, TIM3, TIM4, TIM5**

There are up to 4 synchronizable general-purpose timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F101xF and STM32F101xG access line devices.

These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

2.3.24 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Seven DAC trigger inputs are used in the STM32F101xF and STM32F101xG access line family. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

2.3.25 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between $2\text{ V} < V_{DDA} < 3.6\text{ V}$. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.3.26 Serial wire JTAG debug port (SWJ-DP)

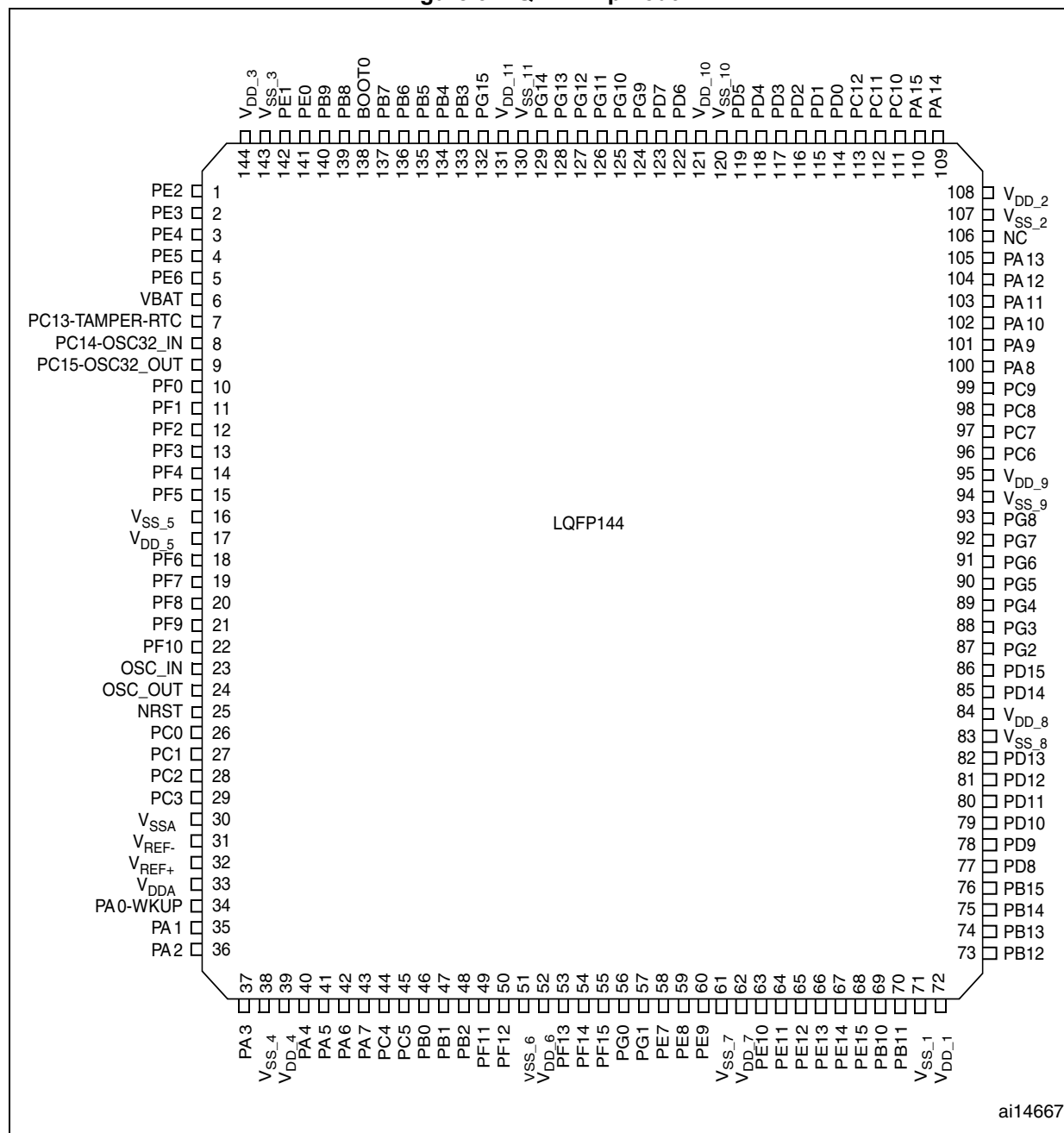
The ARM® SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.3.27 Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F10xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

3 Pinouts and pin descriptions

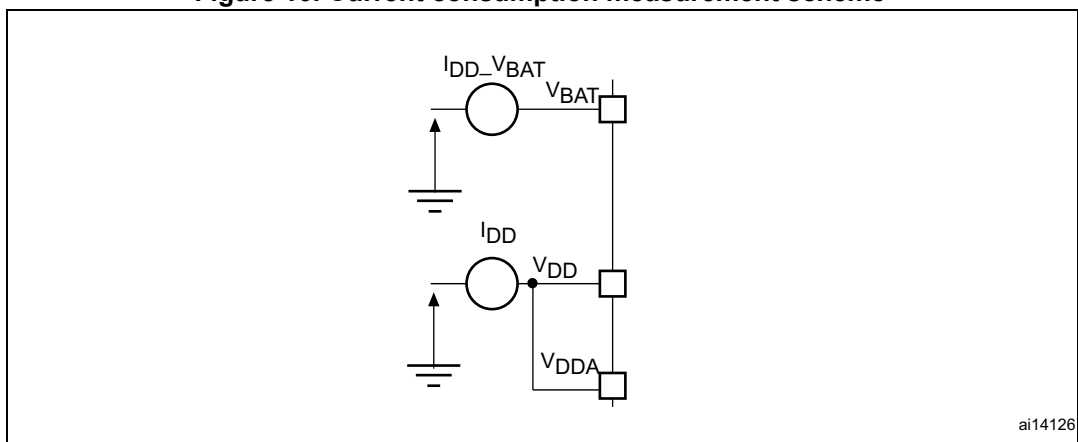
Figure 3. LQFP144 pinout



1. The above figure shows the package top view.

5.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 7: Voltage characteristics](#), [Table 8: Current characteristics](#), and [Table 9: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD}) ⁽¹⁾	-0.3	4.0	V
$V_{IN}^{(2)}$	Input voltage on five volt tolerant pin	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
$ \Delta V_{DDx} $	Variations between different V_{DD} power pins	-	50	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins including V_{REF-}	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 5.3.12: Absolute maximum ratings (electrical sensitivity)		-

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to [Table 8: Current characteristics](#) for the maximum allowed injected current values.

5.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 12](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 10](#).

Table 12. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}^{(2)}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8 ⁽¹⁾	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}^{(2)}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}^{(2)}$	Reset temporization	-	1.5	2.5	3.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

2. Guaranteed by design.

Table 20. Peripheral current consumption⁽¹⁾

Peripherals		μA/MHz
AHB (up to 36MHz)	DMA1	23.06
	DMA2	18.47
	FSMC	55.14
	CRC	2.08
	BusMatrix ⁽²⁾	11.67
APB1 (up to 18 MHz)	APB1-Bridge	8.61
	TIM2	37.22
	TIM3	36.39
	TIM4	35.56
	TIM5	33.61
	TIM6	7.78
	TIM7	7.78
	TIM12	19.17
	TIM13	12.22
	TIM14	13.33
	SPI2/I2S2 ⁽³⁾	8.33
	SPI3/I2S3 ⁽³⁾	8.33
	USART2	12.22
	USART3	12.22
	UART4	12.22
	UART5	12.22
	I2C1	10.28
	I2C2	10.28
	DAC ⁽⁴⁾	9.17
	WWDG	3.06
	PWR	2.50
	BKP	2.78
	IWDG	4.44

Synchronous waveforms and timings

Figure 23 through Figure 26 represent synchronous waveforms and Table 36 through Table 38 provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F10xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Figure 23. Synchronous multiplexed NOR/PSRAM read timings

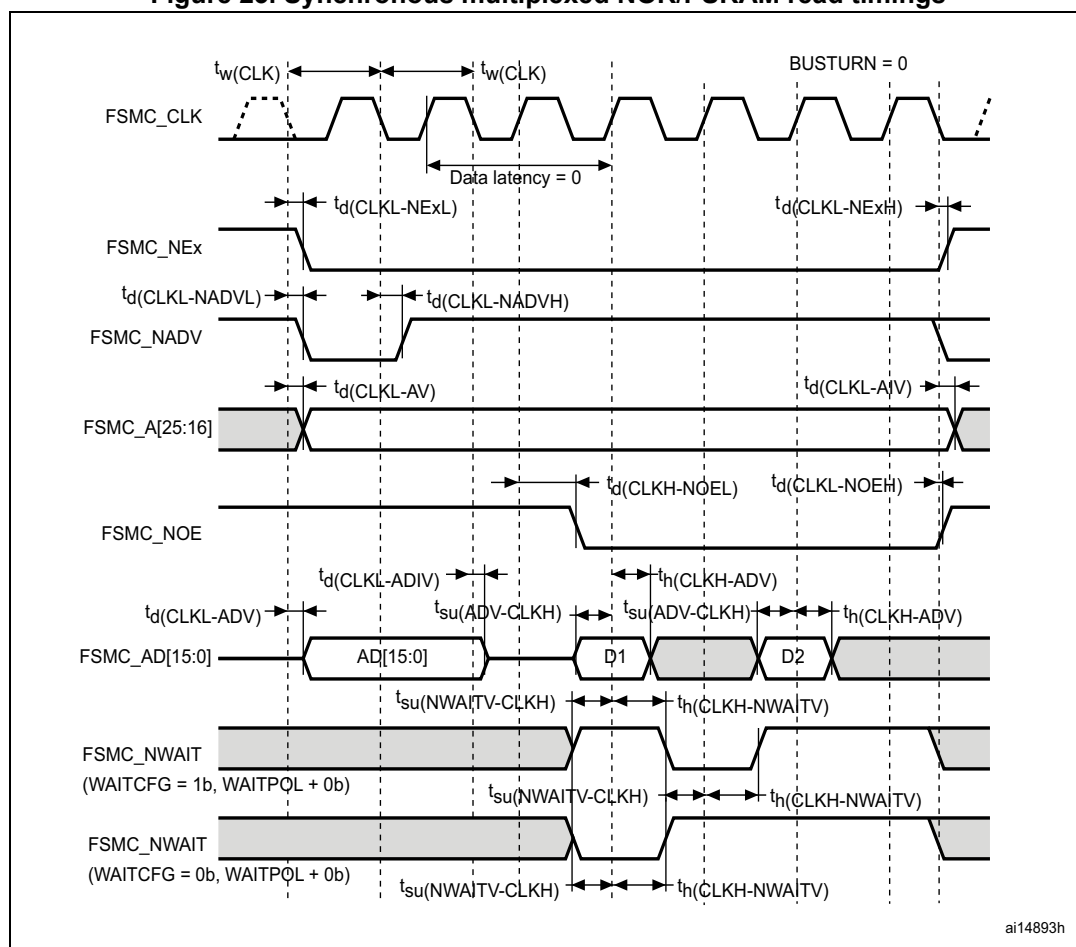


Figure 24. Synchronous multiplexed PSRAM write timings

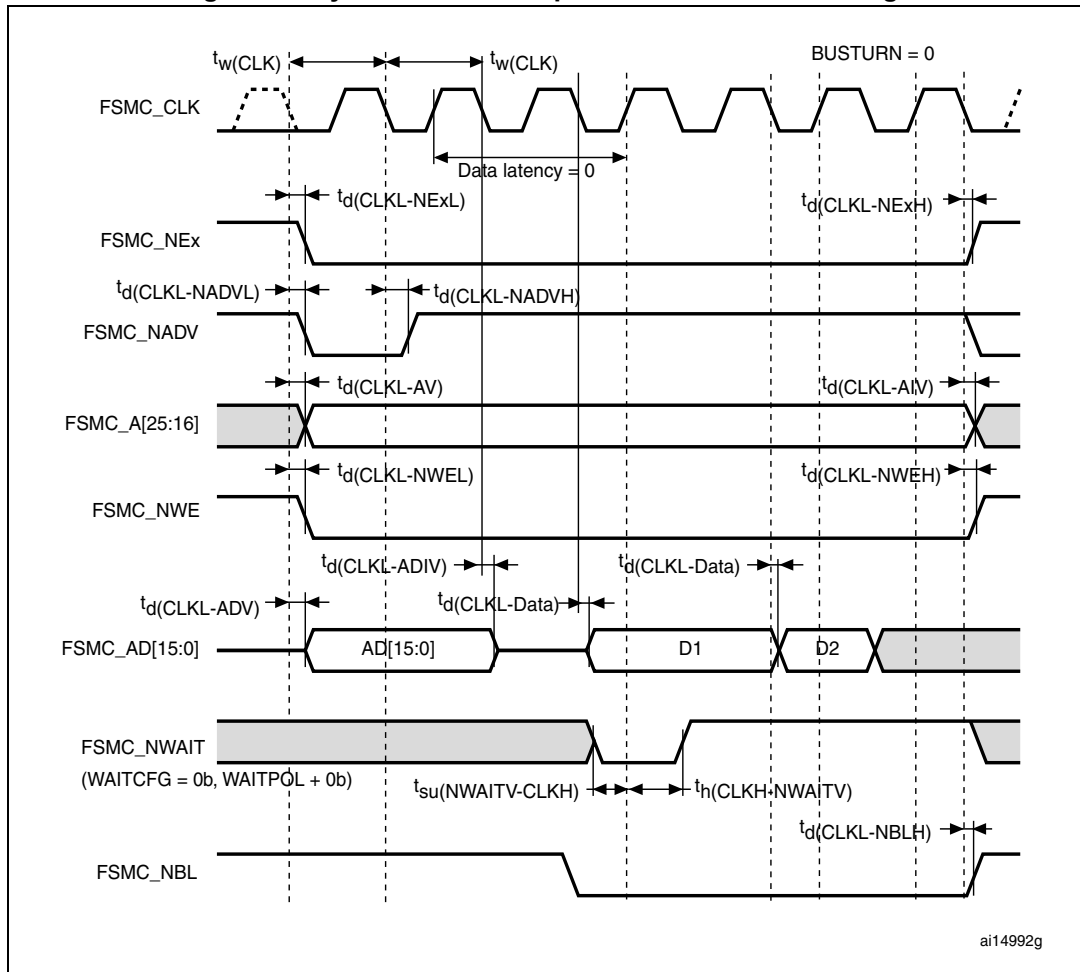
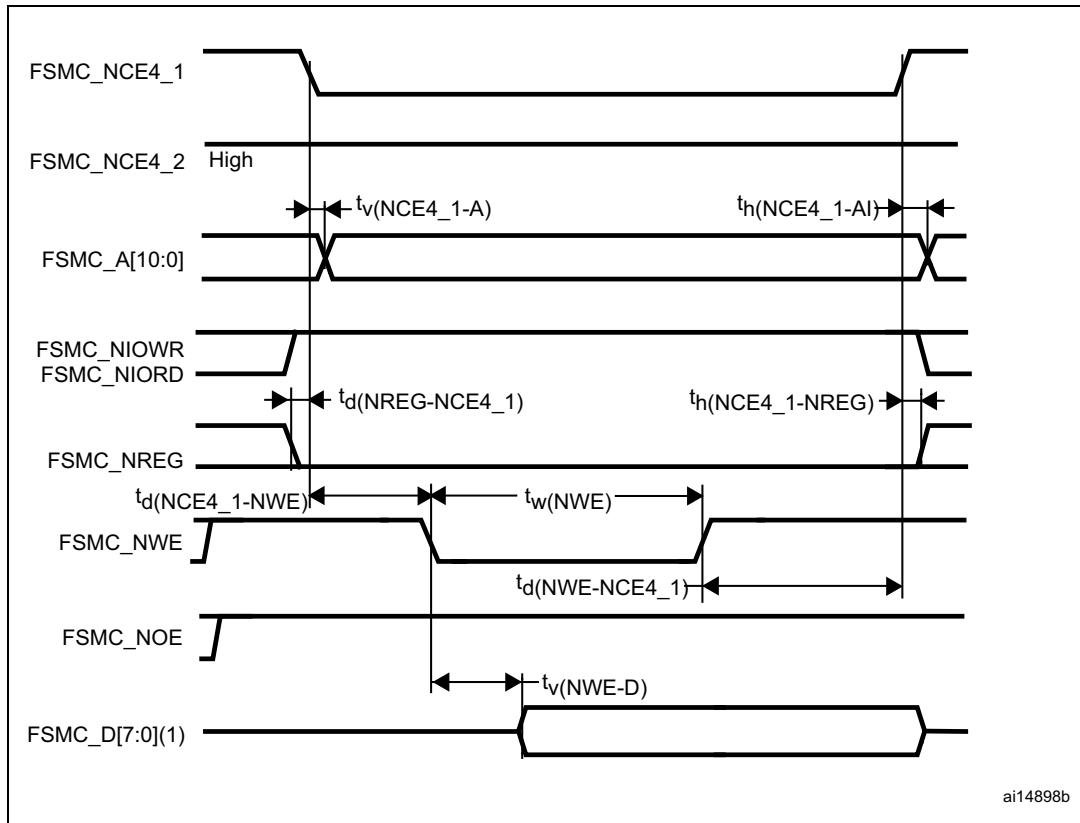
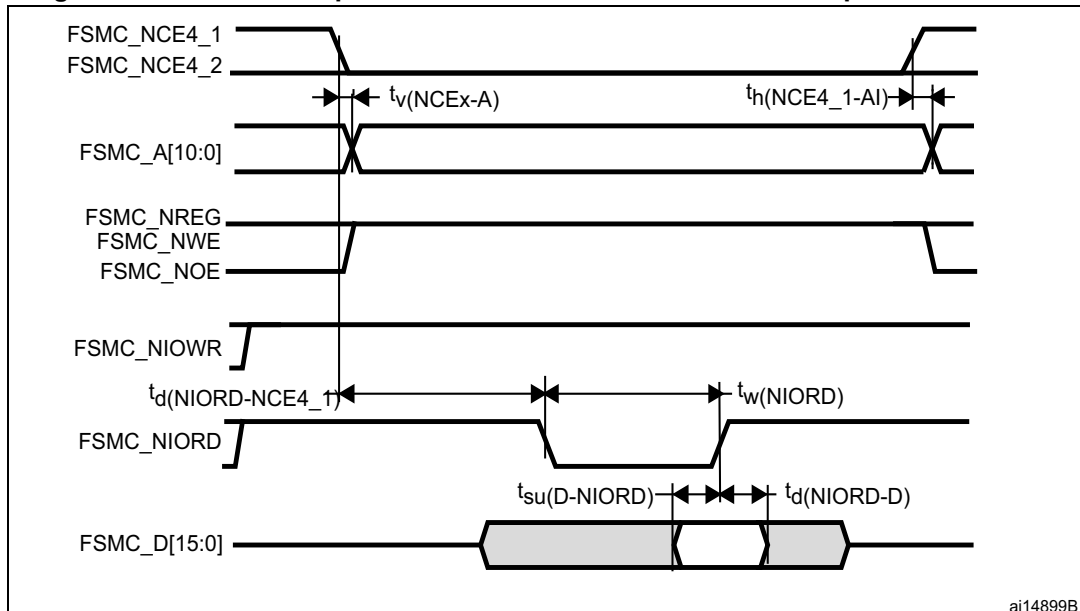


Figure 30. PC Card/CompactFlash controller waveforms for attribute memory write access

1. Only data bits 0...7 are driven (bits 8...15 remains HiZ).

Figure 31. PC Card/CompactFlash controller waveforms for I/O space read access

5.3.17 Communications interfaces

I²C interface characteristics

The STM32F101xF and STM32F101xG access line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

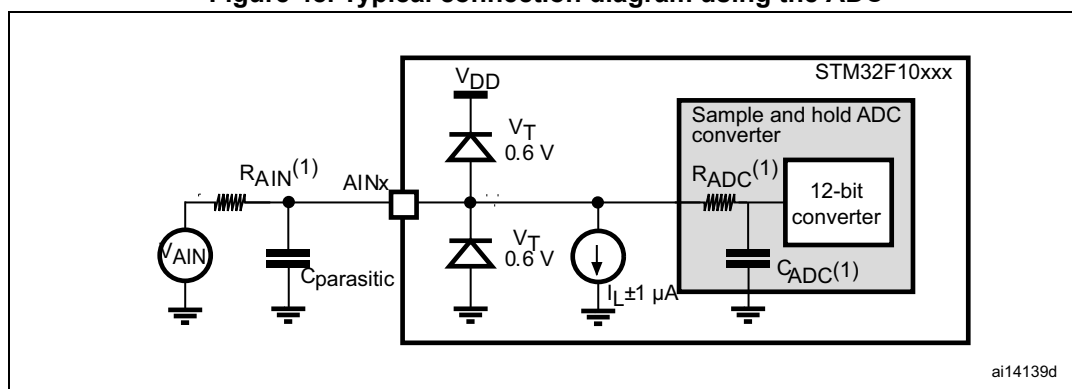
The I²C characteristics are described in [Table 52](#). Refer also to [Section 5.3.13: I/O current injection characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

Table 52. I²C characteristics

Symbol	Parameter	Standard mode I ² C ⁽¹⁾⁽²⁾		Fast mode I ² C ⁽¹⁾⁽²⁾		Unit
		Min	Max	Min	Max	
t _w (SCLL)	SCL clock low time	4.7	-	1.3	-	μs
t _w (SCLH)	SCL clock high time	4.0	-	0.6	-	
t _{su} (SDA)	SDA setup time	250	-	100	-	ns
t _h (SDA)	SDA data hold time	-	3450 ⁽³⁾	-	900 ⁽³⁾	
t _r (SDA) t _r (SCL)	SDA and SCL rise time	-	1000	-	300	
t _f (SDA) t _f (SCL)	SDA and SCL fall time	-	300	-	300	
t _h (STA)	Start condition hold time	4.0	-	0.6	-	μs
t _{su} (STA)	Repeated Start condition setup time	4.7	-	0.6	-	
t _{su} (STO)	Stop condition setup time	4.0	-	0.6	-	μs
t _w (STO:STA)	Stop to Start condition time (bus free)	4.7	-	1.3	-	μs
C _b	Capacitive load for each bus line	-	400	-	400	pF
t _{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	0	50 ⁽⁴⁾	0	50 ⁽⁴⁾	μs

1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve the fast mode I²C frequencies and it must be a multiple of 10 MHz in order to reach the I²C fast mode maximum clock speed of 400 kHz.
3. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. The minimum width of the spikes filtered by the analog filter is above t_{SP}(max).

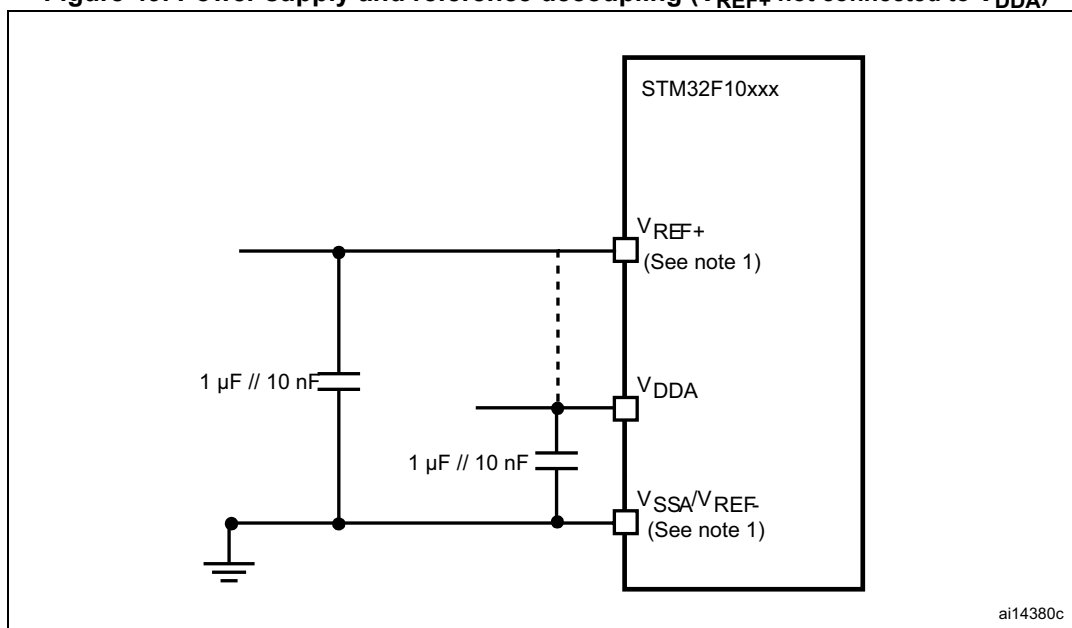
Figure 48. Typical connection diagram using the ADC



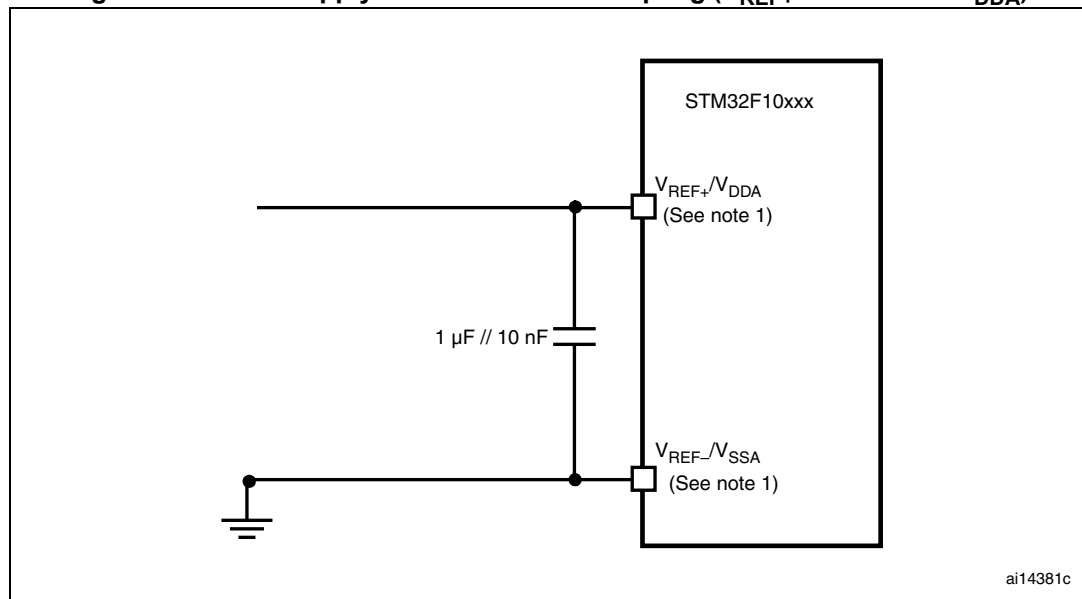
1. Refer to [Table 56](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 49](#) or [Figure 50](#), depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Figure 49. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})

1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Figure 50. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.19 DAC electrical specifications

Table 60. DAC characteristics

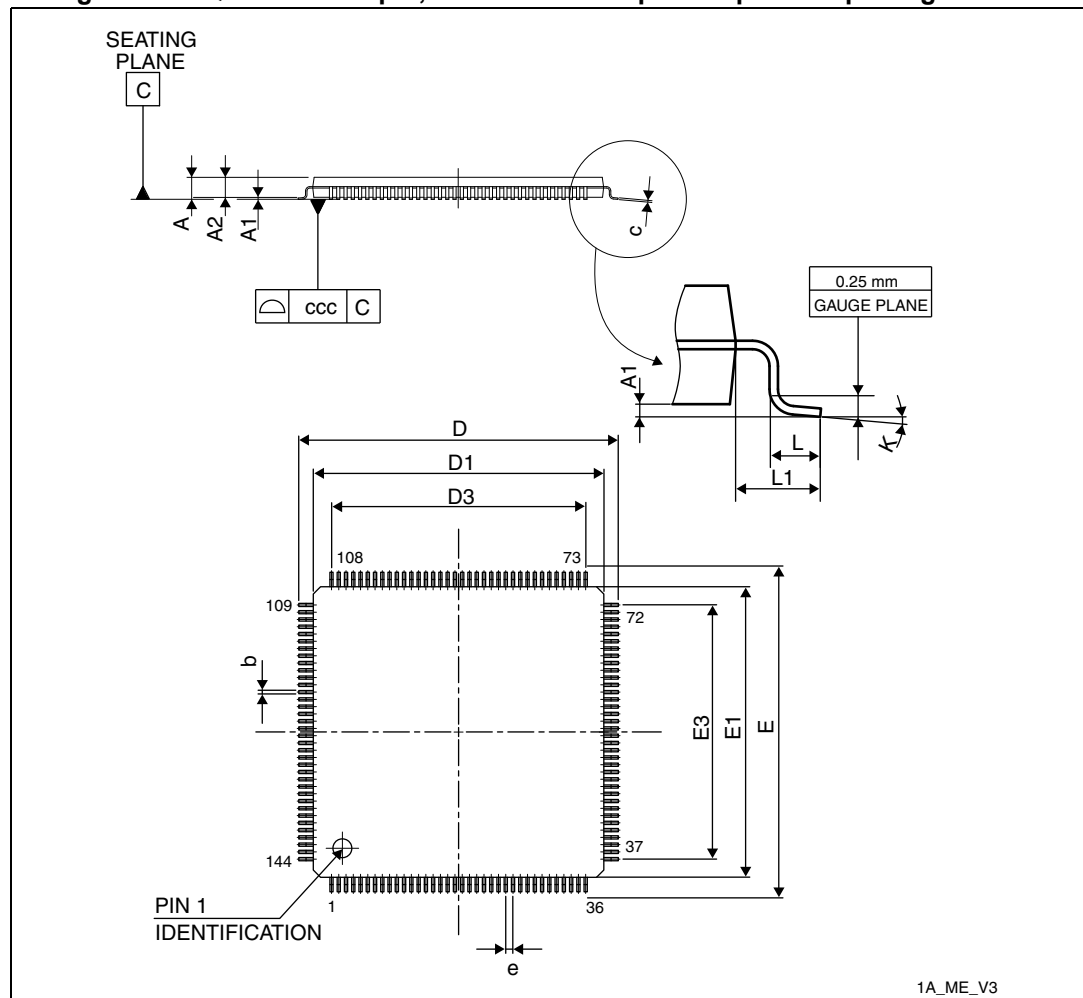
Symbol	Parameter	Conditions		Min	Typ	Max ⁽¹⁾	Unit	Comments
V_{DDA}	Analog supply voltage			2.4	-	3.6	V	-
V_{REF+}	Reference supply voltage			2.4	-	3.6	V	V_{REF+} must always be below V_{DDA}
V_{SSA}	Ground			0	-	0	V	-
$R_{LOAD}^{(2)}$	Resistive load with buffer ON	DAC output buffer ON	R_{LOAD} connected to V_{SSA}	5	-	-	k Ω	-
			R_{LOAD} connected to V_{DDA}	25	-	-		-
$R_O^{(2)}$	Impedance output with buffer OFF			-	-	15	k Ω	When the buffer is OFF, the minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 M Ω
$C_{LOAD}^{(2)}$	Capacitive load			-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

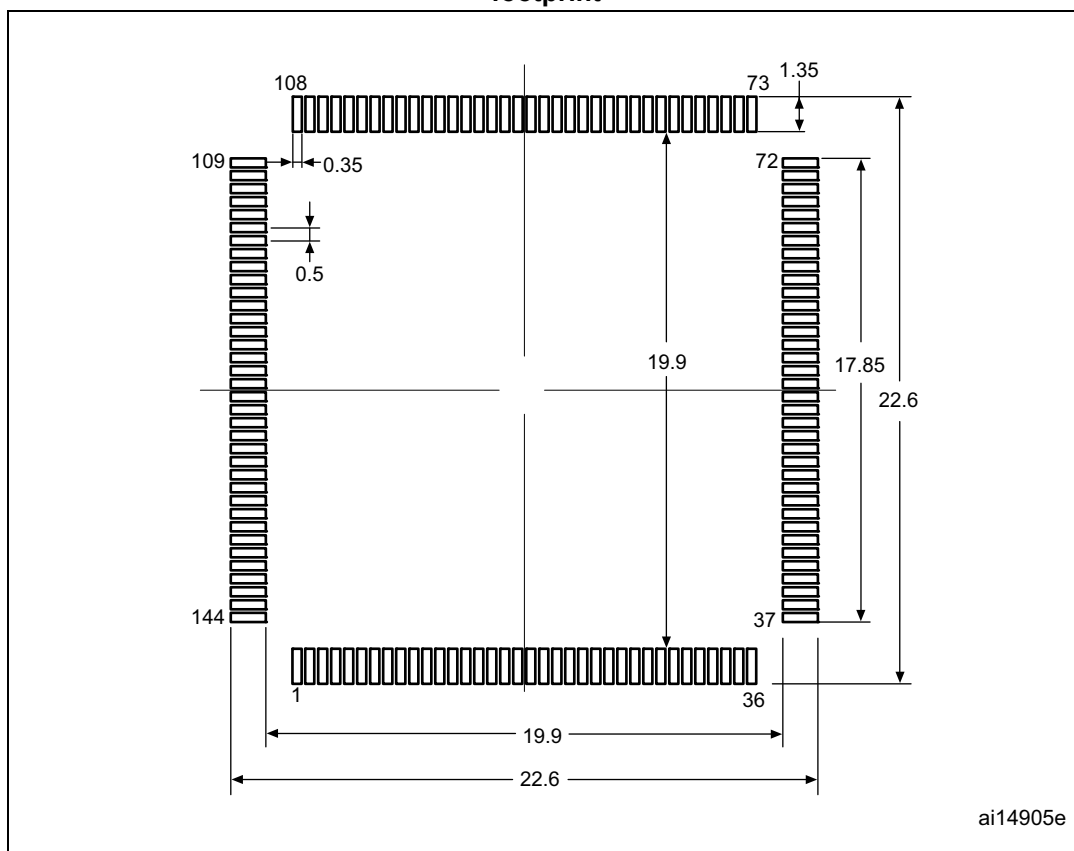
6.1 LQFP144 package information

Figure 52. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.

Figure 53. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package footprint



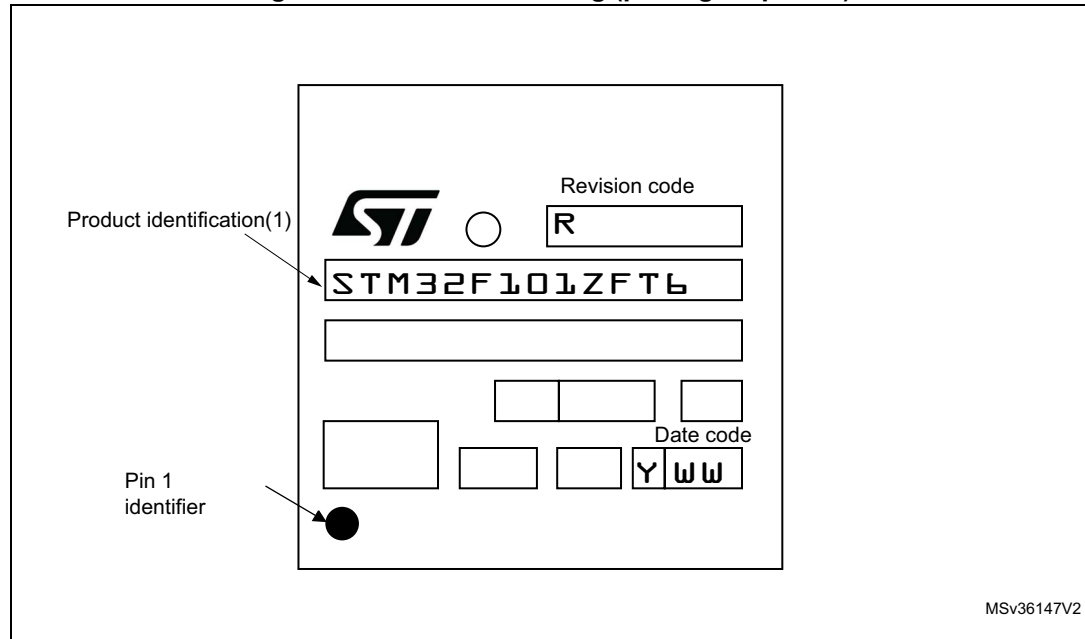
1. Dimensions are expressed in millimeters.

Device marking for LQFP144

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 54. LQFP144 marking (package top view)



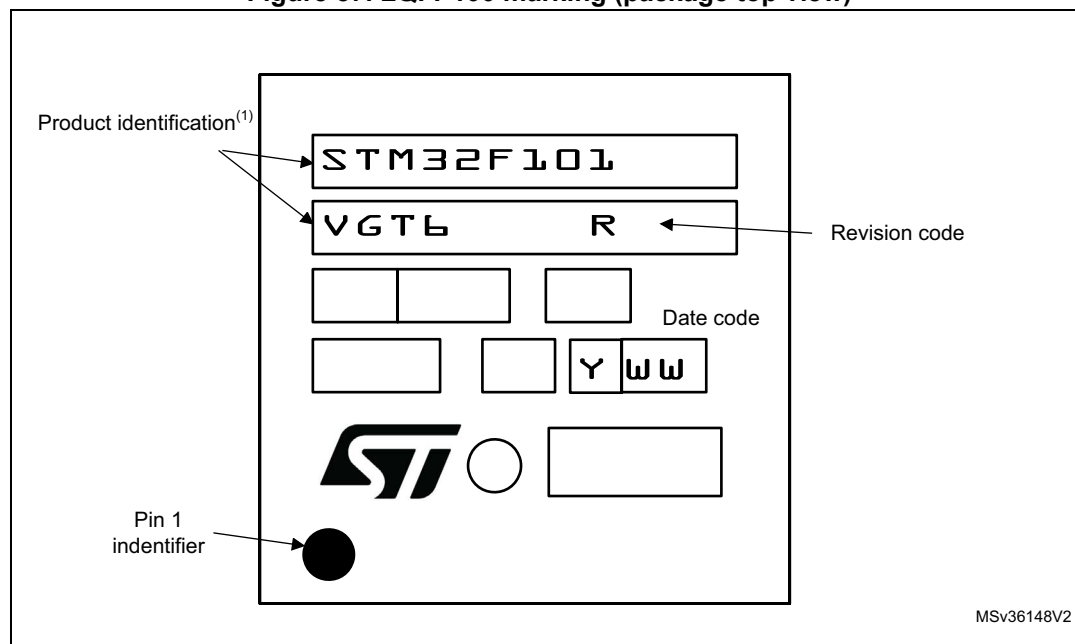
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking for LQFP100

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 57. LQFP100 marking (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 10: General operating conditions on page 39](#).

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 65. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP144 - 20 x 20 mm / 0.5 mm pitch	30	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	45	

6.4.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air), available from www.jedec.org.

6.4.2 Evaluating the maximum junction temperature for an application

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Table 66: STM32F101xF and STM32F101xG ordering information scheme](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature. Here, only temperature range 6 is available (–40 to 85 °C).

The following example shows how to calculate the temperature range needed for a given application, making it possible to check whether the required temperature range is compatible with the STM32F10xxx junction temperature range.

Example: High-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 82\text{ °C}$ (measured according to JESD51-2),
 $I_{DDmax} = 50\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$ and maximum 8 I/Os used at the same time in output mode at low level with $I_{OL} = 20\text{ mA}$, $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

This gives: $P_{INTmax} = 175\text{ mW}$ and $P_{IOmax} = 272\text{ mW}$

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

Thus: $P_{Dmax} = 447\text{ mW}$

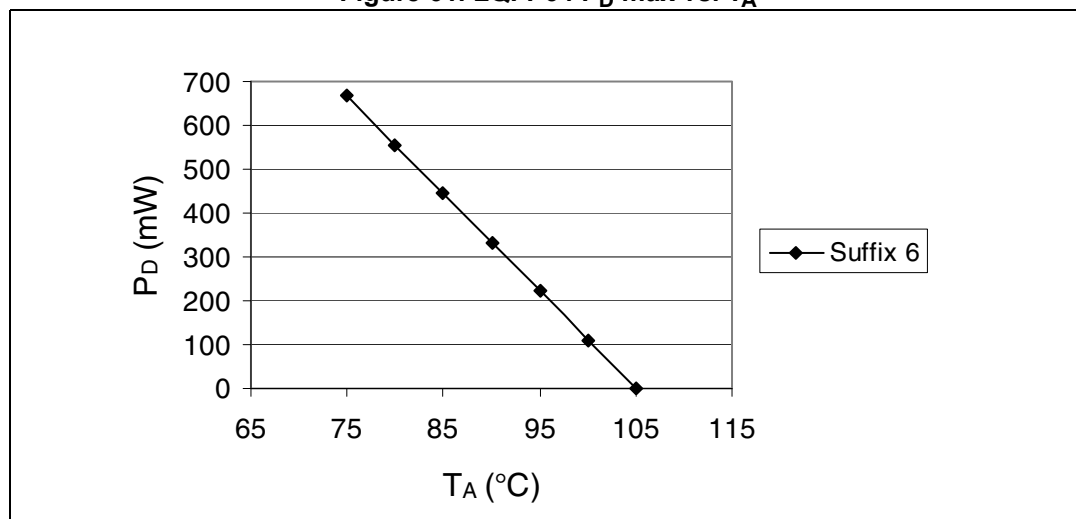
Using the values obtained in [Table 66](#) T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

$$T_{Jmax} = 82\text{ °C} + (45\text{ °C/W} \times 447\text{ mW}) = 82\text{ °C} + 20.1\text{ °C} = 102.1\text{ °C}$$

This is within the junction temperature range of the STM32F10xxx (–40 < T_J < 105 °C).

Figure 61. LQFP64 P_D max vs. T_A



7 Part numbering

Table 66. STM32F101xF and STM32F101xG ordering information scheme

Example:	STM32	F	101	R	F	T	6	xxx
Device family								
STM32 = ARM®-based 32-bit microcontroller								
Product type								
F = general-purpose								
Device subfamily								
101 = access line								
Pin count								
R = 64 pins								
V = 100 pins								
Z = 144 pins								
Flash memory size								
F = 768 Kbytes of Flash memory								
G = 1 Mbyte of Flash memory								
Package								
T = LQFP								
Temperature range								
6 = Industrial temperature range, –40 to 85 °C.								
Options								
xxx = programmed parts								
TR = tape and real								

For a list of available options (speed, package, etc..) or for further information on any aspect of this device, please contact your nearest ST sales office.